

Description

The AP100P04D uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

$V_{DS} = -40V$ $I_D = -100A$

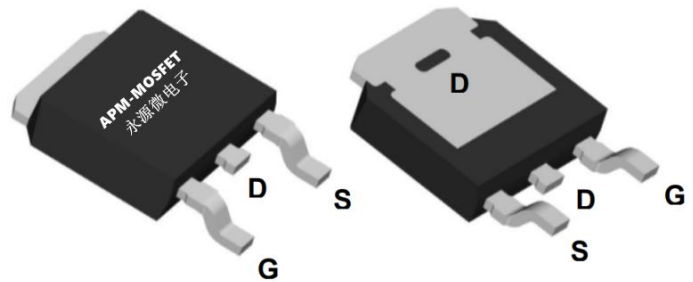
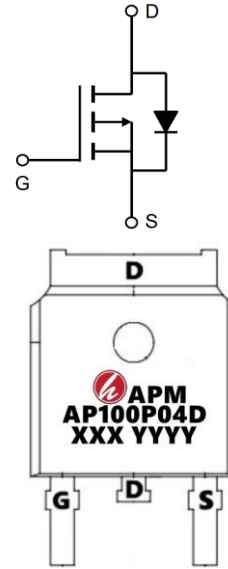
$R_{DS(ON)} < 5.8m\Omega$ @ $V_{GS} = -10V$ (Type: 4.6m Ω)

Application

Battery protection

Load switch

Uninterruptible power supply



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP100P04D	TO-252-3L	AP100P04D	5000

Absolute Maximum Ratings (TC=25°C unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-40	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ -10V^1$	-100	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ -10V^1$	-66	A
I_{DM}	Pulsed Drain Current ²	-300	A
EAS	Single Pulse Avalanche Energy ³	400	mJ
I_{AS}	Avalanche Current	-50	A
$P_D @ T_C = 25^\circ C$	Total Power Dissipation ⁴	52.1	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ C$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	62.5	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	1.8	$^\circ C/W$

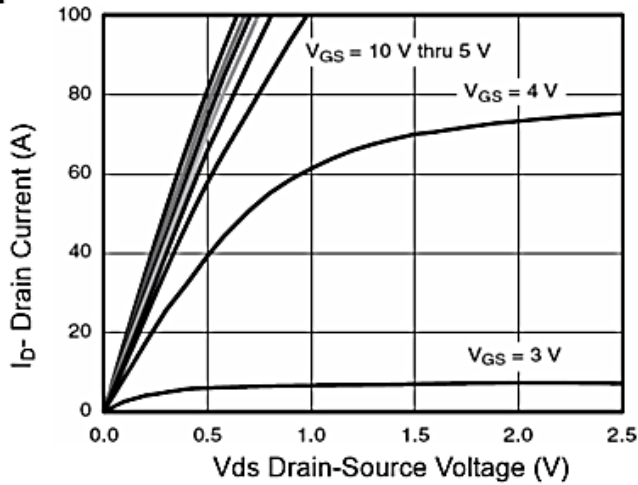
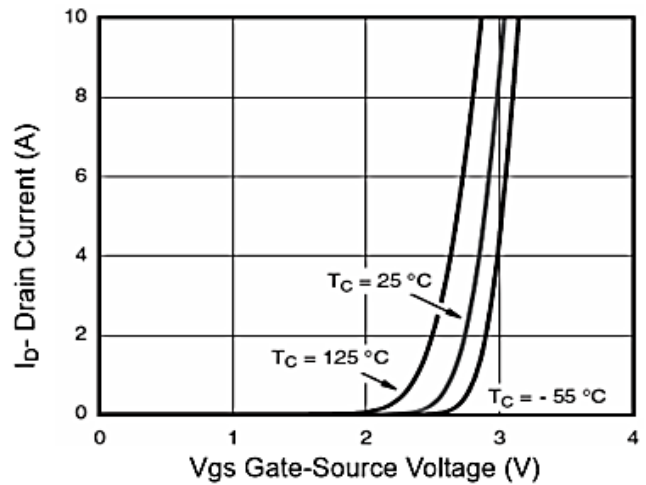
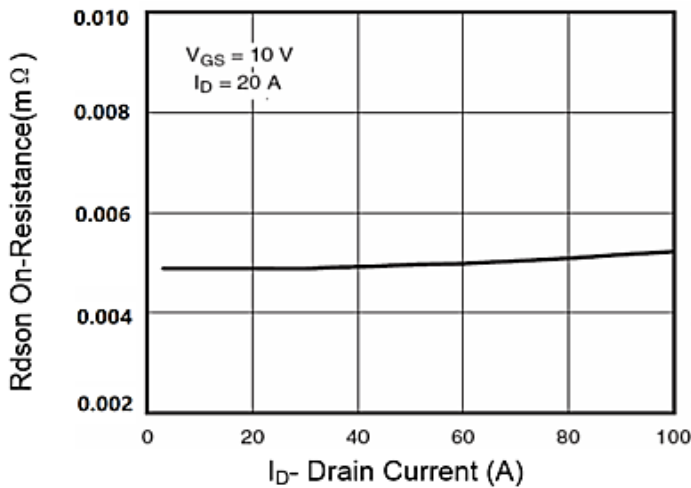
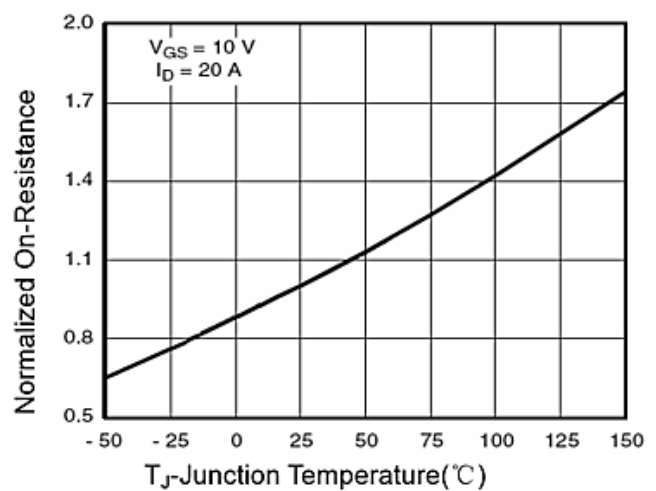
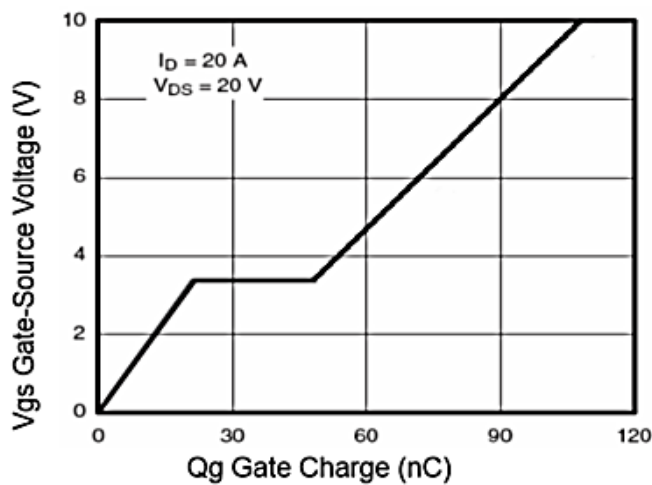
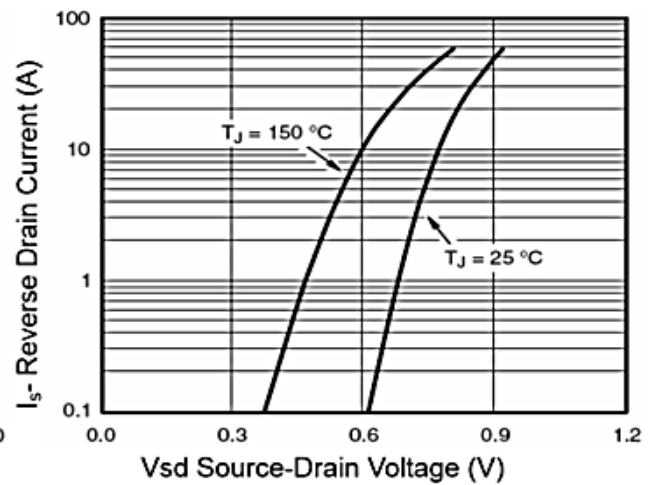
-40V P-Channel Enhancement Mode MOSFET

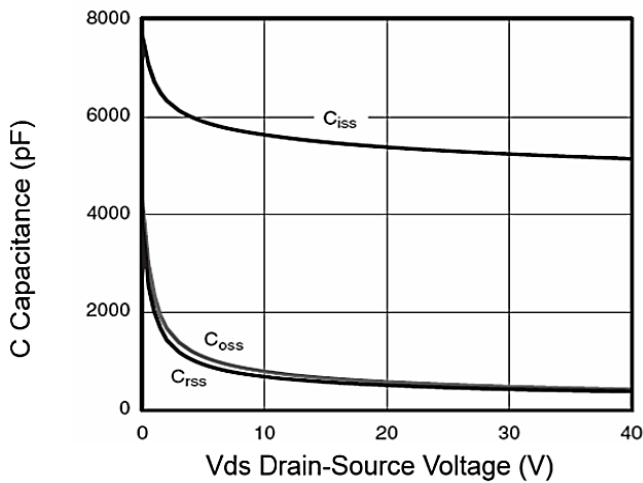
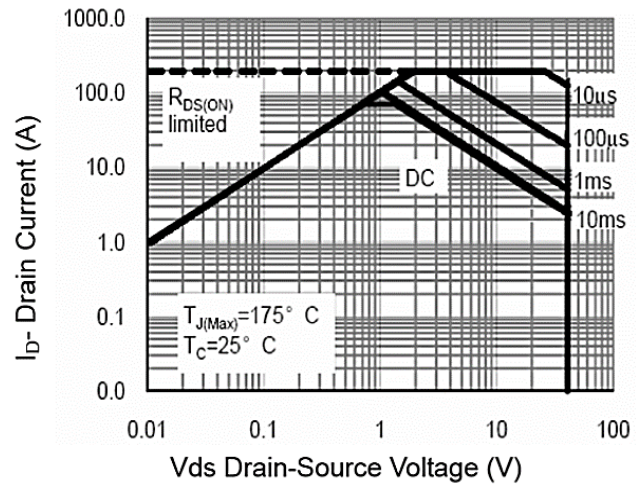
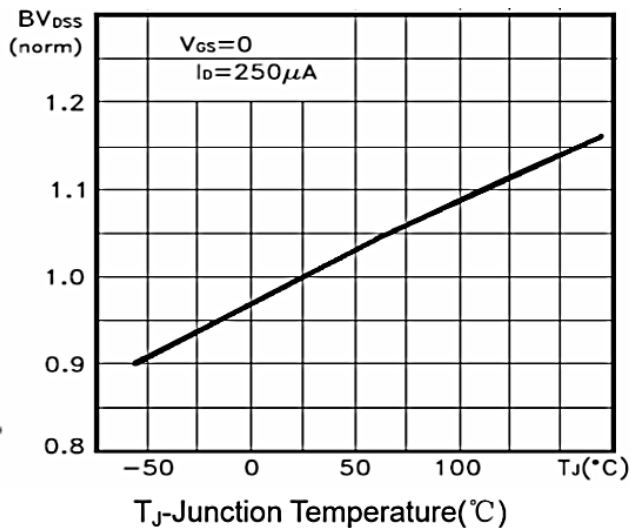
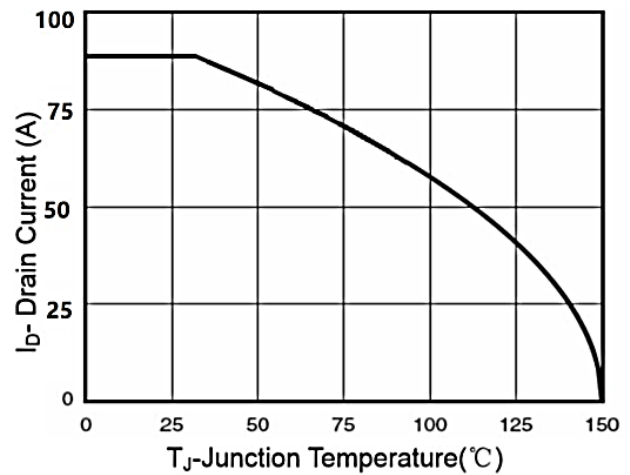
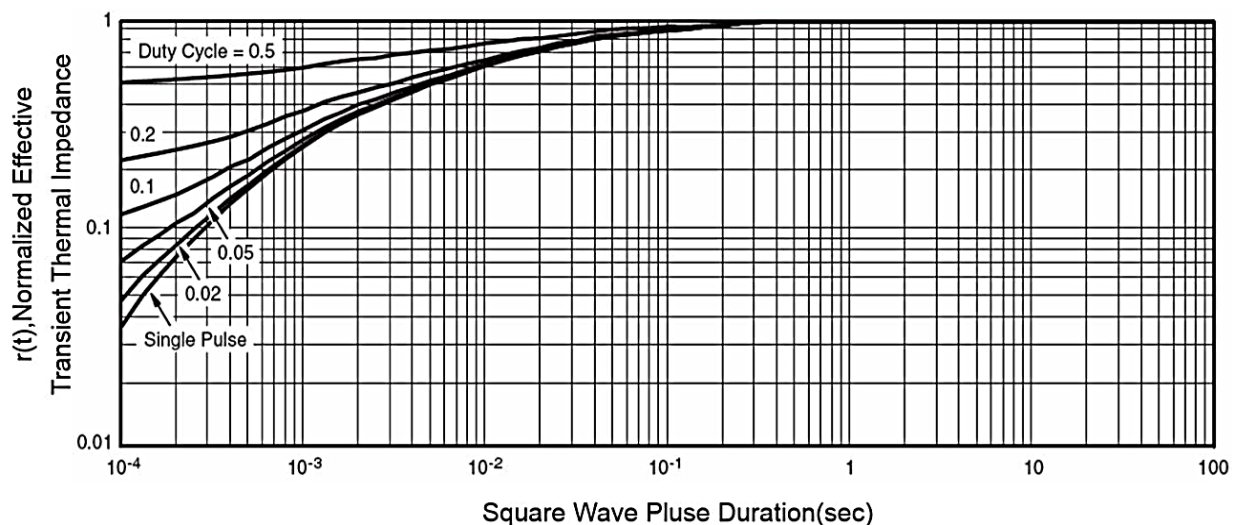
Electrical Characteristics ($T_J=25^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-40	-44	---	V
$\Delta BV_{DSS}/\Delta T_J$	BV_{DSS} Temperature Coefficient	Reference to 25°C , $I_D=-1\text{mA}$	---	-0.023	---	$V/^{\circ}\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=-10V, I_D=-20A$	---	4.6	5.8	m Ω
		$V_{GS}=-4.5V, I_D=-10A$	---	6.0	9.0	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=-250\mu A$	-1.2	-1.8	-2.5	V
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=-40V, V_{GS}=0V, T_J=25^{\circ}\text{C}$	---	---	1	μA
		$V_{DS}=-40V, V_{GS}=0V, T_J=55^{\circ}\text{C}$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{DS}=-15V, I_D=-12A$	---	50	---	S
R_g	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1\text{MHz}$	---	7	14	Ω
Q_g	Total Gate Charge (-4.5V)	$V_{DS}=-20V, V_{GS}=-10V, I_D=-12A$	---	120	---	nC
Q_{gs}	Gate-Source Charge		---	23	---	
Q_{gd}	Gate-Drain Charge		---	29	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=-20V, V_{GS}=-10V, R_G=3.0\Omega, I_D=-12A$	---	18	---	ns
T_r	Rise Time		---	12	---	
$T_{d(off)}$	Turn-Off Delay Time		---	80	---	
T_f	Fall Time		---	20	---	
C_{iss}	Input Capacitance	$V_{DS}=-20V, V_{GS}=0V, f=1\text{MHz}$	---	7000	---	pF
C_{oss}	Output Capacitance		---	950	---	
C_{rss}	Reverse Transfer Capacitance		---	735	---	
I_S	Continuous Source Current ^{1,5}	$V_G=V_D=0V$, Force Current	---	---	-100	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V, I_S=-1A, T_J=25^{\circ}\text{C}$	---	---	-1.2	V

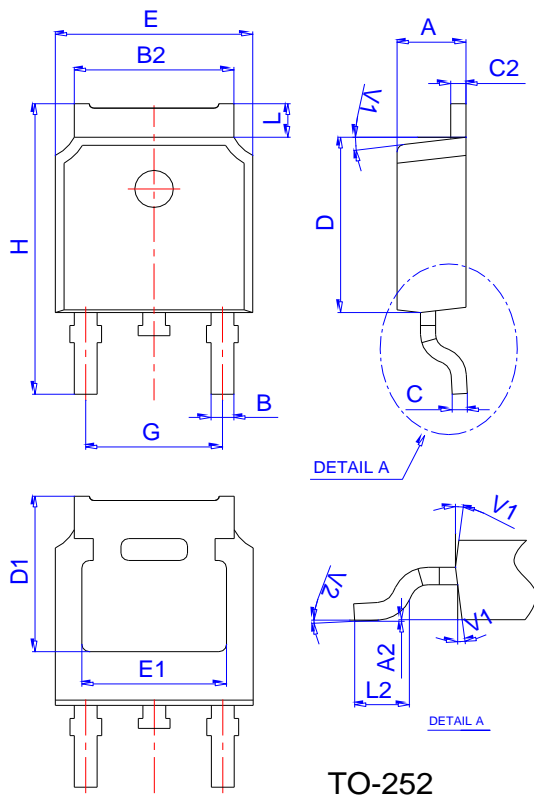
Note :

- 1、The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2、The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3、The EAS data shows Max. rating . The test condition is $V_{DD}=-32V, V_{GS}=-10V, L=0.1\text{mH}, I_{AS}=-50A$
- 4、The power dissipation is limited by 150°C junction temperature
- 5、The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

**Typical Characteristics****Figure 1 Output Characteristics****Figure 2 Transfer Characteristics****Figure 3 $R_{DS(on)}$ - Drain Current****Figure 4 $R_{DS(on)}$ -Junction Temperature****Figure 5 Gate Charge****Figure 6 Source- Drain Diode Forward**

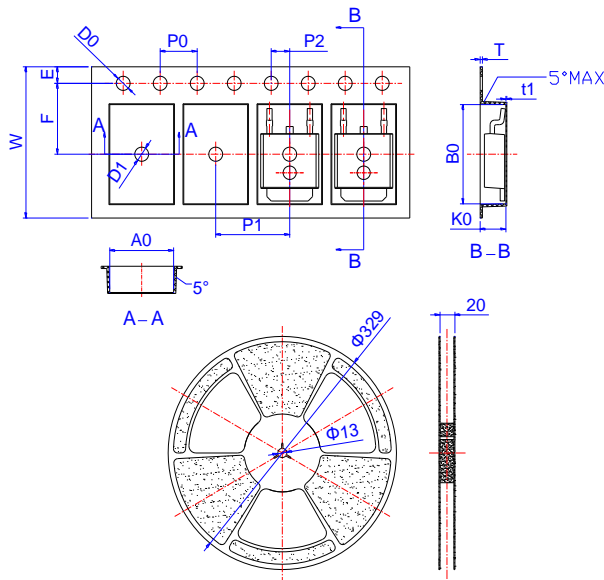
**-40V P-Channel Enhancement Mode MOSFET****Figure 7 Capacitance vs Vds****Figure 8 Safe Operation Area****Figure 9 BV_{DSS} vs Junction Temperature****Figure 10 ID Current Derating vs Junction Temperature****Figure 11 Normalized Maximum Transient Thermal Impedance**

Package Mechanical Data: TO-252-3L



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°

Reel Specification-TO-252



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
W	15.90	16.00	16.10	0.626	0.630	0.634
E	1.65	1.75	1.85	0.065	0.069	0.073
F	7.40	7.50	7.60	0.291	0.295	0.299
D0	1.40	1.50	1.60	0.055	0.059	0.063
D1	1.40	1.50	1.60	0.055	0.059	0.063
P0	3.90	4.00	4.10	0.154	0.157	0.161
P1	7.90	8.00	8.10	0.311	0.315	0.319
P2	1.90	2.00	2.10	0.075	0.079	0.083
A0	6.85	6.90	7.00	0.270	0.271	0.276
B0	10.45	10.50	10.60	0.411	0.413	0.417
K0	2.68	2.78	2.88	0.105	0.109	0.113
T	0.24		0.27	0.009		0.011
t1	0.10			0.004		
10P0	39.80	40.00	40.20	1.567	1.575	1.583

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AP100P04D

-40V P-Channel Enhancement Mode MOSFET

Edition	Date	Change
Rve1.0	2021/10/8	Initial release

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