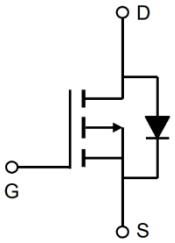
AP100P02NF

-20V P-Channel Enhancement Mode MOSFET

Description

The AP100P02NF uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.



General Features

V_{DS} = -20V I_D =-100 A

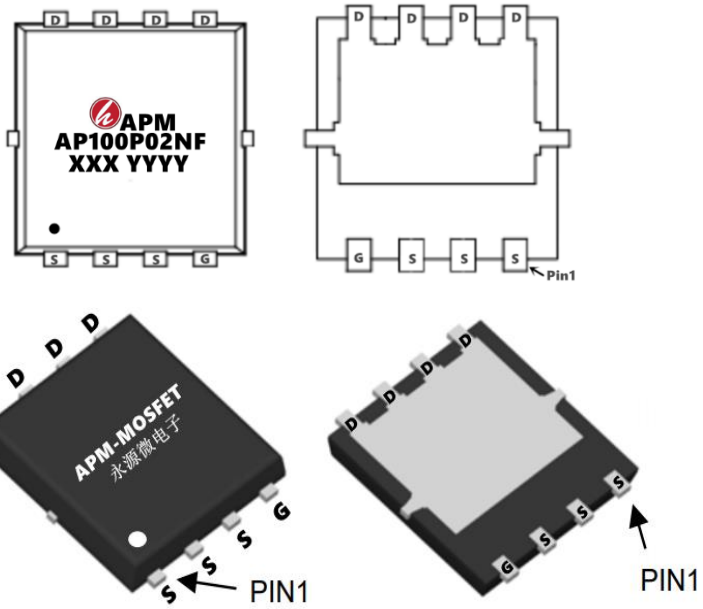
$R_{DS(ON)}$ < -2.7mΩ @ V_{GS}=-10V **(Type：2.1mΩ)**

Application

Battery protection

Load switch

Uninterruptible power supply



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP100P02NF	PDFN5*6-8L	AP100P02NF	5000

Absolute Maximum Ratings (TC=25℃unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-40	V
V_{GS}	Gate-Source Voltage	±20	V
I_D@T_C=25℃	Continuous Drain Current, V_{GS} @ -10V[1]	-100	A
I_D@T_C=100℃	Continuous Drain Current, V_{GS} @ -10V[1]	-66	A
I_{DM}	Pulsed Drain Current[2]	-340	A
EAS	Single Pulse Avalanche Energy[3]	400	mJ
I_{AS}	Avalanche Current	-50	A
P_D@T_C=25℃	Total Power Dissipation[4]	52.1	W
T_{STG}	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃
$R_{\theta JA}$	Thermal Resistance Junction-Ambient [1]	25	℃/W
$R_{\theta JC}$	Thermal Resistance Junction-Case[1]	1.8	℃/W

Electrical Characteristics (T_J=25℃, unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V(BR)DSS	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D= -250μA	-20	-	-	V
IDSS	Zero Gate Voltage Drain Current	V_{DS}= -20V, V_{GS}=0V,	-	-	-1	μA
IGSS	Gate to Body Leakage Current	V_{DS}=0V, V_{GS}= ±12V	-	-	±100	nA
VGS(th)	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D= -250μA	-0.4	0.6	-1.0	V
RDS(on)	Static Drain-Source on-Resistance	V_{GS}= -4.5V, I_D= -30A	-	2.1	2.7	mΩ
RDS(on)	Static Drain-Source on-Resistance	V_{GS}= -2.5V, I_D= -20A	-	2.7	3.8	
RDS(on)	Static Drain-Source on-Resistance	V_{GS}= -1.8V, I_D= -15A	-	3.8	5.7	
Ciss	Input Capacitance	V_{DS}= -10V, V_{GS}=0V, f=1.0MHz	-	15	-	nF
Coss	Output Capacitance		-	1600	-	pF
Crss	Reverse Transfer Capacitance		-	1068	-	pF
Q_g	Total Gate Charge	V_{DS}= -10V, I_D= -20A, V_{GS}= -4.5V	-	100	-	nC
Qgs	Gate-Source Charge		-	21	-	nC
Qgd	Gate-Drain(“Miller”) Charge		-	32	-	nC
td(on)	Turn-on Delay Time	V_{DD} = -10V, R_L=0.5Ω, V_{GS}= -4.5V, R_{GEN}=3Ω	-	20	-	ns
tr	Turn-on Rise Time		-	50	-	ns
td(off)	Turn-off Delay Time		-	100	-	ns
t_f	Turn-off Fall Time		-	40	-	ns
IS	Maximum Continuous Drain to Source Diode Forward Current		-	-	-10	A
ISM	Maximum Pulsed Drain to Source Diode Forward Current		-	-	-340	A
VSD	Drain to Source Diode Forward Voltage	V_{GS}=0V, I_S= -30A	-	-0.8	-1.2	V

Note :

1、The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper.

2、The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%

3、The EAS data shows Max. rating . The test condition is VDD=-16V,VGS=-4.5V,L=0.1mH,IAS=-50A

4、The power dissipation is limited by 150℃ junction temperature

5、The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

Typical Characteristics

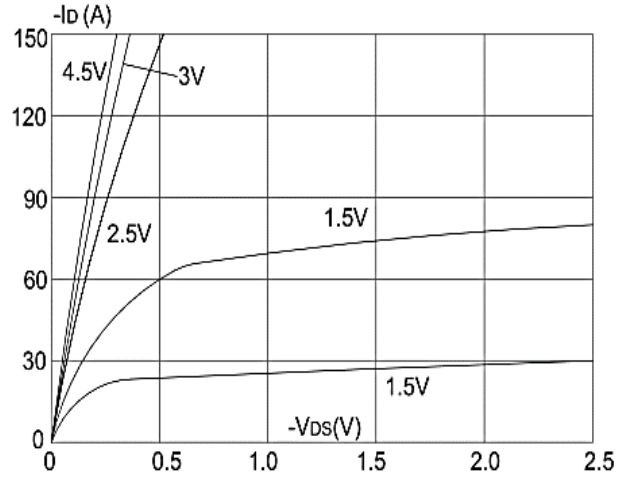


Figure1: Output Characteristics

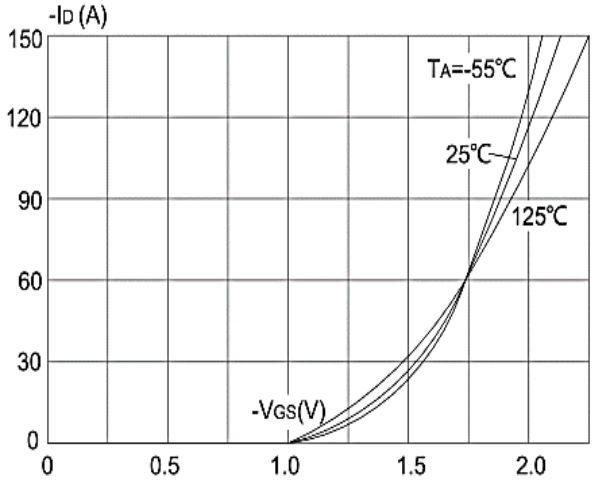


Figure 2: Typical Transfer Characteristics

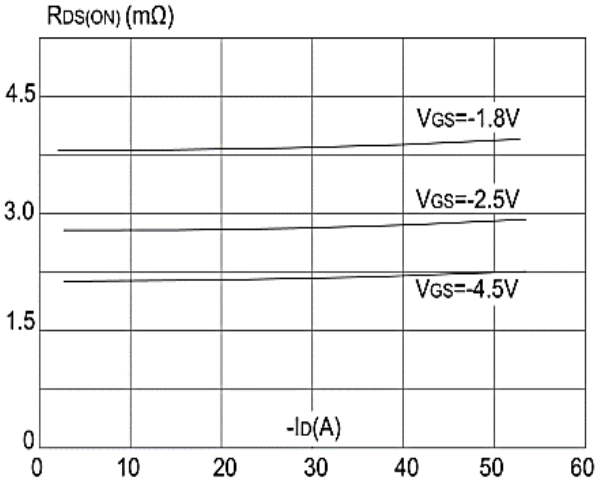


Figure 3:On-resistance vs. Drain Current

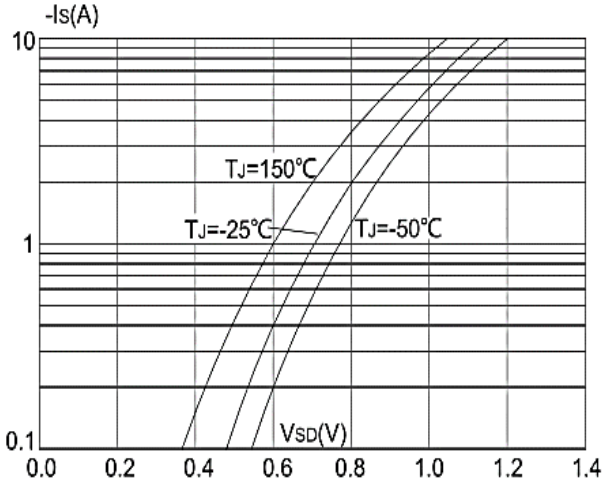


Figure 4: Body Diode Characteristics

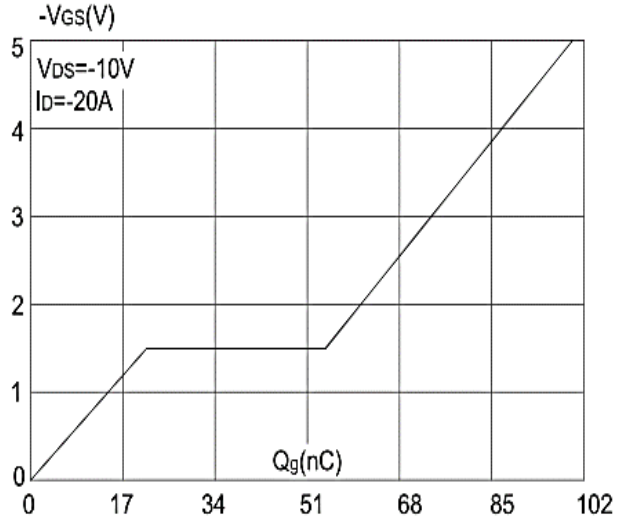


Figure 5: Gate Charge Characteristics

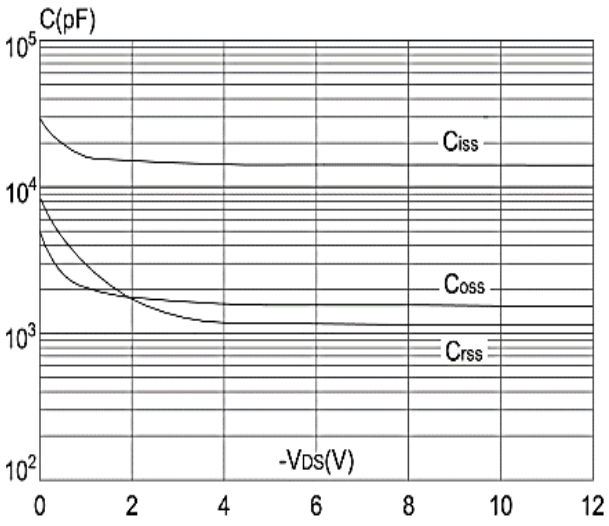


Figure 6: Capacitance Characteristics

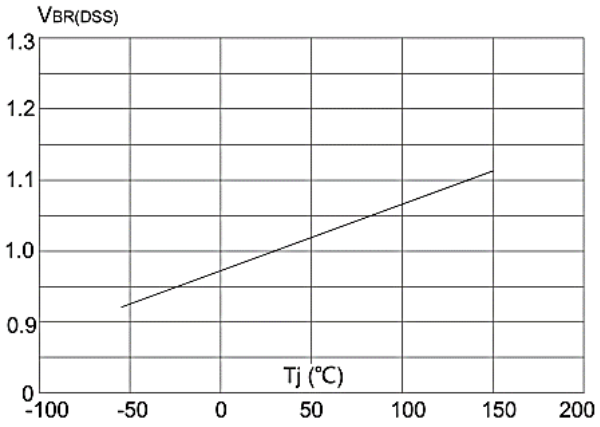


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

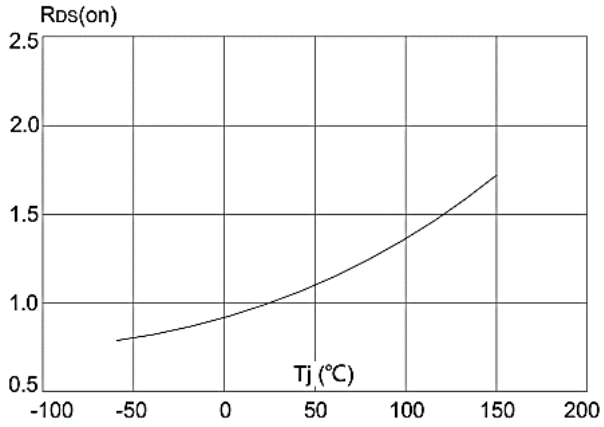


Figure 8: Normalized on Resistance vs Junction Temperature

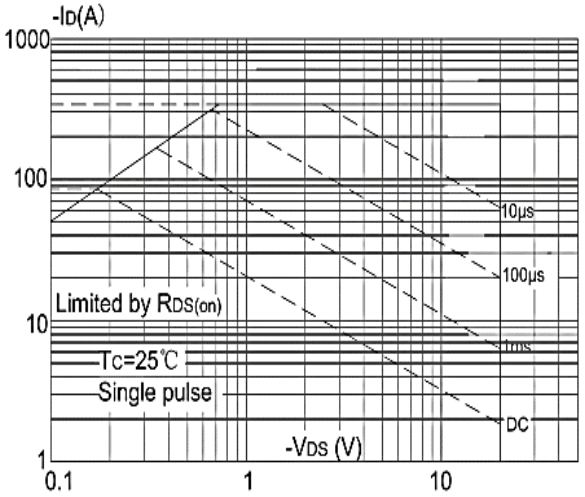


Figure 9: Maximum Safe Operating Area

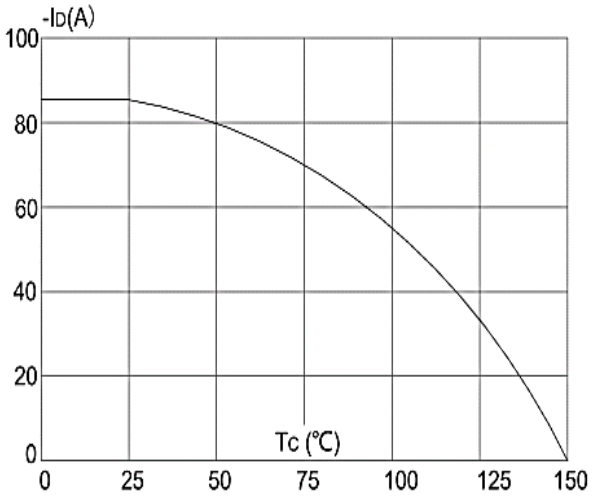


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

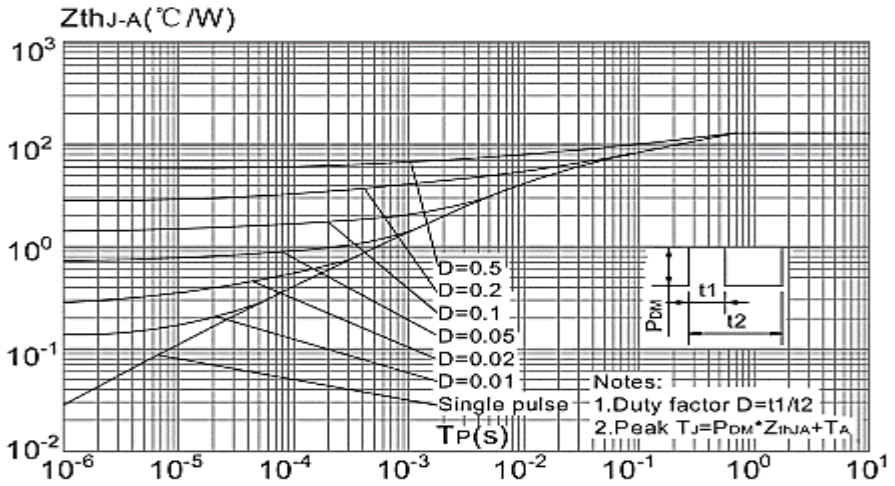
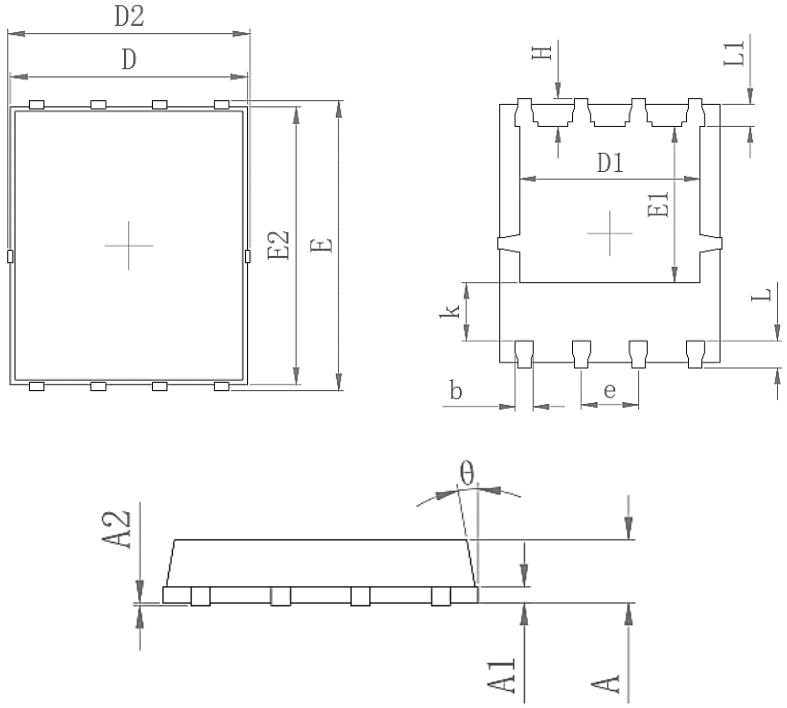


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Case

Package Mechanical Data-PDFN5X6-8L-XZT Single



Symbol	Common	
	mm	
	Mim	Max
A	0.90	1.10
A1	0.254 REF	
A2	0-0.05	
D	4.824	4.976
D1	3.910	4.110
D2	4.944	5.076
E	5.924	6.076
E1	3.375	3.575
E2	5.674	5.826
b	0.350	0.450
e	1.270	
L	0.534	0.686
L1	0.424	0.576
K	1.190	1.390
H	0.549	0.701
Φ	8°	12°

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-20V P-Channel Enhancement Mode MOSFET

Edition	Date	Change
Rve1.0	2021/10/8	Initial release