

-60V P-Channel Enhancement Mode MOSFET

Description

The AP50P06P uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

$V_{DS} = -60V$ $I_D = -50A$

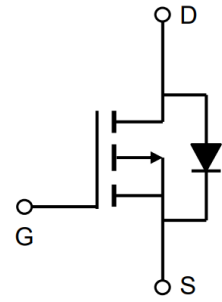
$R_{DS(ON)} < -18m\Omega$ @ $V_{GS} = -10V$

Application

Battery protection

Load switch

Uninterruptible power supply



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP50P06P	TO-220-3L	AP50P06P XXX YYYY	1000
AP50P06T	TO-263-3L	AP50P06T XXX YYYY	1000

Absolute Maximum Ratings (TC=25°C unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-60	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D @ T_C = 25^\circ C$	Continuous Drain Current ¹	-50	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current ¹	-34	A
I_{DM}	Pulsed Drain Current ²	-90	A
EAS	Single Pulse Avalanche Energy ³	101	mJ
I_{AS}	Avalanche Current	-45	A
$P_D @ T_C = 25^\circ C$	Total Power Dissipation ⁴	86.8	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ C$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	62	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	1.44	$^\circ C/W$

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Electrical Characteristics ($T_C=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-60	---	---	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=-10V, I_D=-18A$	---	13	18	m Ω
		$V_{GS}=-4.5V, I_D=-12A$	---	29	35	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=-250\mu A$	-1.0	1.8	-3.0	V
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=-48V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	1	μA
		$V_{DS}=-48V, V_{GS}=0V, T_J=55^\circ\text{C}$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{DS}=-10V, I_D=-18A$	---	23	---	S
R_g	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1\text{MHz}$	---	7	14	
Q_g	Total Gate Charge (-4.5V)	$V_{DS}=-20V, V_{GS}=-4.5V, I_D=-12A$	---	25	---	nC
Q_{gs}	Gate-Source Charge		---	6.7	---	
Q_{gd}	Gate-Drain Charge		---	5.5	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=-15V, V_{GS}=-10V, R_G=3.3, I_D=-1A$	---	38	---	ns
T_r	Rise Time		---	23.6	---	
$T_{d(off)}$	Turn-Off Delay Time		---	100	---	
T_f	Fall Time		---	6.8	---	
C_{iss}	Input Capacitance	$V_{DS}=-15V, V_{GS}=0V, f=1\text{MHz}$	---	3635	---	pF
C_{oss}	Output Capacitance		---	224	---	
C_{rss}	Reverse Transfer Capacitance		---	141	---	
I_S	Continuous Source Current ^{1,5}	$V_G=V_D=0V, \text{Force Current}$	---	---	-20	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V, I_S=-1A, T_J=25^\circ\text{C}$	---	---	-1	V

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is $V_{DD}=-25V, V_{GS}=-10V, L=0.1mH, I_{AS}=-45A$
- 4.The power dissipation is limited by 150 $^\circ\text{C}$ junction temperature
- 5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

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Typical Characteristics

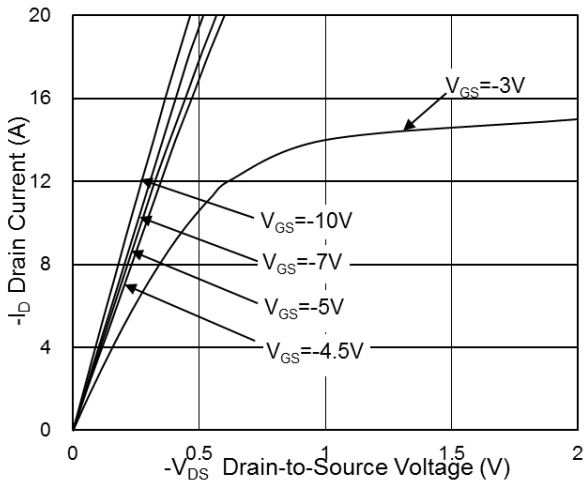


Fig.1 Typical Output Characteristics

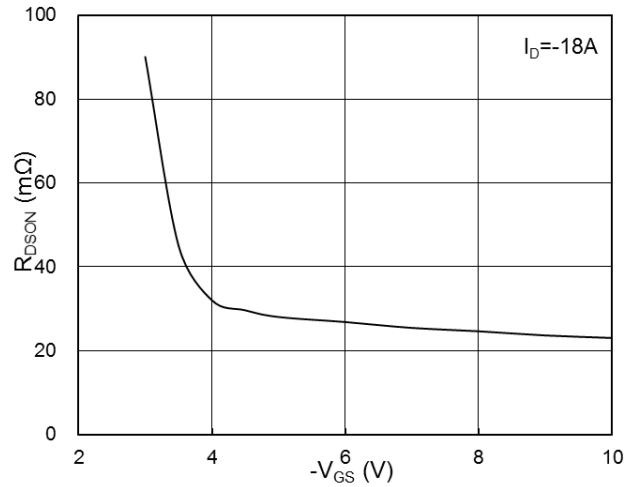


Fig.2 On-Resistance vs. G-S Voltage

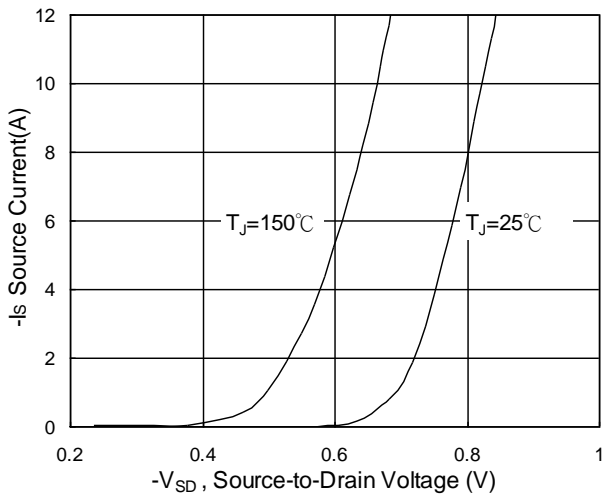


Fig.3 Source Drain Forward Characteristics

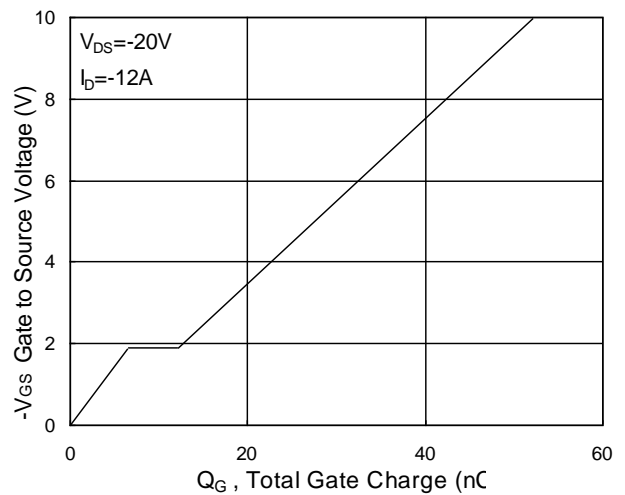


Fig.4 Gate-Charge Characteristics

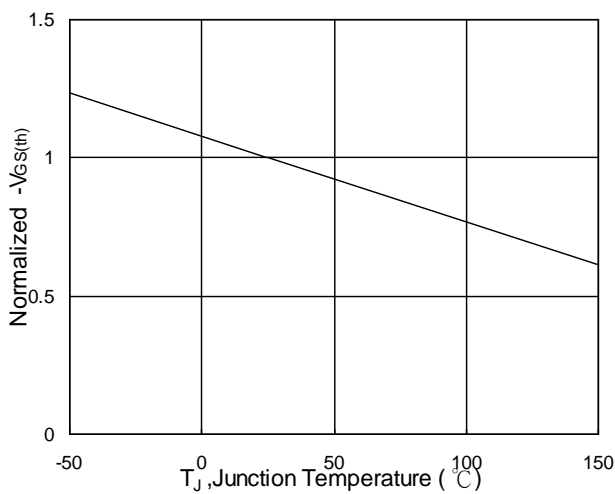


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

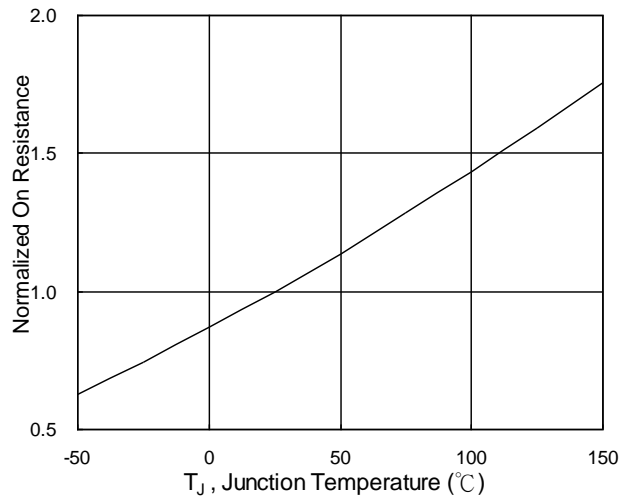


Fig.6 Normalized $R_{DS(on)}$ vs. T_J



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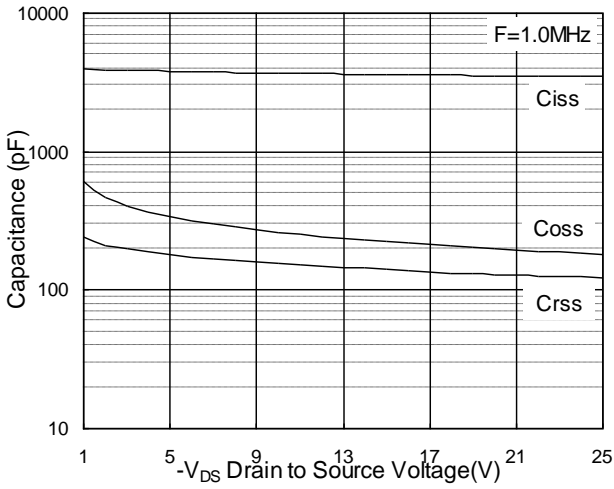


Fig.7 Capacitance

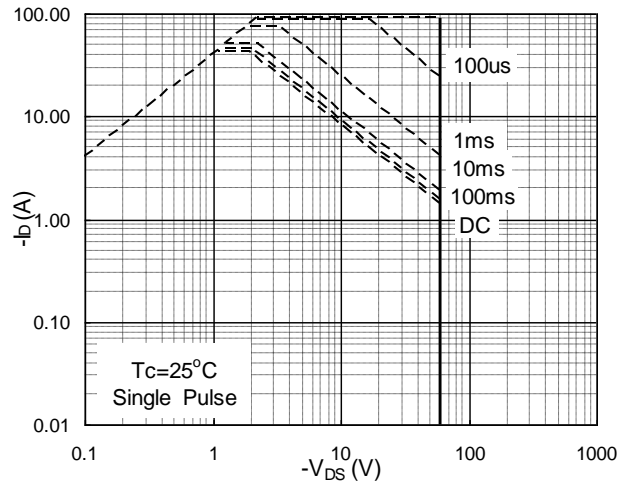


Fig.8 Safe Operating Area

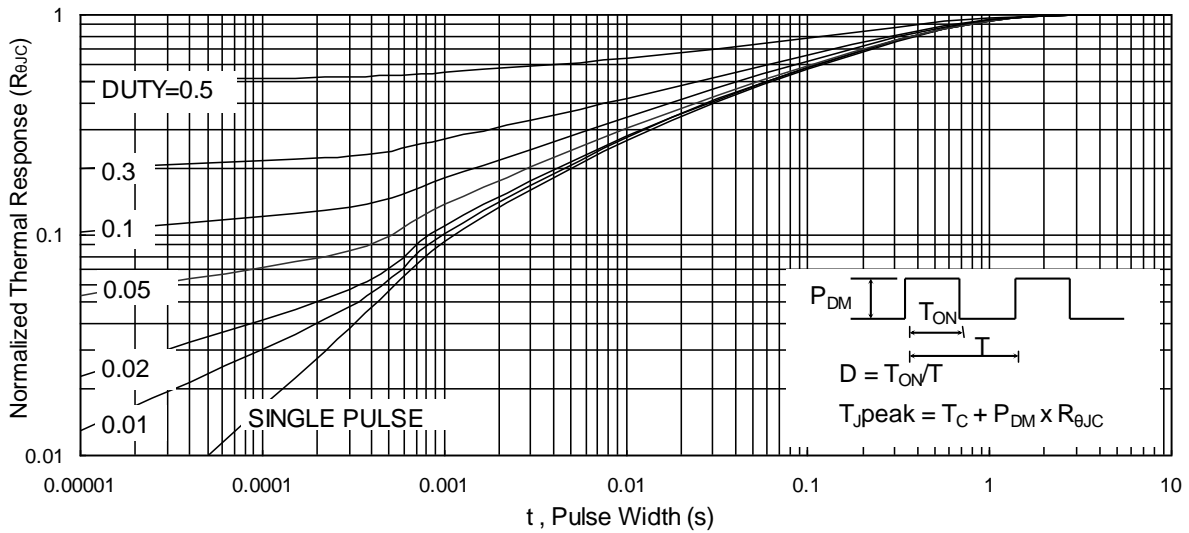


Fig.9 Normalized Maximum Transient Thermal Impedance

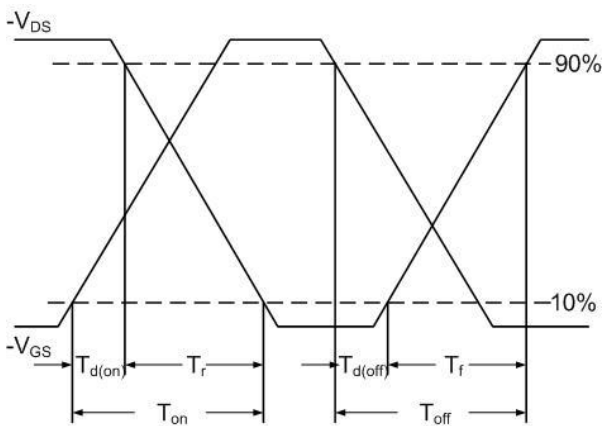


Fig.10 Switching Time Waveform

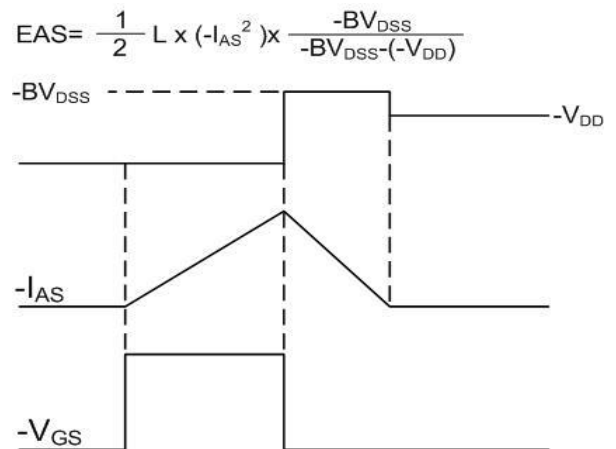
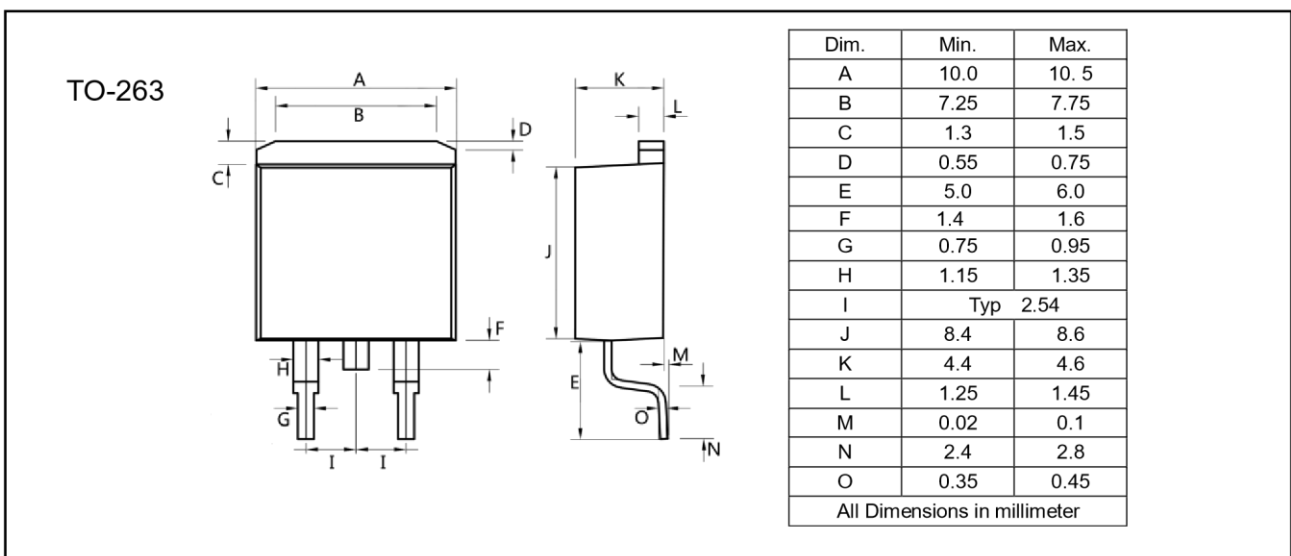
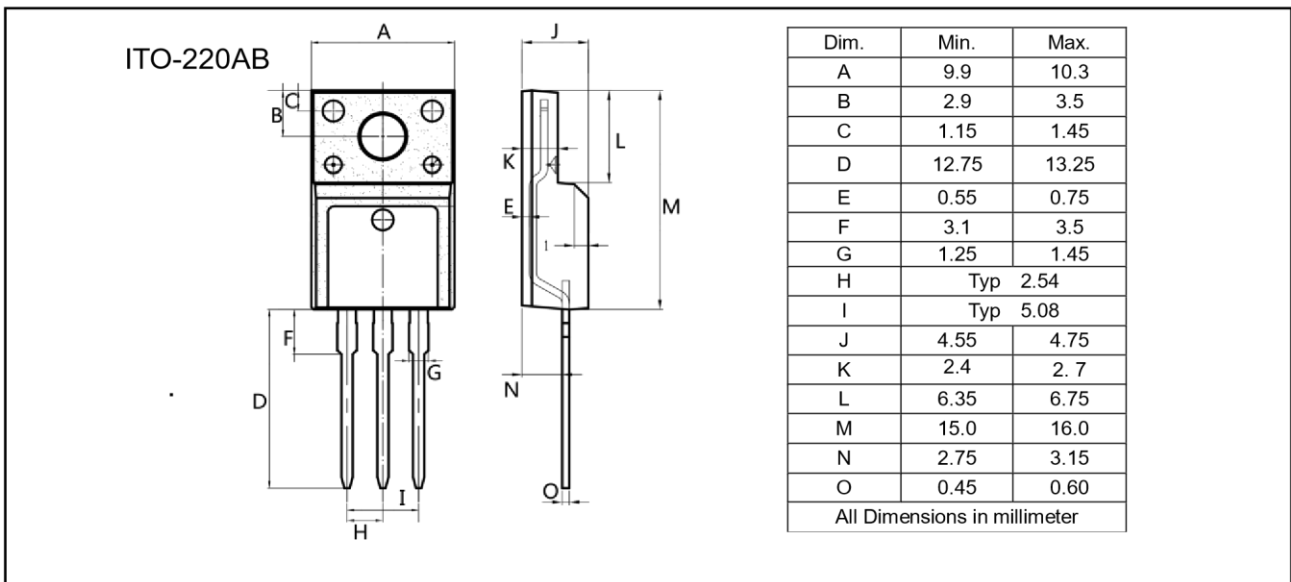
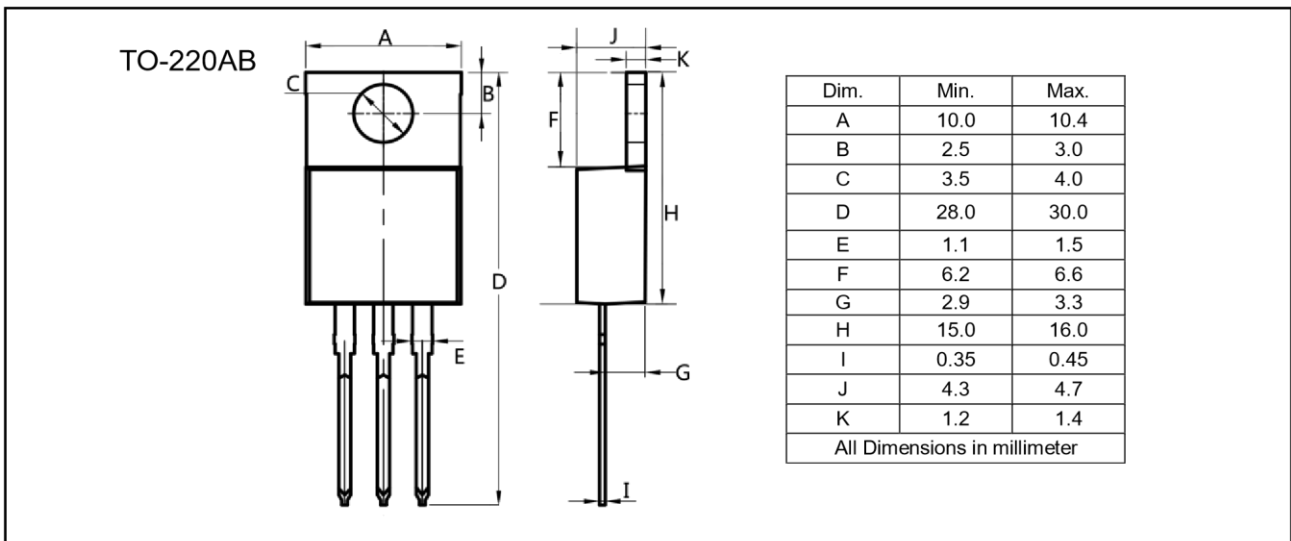


Fig.11 Unclamped Inductive Waveform

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