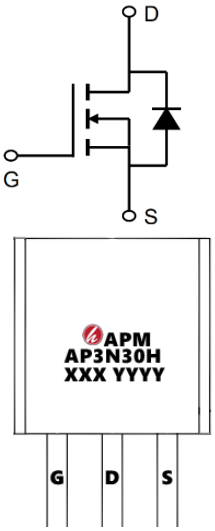
# AP3N30H

## 300V N-Channel Enhancement Mode MOSFET

### Description

The AP3N30H is silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency.




### General Features

$V_{DS}$ = 300V $I_D$ =3A

$R_{DS(ON)}$ < 4000mΩ @ $V_{GS}$=10V （**Type：2600mΩ**）

### Application

Load switch

Uninterruptible power supply


### Package Marking and Ordering Information

| Product ID | Pack | Marking | Qty(PCS) |
|---|---|---|---|
| AP3N30H | TO-92-3L | AP3N30H XXX YYYY | 4000 |

### Absolute Maximum Ratings ($T_C$=25℃unless otherwise noted)

| Symbol | Parameter | Rating | Units |
|---|---|---|---|
| VDS | Drain-Source Voltage | 300 | V |
| VGS | Gate-Source Voltage | ±20 | V |
| $I_D$@$T_A$=25℃ | Continuous Drain Current, $V_{GS}$ @ 10V[1] | 3 | A |
| $I_D$@$T_A$=70℃ | Continuous Drain Current, $V_{GS}$ @ 10V[1] | 1.7 | A |
| IDM | Pulsed Drain Current[2] | 9 | A |
| $P_D$@$T_A$=25℃ | Total Power Dissipation[3] | 1.5 | W |
| TSTG | Storage Temperature Range | -55 to 150 | ℃ |
| $T_J$ | Operating Junction Temperature Range | -55 to 150 | ℃ |
| $R_{\theta}$JA | Thermal Resistance Junction-ambient[1] | 100 | ℃/W |
| $R_{\theta}$JC | Thermal Resistance Junction-Case[1] | 30 | ℃/W |

## Electrical Characteristics ($T_J$=25°C, unless otherwise noted)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| V(BR)DSS | Drain-Source Breakdown Voltage | $V_{GS}$ = 0V, $I_D$ = 250μA | 300 | 330 | -- | V |
| VGS(th) | Gate-Source Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250μA | 2.0 | 3.5 | 4.0 | V |
| RDS(on) | Drain-Source On-Resistance | $V_{GS}$ = 10V, $I_D$ = 1.5A | -- | 2600 | 4000 | mΩ |
| IDSS | Zero Gate Voltage Drain Current | $V_{DS}$ = 300V, $V_{GS}$ = 0V, $T_J$ = 25ºC | -- | -- | 1 | μA |
| | | $V_{DS}$ = 240V, $V_{GS}$ = 0V, $T_J$ = 125ºC | -- | -- | 100 | |
| IGSS | Gate-Source Leakage | $V_{GS}$ = ±20V | -- | -- | ±100 | nA |
| $C_{iss}$ | Input Capacitance | $V_{GS}$ = 0V, $V_{DS}$ = 20V, f = 1.0MHz | -- | 138 | -- | pF |
| $C_{oss}$ | Output Capacitance | | -- | 30 | -- | |
| $C_{rss}$ | Reverse Transfer Capacitance | | -- | 5 | -- | |
| $Q_g$ | Total Gate Charge | $V_{DD}$ = 240V, $I_D$ = 3.0A, $V_{GS}$ = 10V | -- | 4.4 | -- | nC |
| $Q_{gs}$ | Gate-Source Charge | | -- | 0.7 | -- | |
| $Q_{gd}$ | Gate-Drain Charge | | -- | 2 | -- | |
| td(on) | Turn-on Delay Time | $V_{DD}$ = 150V, $I_D$ = 3.0A, $R_G$ = 25 Ω | -- | 18 | -- | ns |
| $t_r$ | Turn-on Rise Time | | -- | 55 | -- | |
| td(off) | Turn-off Delay Time | | -- | 60 | -- | |
| $t_f$ | Turn-off Fall Time | | -- | 55 | -- | |
| $I_S$ | Continuous Body Diode Current | $T_C$ = 25 ºC | -- | -- | 3 | A |
| ISM | Pulsed Diode Forward Current | | -- | -- | 12 | |
| $t_{rr}$ | Reverse Recovery Time | $V_{GS}$ = 0V,$I_S$ = 3A, $di_F/dt$ =100A /μs | -- | 250 | -- | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | -- | 1.8 | -- | μC |
| $V_{SD}$ | Body Diode Voltage | $T_J$ = 25ºC, $I_{SD}$ = 3A, $V_{GS}$ = 0V | -- | -- | 1.4 | V |

**Note :**

1、The data tested by surface mounted on a 1 inch$^2$ FR-4 board with 2OZ copper.

2、The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%

3、The power dissipation is limited by 150℃ junction temperature

4、The data is theoretically the same as $I_D$ and $I_{DM}$ , in real applications , should be limited by total power dissipation.

## Typical Characteristics

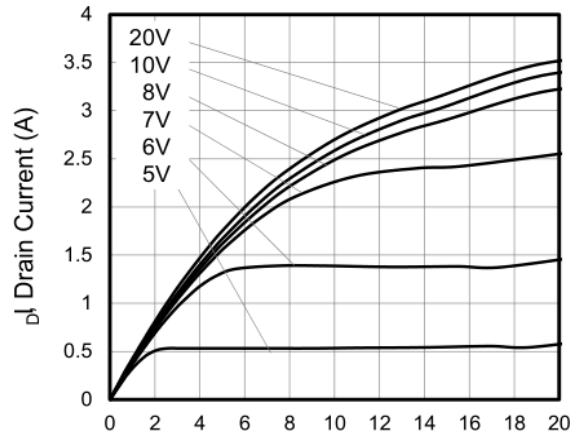



Figure 1. Output Characteristics

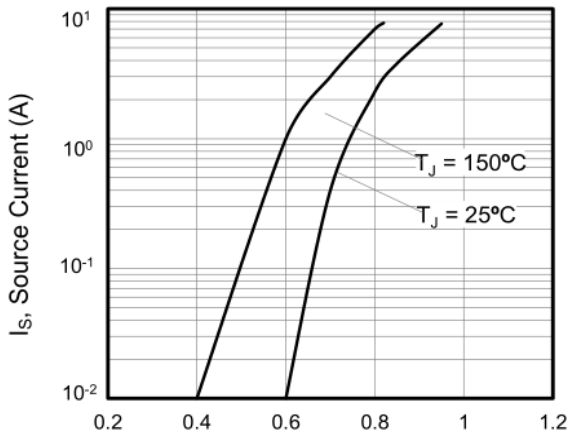



Figure 2. Body Diode Forward Voltage

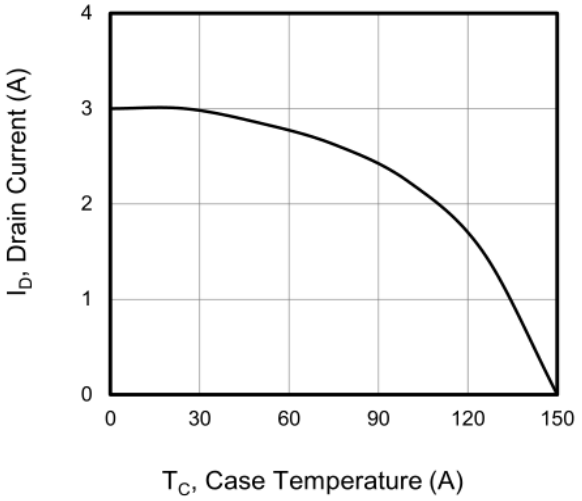



Figure 3. Drain Current vs. Temperature

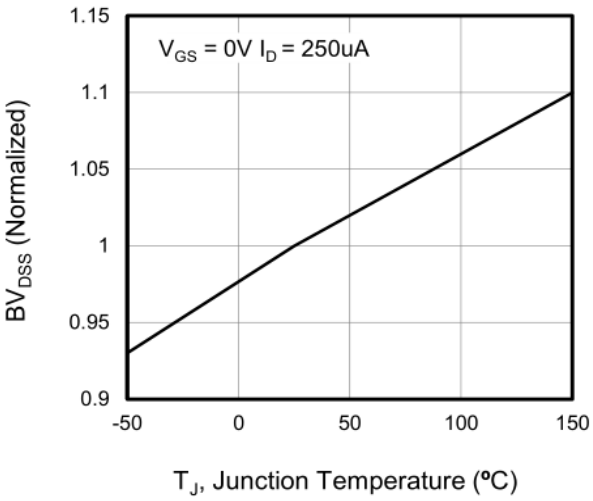



Figure 4. BVDSS Variation vs. Temperature

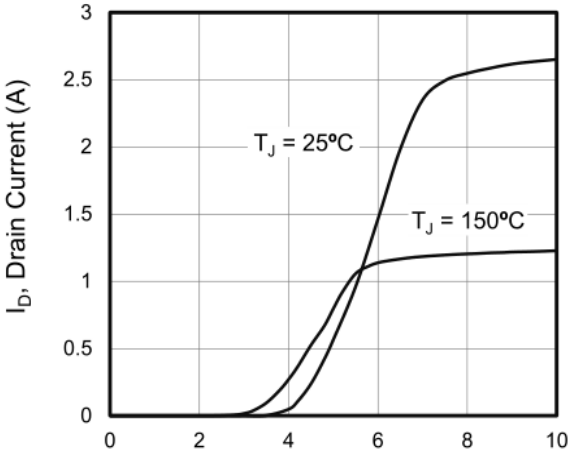



Figure 5. Transfer Characteristics

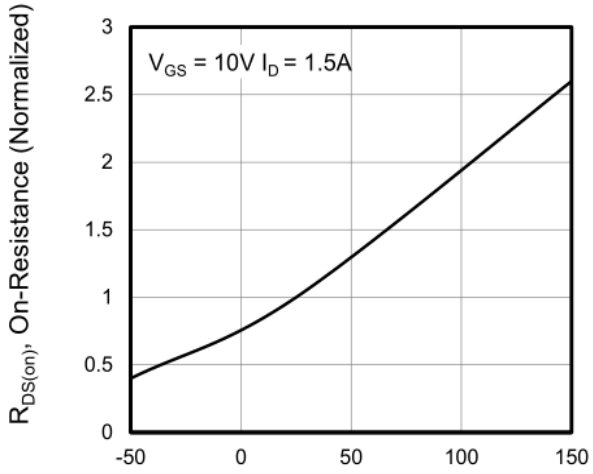



Figure 6. On-Resistance vs. Temperature

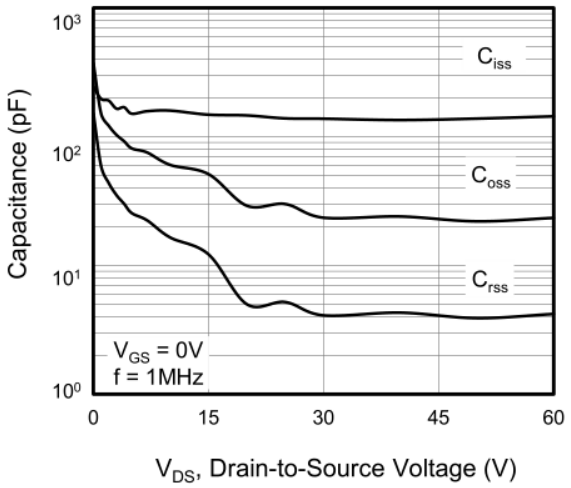



**Figure 7. Capacitance**

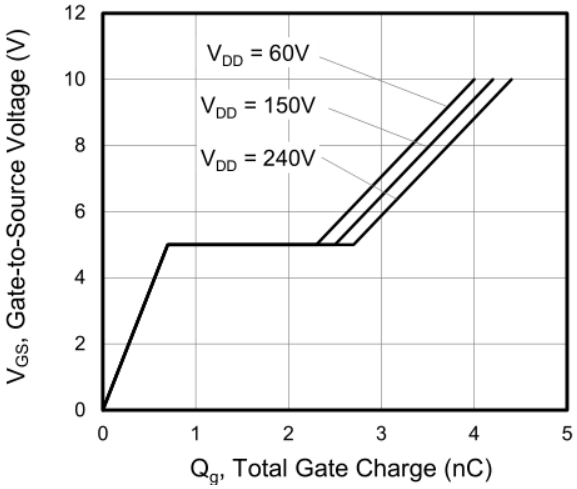



**Figure 8. Gate Charge**

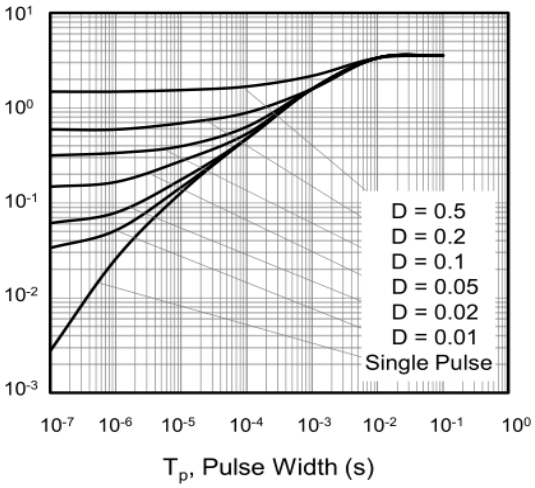
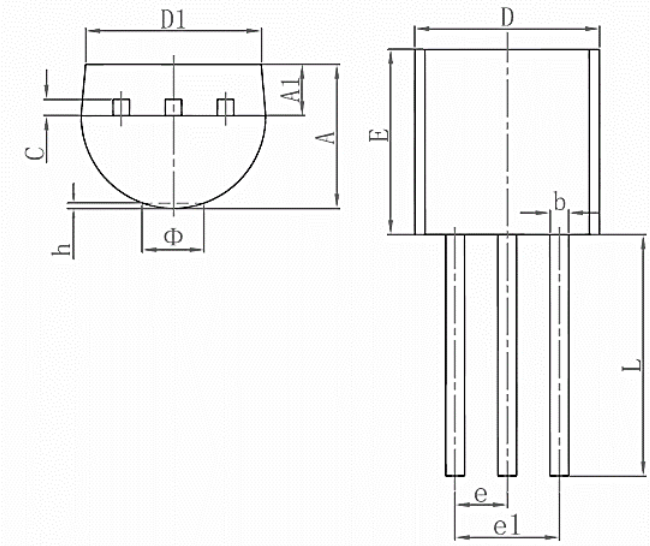



**Figure 9. Transient Thermal Impedance**

## Package Mechanical Data-TO-92-3LSingle




| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 3.300 | 3.700 | 0.130 | 0.146 |
| A1 | 1.100 | 1.400 | 0.043 | 0.055 |
| b | 0.380 | 0.550 | 0.015 | 0.022 |
| c | 0.360 | 0.510 | 0.014 | 0.020 |
| D | 4.400 | 4.700 | 0.173 | 0.185 |
| D1 | 3.430 | | 0.135 | |
| E | 4.300 | 4.700 | 0.169 | 0.185 |
| e | 1.270 TYP | | 0.050 TYP | |
| e1 | 2.440 | 2.640 | 0.096 | 0.104 |
| L | 14.100 | 14.500 | 0.555 | 0.571 |
| Φ | | 1.600 | | 0.063 |
| h | 0.000 | 0.380 | 0.000 | 0.015 |

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## 300V N-Channel Enhancement Mode MOSFET

| Edition | Date | Change |
|---|---|---|
| Rve1.0 | 2018/12/21 | Initial release |