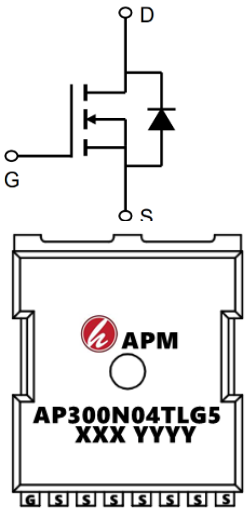
AP300N04TLG5

40V N-Channel Enhancement Mode MOSFET

Description

The AP300N04TLG5 uses advanced **APM-SGT V** technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.



TOLLA

General Features

V_{DS} = 40V I_D =300A

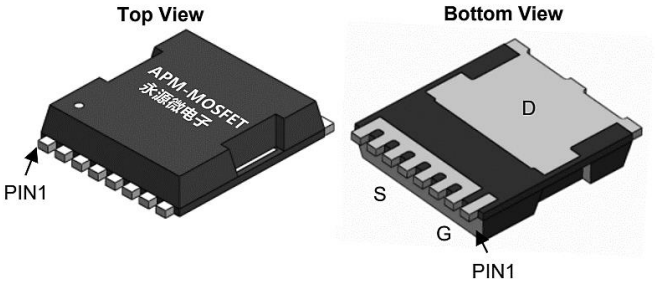
$R_{DS(ON)}$ < 1.5mΩ @ V_{GS}=10V **（Type：1.2mΩ）**

Application

BMS

BLDC

UPS



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP300N04TLG5	TOLLA-8L	AP300N04TLG5 XXX YYYY	2000

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Symbol	Parameter	Max.	Units
VDSS	Drain-Source Voltage	40	V
VGSS	Gate-Source Voltage	±20	V
ID@TC=25℃	Continuous Drain Current, VGS @ 10V1	300	A
ID@TC=100℃	Continuous Drain Current, VGS @ 10V1	210	A
IDM	Pulsed Drain Current	900	A
EAS	Single Pulsed Avalanche Energy	510	mJ
IAS	Avalanche Current	70	A
PD@TC=25℃	Power Dissipation	230	W
$R_{\theta}JA$	Thermal Resistance Junction-Ambient [1]	35	°C/W
RθJC	Thermal Resistance, Junction to Case	1.9	℃/W
T_J	Operating Junction Temperature Range	-55 to 150	°C
TSTG	Storage Temperature Range	-55 to 150	°C

N-Channel Electrical Characteristics (T_J=25 ℃, unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V(BR)DSS	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	40	48	-	V
IDSS	Zero Gate Voltage Drain Current	V_{DS}=40V, V_{GS}=0V,	-	-	1.0	μA
IGSS	Gate to Body Leakage Current	V_{DS}=0V, V_{GS}= ±20V	-	-	±100	nA
VGS(th)	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	1.0	1.8	2.5	V
RDS(on)	Static Drain-Source on-Resistance	V_{GS}=10V, I_D=30A	-	1.2	1.5	mΩ
		V_{GS}=4.5V, I_D=20A	-	1.7	2.5	mΩ
Ciss	Input Capacitance	V_{DS}=20V, V_{GS}=0V, f=1.0MHz	-	8300	-	pF
Coss	Output Capacitance		-	1510	-	pF
Crss	Reverse Transfer Capacitance		-	130	-	pF
Q_g	Total Gate Charge	V_{DS}=20V, I_D=85A, V_{GS}=10V	-	127	-	nC
Qgs	Gate-Source Charge		-	35	-	nC
Qgd	Gate-Drain(“Miller”) Charge		-	26	-	nC
td(on)	Turn-on Delay Time	V_{DD}=20V, I_D=85A, R_G=1.6Ω, V_{GS}=10V	-	22.5	-	ns
tr	Turn-on Rise Time		-	6.7	-	ns
td(off)	Turn-off Delay Time		-	80.3	-	ns
t_f	Turn-off Fall Time		-	26.9	-	ns
IS	Maximum Continuous Drain to Source Diode Forward Current		-	-	300	A
ISM	Maximum Pulsed Drain to Source Diode Forward Current		-	-	750	A
VSD	Drain to Source Diode Forward Voltage	V_{GS}=0V, I_S=30A	-	-	1.2	V
trr	Body Diode Reverse Recovery Time	T_J=25℃, I_F=I_S,dI/dt=100A/μs	-	100	-	ns
Q_{rr}	Body Diode Reverse Recovery Charge		-	163	-	nC

Note :

1、The data tested by surface mounted on a 1 inch 2 FR-4 board with 2OZ copper.

2、The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%

3、The EAS data shows Max. rating . The test condition is VDD =32V,VGS =10V,L=0.1mH,IAS =70A

4、The power dissipation is limited by 150℃ junction temperature

5、The data is theoretically the same as I D and I DM , in real applications , should be limited by total power dissipation.

Typical Characteristics

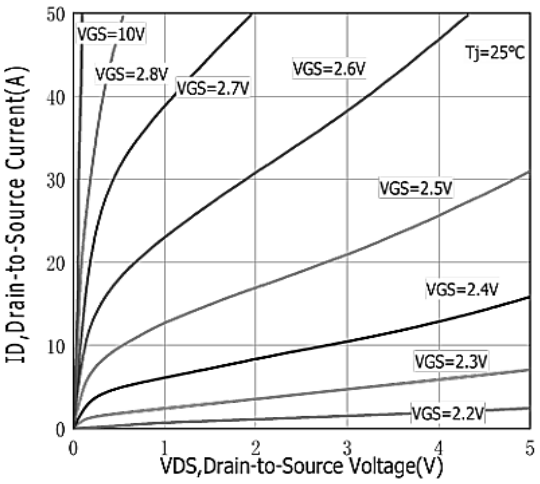


Figure.1 Typical Output Characteristics

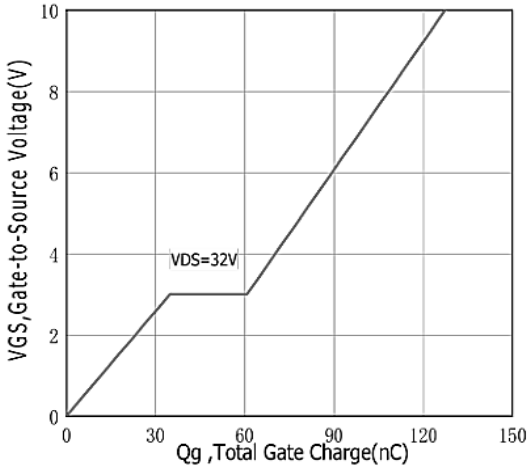


Figure.2 Typical Gate Charge vs Gate to Source Voltage

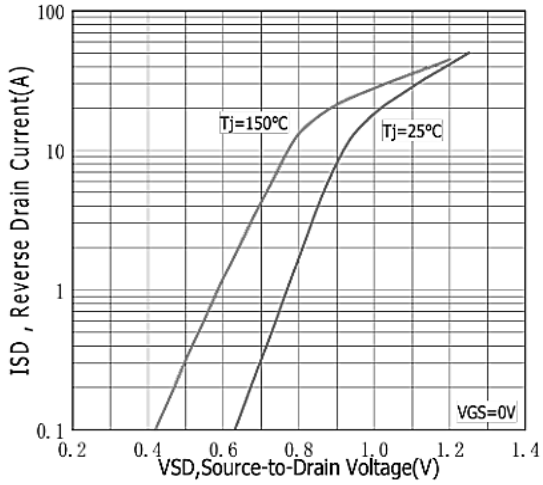


Figure.3 Typical Body Diode Transfer Characteristics

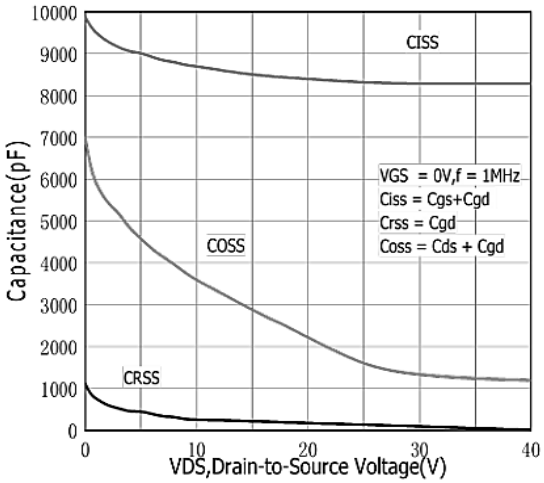


Figure 4: Body Diode Characteristics

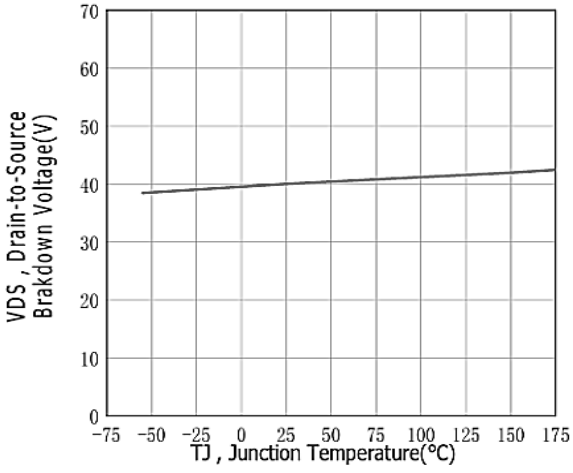


Figure.5 Typical Breakdown Voltage vs Junction Temperature

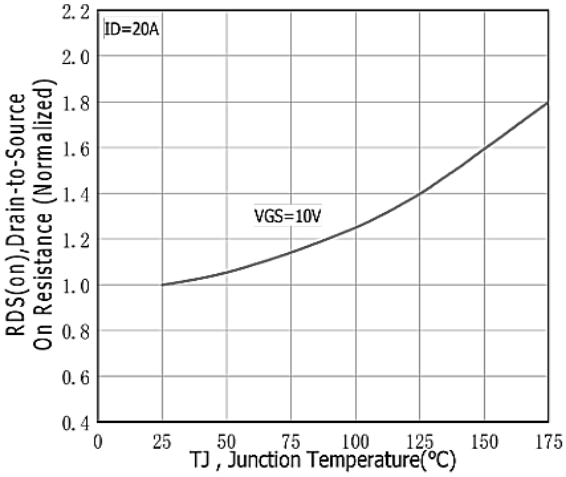


Figure 6: CapacitanceCharacteristics

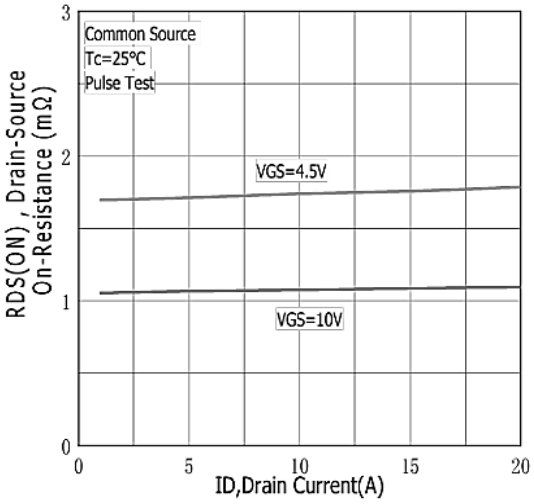


Figure.7 Typical Drain to Source ON Resistance vs Drain Current

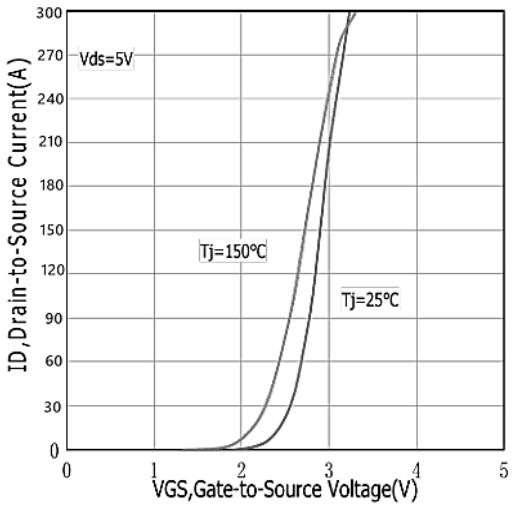


Figure.10 Typical Transfer Characteristics

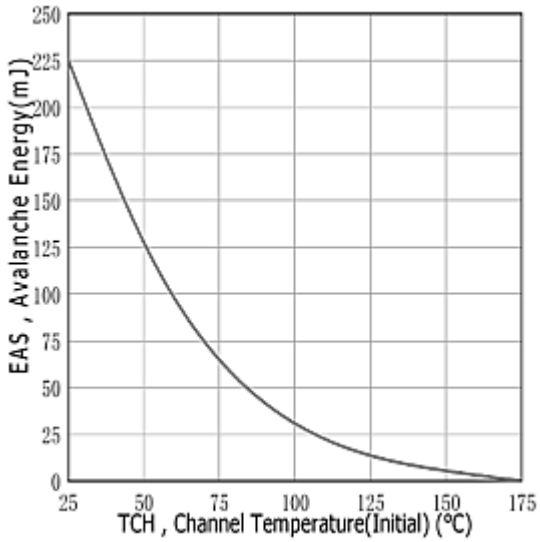


Figure.9 Maximum EAS vs Channel Temperature

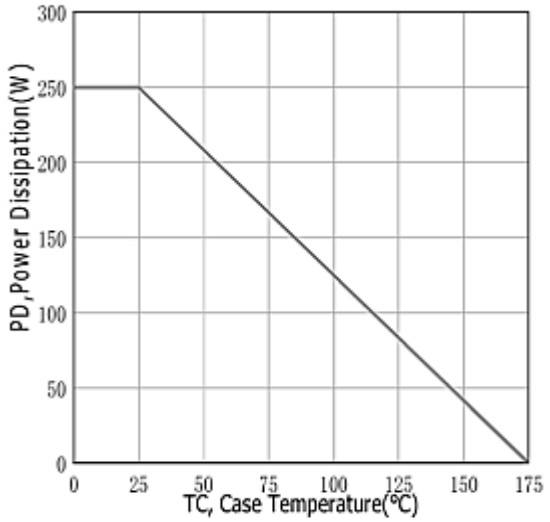


Figure.12 Maximum Power Dissipation vs Case Temperature

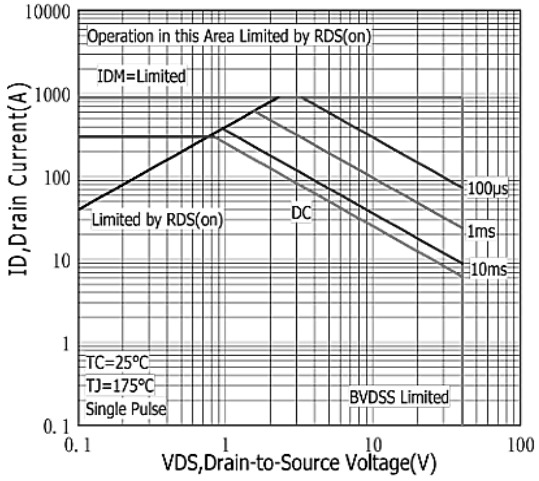


Figure 11: Maximum Safe Operating Area

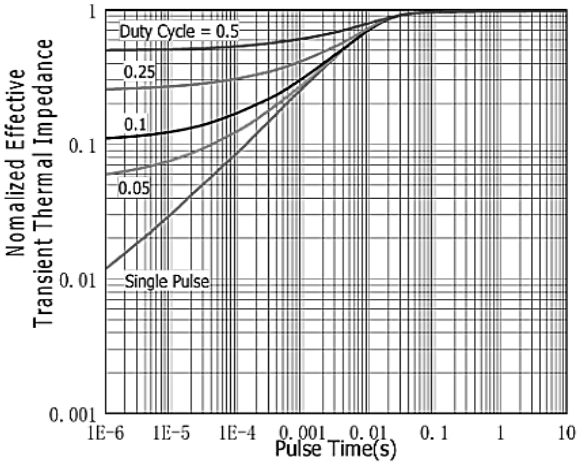
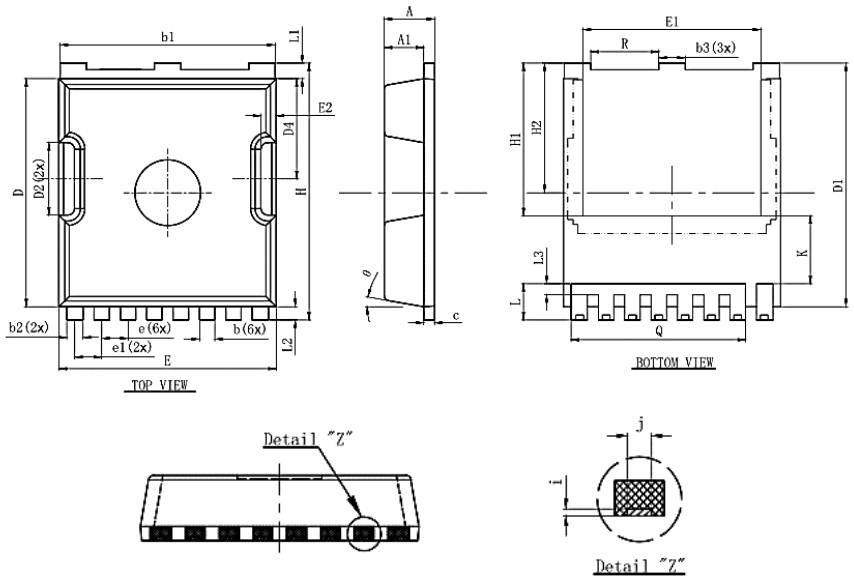


Figure.12: Maximum EffectiveTransient Thermal Impedance, Junction-to-Cas

Package Mechanical Data-TOLLA-8-XZ Single



Symbol	Dimensions In Millimeters		
	Min.	Nom	Max.
A	2.2	2.3	2.4
A1	1.7	1.8	1.9
b	0.6	0.7	0.8
b1	9.7	9.8	9.9
b2	0.65	0.75	0.85
b3	1.1	1.2	1.3
C	0.4	0.5	0.6
D	10.3	10.4	10.5
D1	11.0	11.1	11.2
D2	3.2	3.3	3.4
D4	4.47	4.57	4.67
E	9.8	9.9	10.0
E1	8.0	8.1	8.2
E2	0.5	0.6	0.7
e	1.200（BSC）		
e1	1.225（BSC）		
H	11.6	11.7	11.8
H1	6.95BSC		
H2	5.9BSC		
i	0.1REF		
j	0.350REF		
K	3.100REF		
L	1.55	1.65	1.75
L1	0.6	0.7	0.8
L2	0.5	0.6	0.7
L3	0.4	0.5	0.6
Q	7.95REF		
R	3.0	3.1	3.2
θ	10°REG		

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40V N-Channel Enhancement Mode MOSFET

Edition	Date	Change
RVE1.0	2021/12/31	Initial release