

### 150V N-Channel Enhancement Mode MOSFET

#### **Description**

The AP200N15TLG1 uses advanced APM-SGT technology to provide excellent R<sub>DS(ON)</sub>, low gate charge and operation with gate voltages as low as 10V. This device is suitable for use as a Battery protection or in other Switching application.

#### **General Features**

V<sub>DS</sub> = 150V I<sub>D</sub> =200A

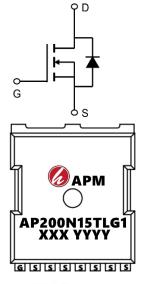
 $R_{DS(ON)} < 7.2 m\Omega$  @  $V_{GS}=10V$  (Type: 6.2 m $\Omega$ )



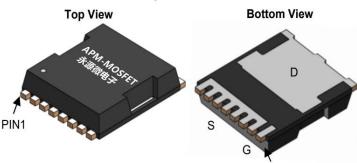
DC/DC Converter

Power Management Switches

**BMS/UPS** 







PIN1

#### **Package Marking and Ordering Information**

ackage marking and Ordering information					
Product ID	Pack	Marking	Qty(PCS)		
AP200N15TLG1	TOLLA-8L	AP200N15TLG1 XXX YYYY	300		

### Absolute Maximum Ratings (T<sub>C</sub>=25°Cunless otherwise noted)

Symbol	Parameter	Rating	Units
VDS Drain-Source Voltage		150	V
VGS Gate-Source Voltage		±20	V
I <sub>D</sub> @T <sub>C</sub> =25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	200	Α
I <sub>D</sub> @T <sub>C</sub> =100°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	140	Α
IDM	Pulsed Drain Current	550	А
EAS	Single Pulse Avalanche Energy	506	mJ
IAS	Avalanche Current	53.4	А
P <sub>D</sub> @T <sub>C</sub> =25°C	Total Power Dissipation <sup>4</sup>	210	W
TSTG	Storage Temperature Range	-55 to 150	°C
TJ	Operating Junction Temperature Range	-55 to 150	℃
R <sub>θ</sub> JA	Thermal Resistance Junction-Ambient	0.84	°C/W
R₀JC	Thermal Resistance Junction-Case	40	°C/W



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### **Electrical Characteristics (Tc=25** ℃ unless otherwise noted)

		<del>-</del>				
Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
VDSS	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250µA	150	-	-	V
IGSS	Gate-body Leakage current	V <sub>DS</sub> = 0V, V <sub>GS</sub> = ±20V	-	-	±100	nA
IDSS	Zero Gate Voltage Drain Current T <sub>J</sub> =25°C	1001/11/ 01/	-	-	1	
IDSS	Zero Gate Voltage Drain Current T <sub>J</sub> =100°C	V <sub>DS</sub> =100V, V <sub>GS</sub> = 0V	-	-	100	μA
VGS(th)	Gate-Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	2.0	2.9	4.0	V
RDS(on)	Drain-Source on-Resistance <sup>2</sup>	V <sub>GS</sub> = 10V, I <sub>D</sub> = 20A	-	6.6	7.5	mΩ
Ciss	Input Capacitance	V <sub>DS</sub> = 50V, V <sub>GS</sub> =0V, f =1MHz	-	5240	-	pF
Coss	Output Capacitance		-	412	-	
Crss	Reverse Transfer Capacitance	111112	-	10	-	
Rg	Gate Resistance	$V_{GS} = 0V$ , $V_{DS} = 0V$ , f =1MHz	-	1.7	-	Ω
Qg	Total Gate Charge		-	18	-	
Qgs	Gate-Source Charge	$V_{GS} = 10V, V_{DS} = 50V,$ $I_{D}=20A$	-	10	-	nC
Qgd	Gate-Drain Charge	15 25.1	-	72	-	
td(on)	Turn-on Delay Time	V <sub>GS</sub> =10V, V <sub>DS</sub> =50V, R <sub>G</sub> =	-	22	-	ne
t <sub>r</sub>	Rise Time		-	115	-	ns
td(off)	Turn-off Delay Time	3Ω, I <sub>D</sub> = 20A	-	44	-	
t <sub>f</sub>	Fall Time		-	105	-	
VSD	Diode Forward Voltage <sup>2</sup>	I <sub>F</sub> = 20A, V <sub>GS</sub> = 0V	-	-	1.2	V
IS	Continuous Source Current <sup>1,5</sup>	V <sub>G</sub> =V <sub>D</sub> =0V , Force Current	-	-	190	Α
trr	Body Diode Reverse Recovery Time	I <sub>F</sub> = 20A, dl/dt=100A/μs	-	45	-	ns
Qrr	Body Diode Reverse Recovery Charge	- 1- 20Λ, αι/αι-100Λ/μδ	Ī	12	-	nC

#### Notes:

- 1. The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper.
- $2\sqrt{100}$  The data tested by pulsed , pulse width  $\leq 300$ us , duty cycle  $\leq 2\%$
- 3. The EAS data shows Max. rating . The test condition is  $V_{DD}$ =50V,  $V_{GS}$ =10V, L=0.5mH,  $I_{AS}$ =45A
- 4. The power dissipation is limited by 150°C junction temperature
- 5. The data is theoretically the same as I<sub>D</sub> and I<sub>DM</sub>, in real applications, should be limited by total power dissipation.



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### **Typical Characteristics**

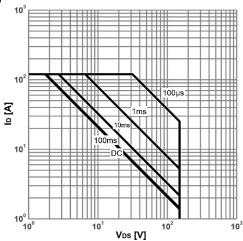


Figure 1. Power dissipation

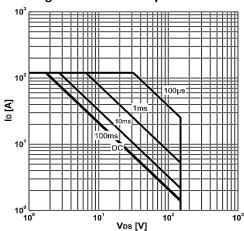


Figure 3. Safe operating area

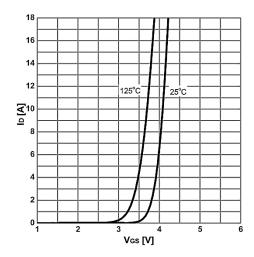


Figure 5. Typ. transfer characteristics

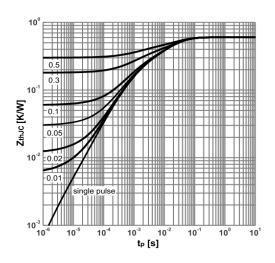


Figure 2. Max. transient thermal impedance

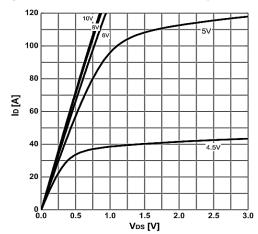


Figure 4. Typ. output characteristics

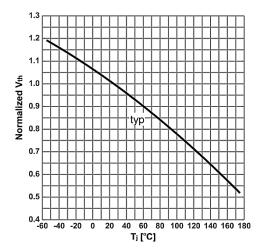


Figure 6. Gate threshold voltage vs. Junction Temperature





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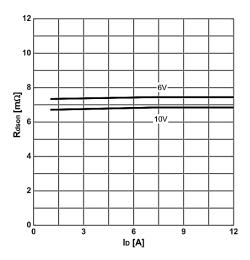


Figure 7. On-state resistance vs. Drain current

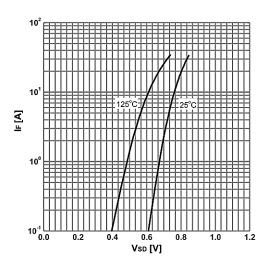


Figure 9. Forward characteristics of reverse diode

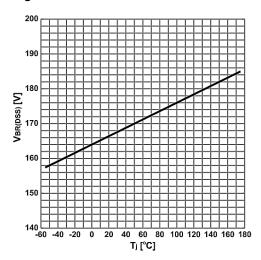


Figure 10: Breakdown Voltage Variation vs. Temperature

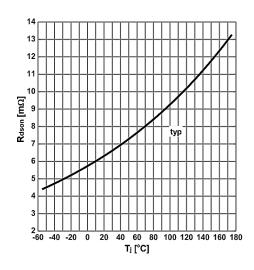


Figure 8. On-state resistance vs. Junction temperature

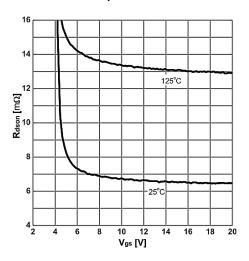


Figure 10. On-state resistance vs. Vgs characteristics

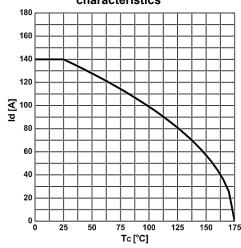


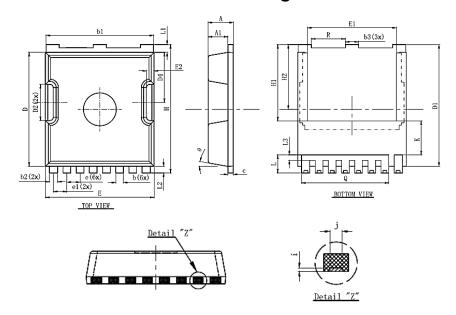
Figure 11: Maximum Drain Current

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## Package Mechanical Data-TOLLA-8-XZ Single



Symbol	Dimensions In Millimeters		
Syllibol	Min.	Nom	Max.
Α	2.2	2.3	2.4
A1	1.7	1.8	1.9
b	0.6	0.7	0.8
b1	9.7	9.8	9.9
b2	0.65	0.75	0.85
b3	1.1	1.2	1.3
С	0.4	0.5	0.6
D	10.3	10.4	10.5
D1	11.0	11.1	11.2
D2	3.2	3.3	3.4
D4	4.47	4.57	4.67
Е	9.8	9.9	10.0
E1	8.0	8.1	8.2
E2	0.5	0.6	0.7
е	1.200 (BSC)		
e1		1.225 (BSC)	
Н	11.6	11.7	11.8
H1	6.95BSC		
H2	5.9BSC		
i	0.1REF		
j	0.350REF		
K	3.100REF		
L	1.55	1.65	1.75
L1	0.6	0.7	0.8
L2	0.5	0.6	0.7
L3	0.4	0.5	0.6
Q	7.95REF		
R	3.0	3.1	3.2
θ	10°REG		



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### **150V N-Channel Enhancement Mode MOSFET**

Edition	Date	Change
Rve1.0	2021/8/5	Initial release

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