

100V N-Channel Enhancement Mode MOSFET

Description

The AP180N10MP uses advanced **APM-SGT₁₁** technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 10V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

$V_{DS} = 100V$ $I_D = 180A$

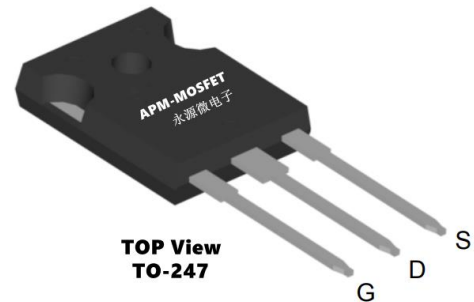
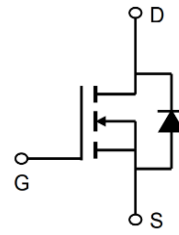
$R_{DS(ON)} < 6.0m\Omega$ @ $V_{GS}=10V$ (Type: **5.0mΩ**)

Application

DC/DC Converter

LED Backlighting

Power Management Switches



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP180N10MP	TO-247-3L	AP180N10P XXX YYYY	300

Absolute Maximum Ratings ($T_C=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	100	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_C=25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V$	180	A
$I_D@T_C=100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V$	120	A
IDM	Pulsed Drain Current	420	A
EAS	Single Pulse Avalanche Energy	250	mJ
IAS	Avalanche Current	53.4	A
$P_D@T_C=25^\circ\text{C}$	Total Power Dissipation ⁴	148	W
TSTG	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient	0.84	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance Junction-Case	62	$^\circ\text{C/W}$

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Electrical Characteristics (T_c=25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VDSS	Drain-Source Breakdown Voltage	V _{GS} = 0V, I _D = 250μA	100	-	-	V
IGSS	Gate-body Leakage current	V _{DS} = 0V, V _{GS} = ±20V	-	-	±100	nA
IDSS	Zero Gate Voltage Drain Current T _J =25°C	V _{DS} = 100V, V _{GS} = 0V	-	-	1	μA
IDSS	Zero Gate Voltage Drain Current T _J =100°C		-	-	100	
VGS(th)	Gate-Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	2.0	2.9	4.0	V
RDS(on)	Drain-Source on-Resistance ²	V _{GS} = 10V, I _D = 20A	-	5.0	6	mΩ
Ciss	Input Capacitance	V _{DS} = 50V, V _{GS} = 0V, f = 1MHz	-	4400	-	pF
Coss	Output Capacitance		-	645	-	
Crss	Reverse Transfer Capacitance		-	20	-	
R _g	Gate Resistance	V _{GS} = 0V, V _{DS} = 0V, f = 1MHz	-	1.7	-	Ω
Q _g	Total Gate Charge	V _{GS} = 10V, V _{DS} = 50V, I _D = 20A	-	75	-	nC
Q _{gs}	Gate-Source Charge		-	17	-	
Q _{gd}	Gate-Drain Charge		-	13	-	
td(on)	Turn-on Delay Time	V _{GS} = 10V, V _{DS} = 50V, R _G = 3Ω, I _D = 20A	-	15.4	-	ns
t _r	Rise Time		-	13	-	
td(off)	Turn-off Delay Time		-	34	-	
t _f	Fall Time		-	6.2	-	
VSD	Diode Forward Voltage ²	I _F = 20A, V _{GS} = 0V	-	-	1.2	V
IS	Continuous Source Current ^{1,5}	V _G =V _D =0V, Force Current	-	-	95	A
trr	Body Diode Reverse Recovery Time	I _F = 20A, di/dt=100A/μs	-	55	-	ns
Q _{rr}	Body Diode Reverse Recovery Charge		-	101	-	nC

Notes:

- 1、 The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2、 The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%
- 3、 The EAS data shows Max. rating . The test condition is V_{DD}=50V, V_{GS}=10V, L=0.4mH, I_{AS}=32A
- 4、 The power dissipation is limited by 150°C junction temperature
- 5、 The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

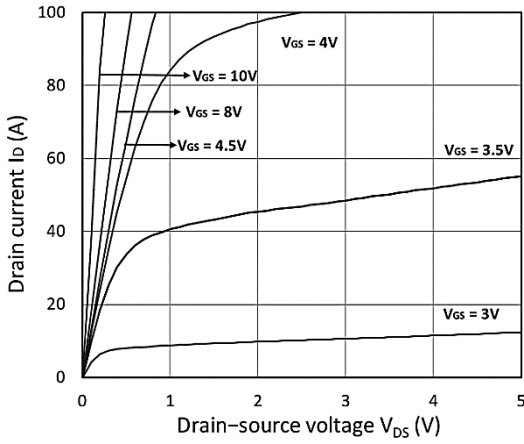


Figure 1. Output Characteristics

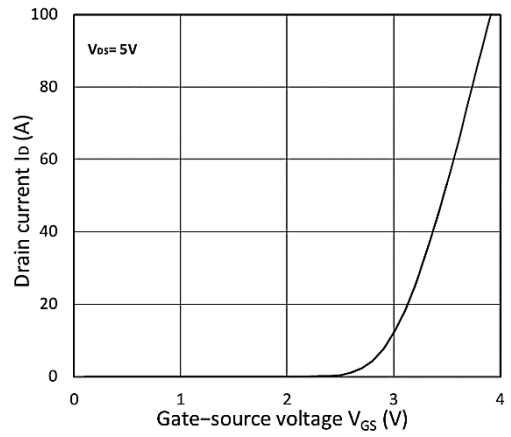


Figure 2. Transfer Characteristics

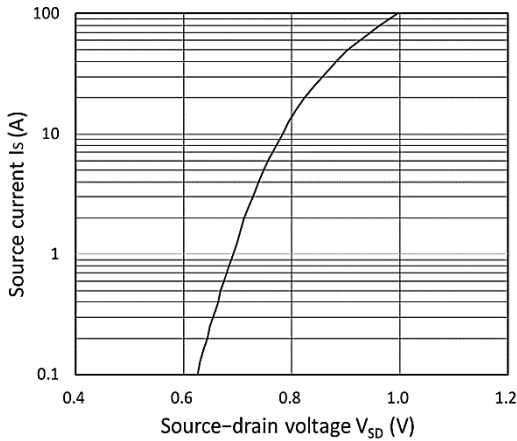


Figure 3. Forward Characteristics of Reverse

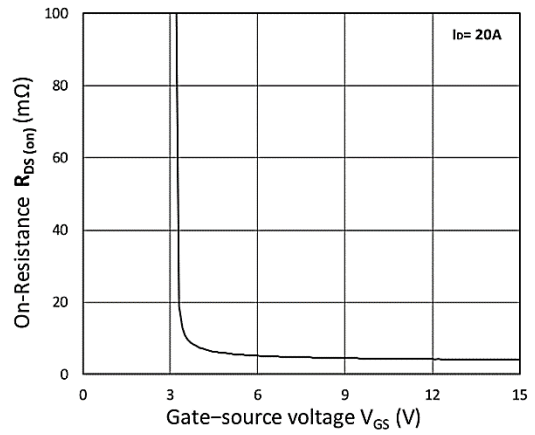


Figure 4. $R_{DS(ON)}$ vs. V_{GS}

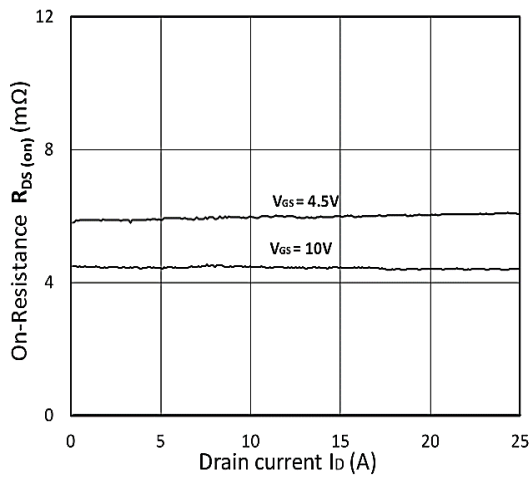


Figure 5. $R_{DS(ON)}$ vs. I_D

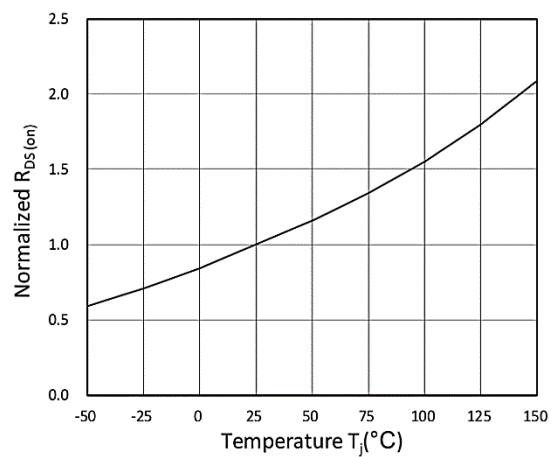


Figure 6. Normalized $R_{DS(on)}$ vs. Temperature

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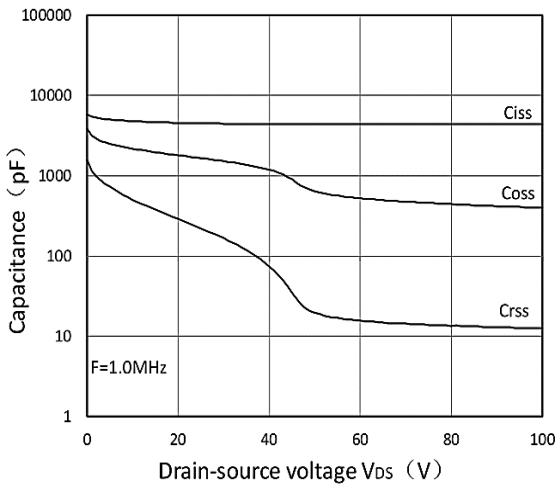


Figure 7. Capacitance Characteristics

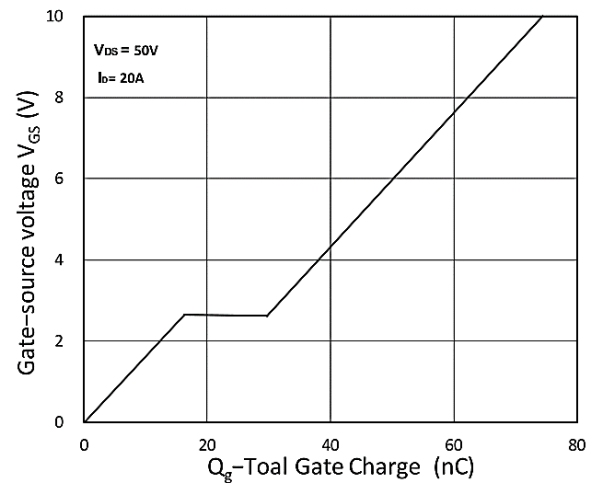


Figure 8. Gate Charge Characteristics

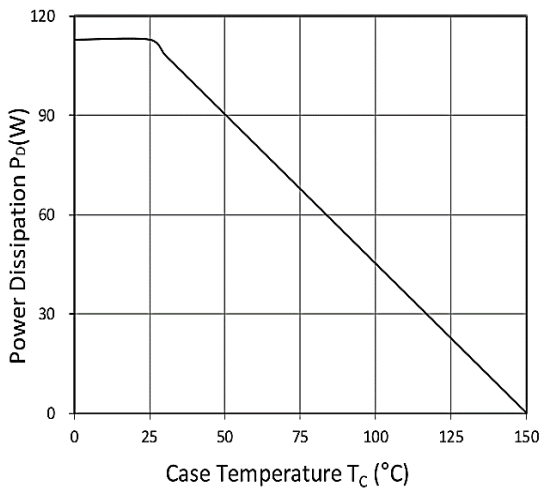


Figure 9. Power Dissipation

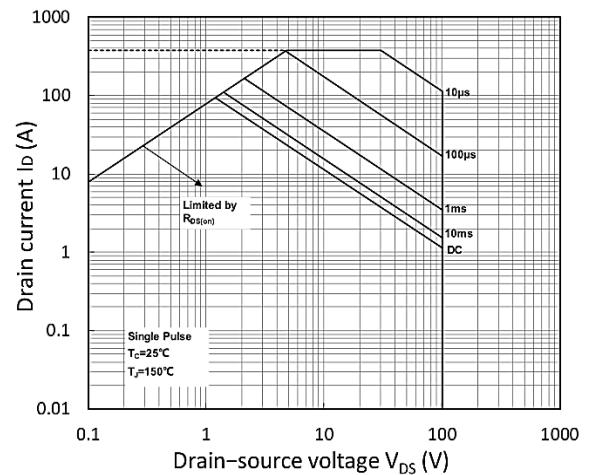


Figure 10. Safe Operating Area

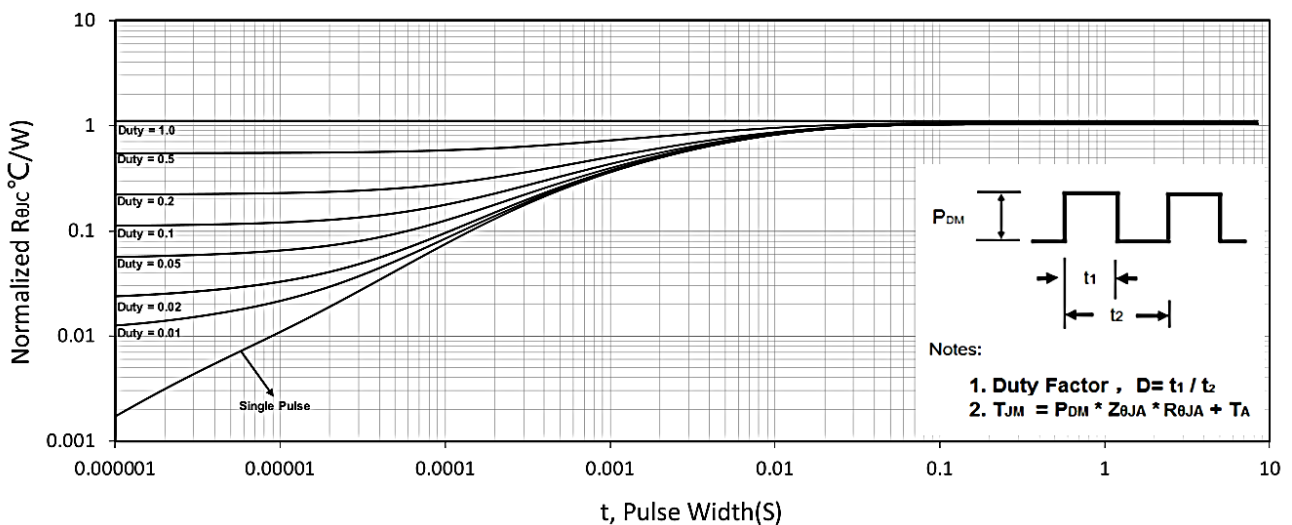
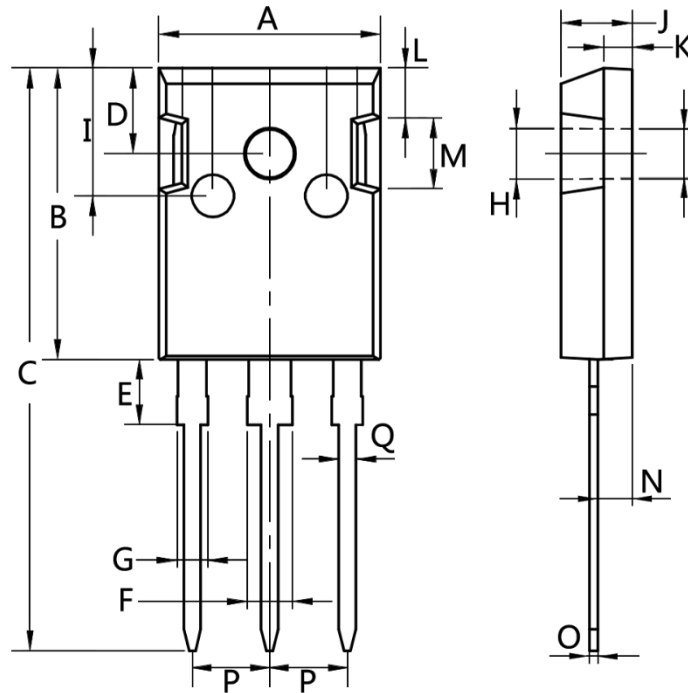


Figure 11. Normalized Maximum Transient Thermal Impedance

Package Mechanical Data-TO-247-3L



Dim.	Min.	Max.
A	15.0	16.0
B	20.0	21.0
C	41.0	42.0
D	5.0	6.0
E	4.0	5.0
F	2.5	3.5
G	1.75	2.5
H	3.0	3.5
I	8.0	10.0
J	4.9	5.1
K	1.9	2.1
L	3.5	4.0
M	4.75	5.25
N	2.0	3.0
O	0.55	0.75
P	Typ 5.08	
Q	1.2	1.3

100V N-Channel Enhancement Mode MOSFET**Attention**

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Edition	Date	Change
Rve1.0	2021/8/5	Initial release

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