

## 400V N-Channel Enhancement Mode MOSFET

### Description

The AP12N40F/P is silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency.

### General Features

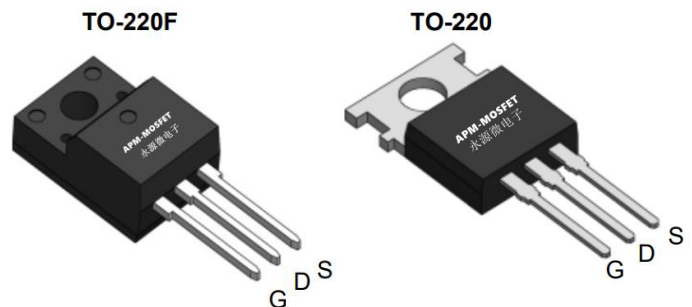
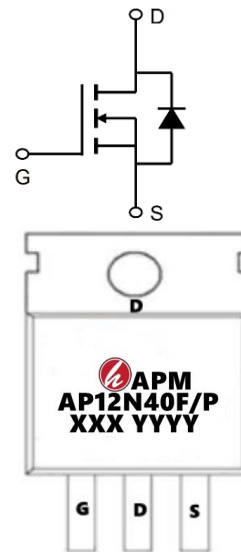
$V_{DS} = 400V$   $I_D = 12A$

$R_{DS(ON)} < 500m\Omega$  @  $V_{GS}=10V$  (Type: 430m $\Omega$ )

### Application

Uninterruptible Power Supply(UPS)

Power Factor Correction (PFC)



### Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP12N40F	TO-220F-3L	AP12N40F XXX YYYY	1000
AP12N40P	TO-220-3L	AP12N40P XXX YYYY	1000

### Absolute Maximum Ratings ( $T_C=25^{\circ}C$ unless otherwise noted)

Symbol	Parameter	Value		Unit
		TO-220F	TO-220	
$V_{DS}$	Drain-Source Voltage ( $V_{GS} = 0V$ )	400		V
$I_D$	Continuous Drain Current	12		A
$I_{DM}$	Pulsed Drain Current (note1)	44		A
$V_{GS}$	Gate-Source Voltage	$\pm 30$		V
$E_{AS}$	Single Pulse Avalanche Energy (note2)	368		mJ
$I_{AR}$	Avalanche Current (note1)	11		A
$E_{AR}$	Repetitive Avalanche Energy note1)	28		mJ
$P_D$	Power Dissipation ( $T_C = 25^{\circ}C$ )	33.2		W
$T_J, T_{stg}$	Operating Junction and Storage Temperature Range	-55~+150		$^{\circ}C$
$R_{thJC}$	Thermal Resistance, Junction-to-Case	3.8		$^{\circ}C/W$
$R_{thJA}$	Thermal Resistance, Junction-to-Ambient	62.5		$^{\circ}C/W$

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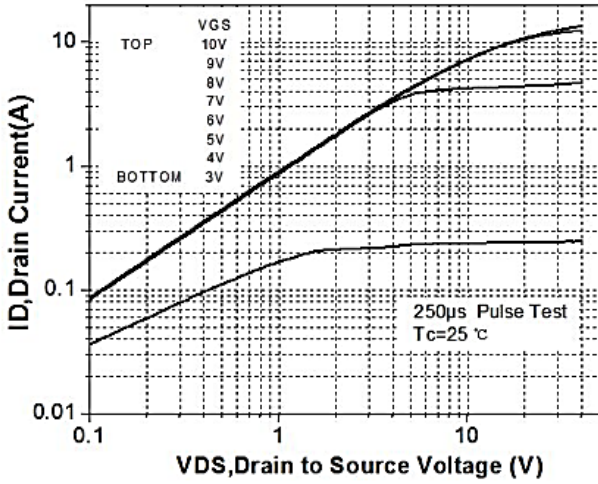
### Electrical Characteristics (T<sub>J</sub>=25°C, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	400	450		V
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> =250μA, Referenced to 25°C		0.43		V/°C
IDSS	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 400 V, V <sub>GS</sub> = 0 V			1	μA
		V <sub>DS</sub> = 320 V, TC = 125°C			10	μA
IGSSF	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 30 V, V <sub>DS</sub> = 0 V			100	nA
IGSSR	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -30 V, V <sub>DS</sub> = 0 V			-100	nA
VGS(TH)	Gate Threshold voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250 uA	2.0		4.0	V
RDS(On)	Drain-Source on-state resistance	V <sub>GS</sub> =10V, I <sub>D</sub> = 5.5A, T <sub>J</sub> =25°C		0.460	0.575	Ω
gFS	Forward Transconductance	V <sub>DS</sub> =40V, I <sub>D</sub> = 5.5A (Note 4)		6.5		S
C <sub>iss</sub>	Input capacitance	V <sub>DS</sub> = 25V, V <sub>GS</sub> =0V, f=1.0MHz		755		pF
C <sub>oss</sub>	Output capacitance			132		pF
C <sub>rss</sub>	Reverse transfer capacitance			9.0		pF
td(on)	Turn On Delay Time	V <sub>DD</sub> =200 V, I <sub>D</sub> =11A, R <sub>G</sub> = 25Ω (Note 4, 5)		11		ns
t <sub>r</sub>	Rising Time			25		ns
td(off)	Turn Off Delay Time			28		ns
t <sub>f</sub>	Fall Time			26		ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = 320 V, I <sub>D</sub> = 11 A, V <sub>GS</sub> = 10 V (Note 4, 5)		9.6		nC
Q <sub>gs</sub>	Gate-Source Charge			3.0		nC
Q <sub>gd</sub>	Gate-Drain Charge			2.5		nC
ISM	Maximum Pulsed Drain-Source Diode Forward Current				44	A
V <sub>SD</sub>	Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 11 A			1.2	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 11 A, dI <sub>F</sub> / dt = 100 A/μs Note 4)		356		ns
Q <sub>rr</sub>	Reverse Recovery Charge			2.4		μC

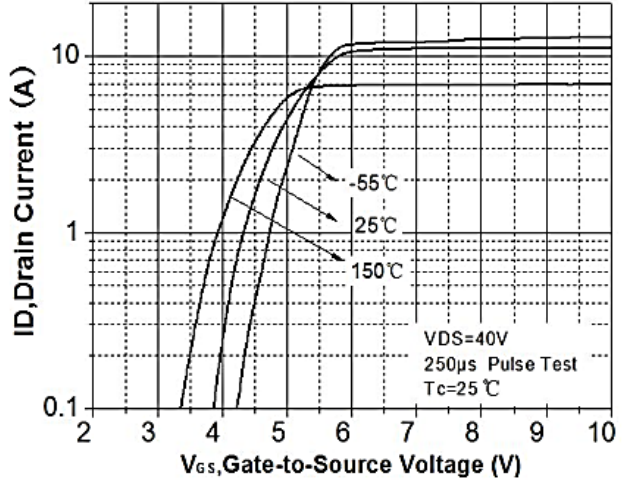
#### Note :

- 1、 The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2、 The EAS data shows Max. rating . L=4.1Mh IAS=11A, VDD=50V, RG=25Ω, Starting T<sub>J</sub> = 25 °C
- 3、 The test condition is Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 1%
- 4、 The power dissipation is limited by 150°C junction temperature
- 5、 The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

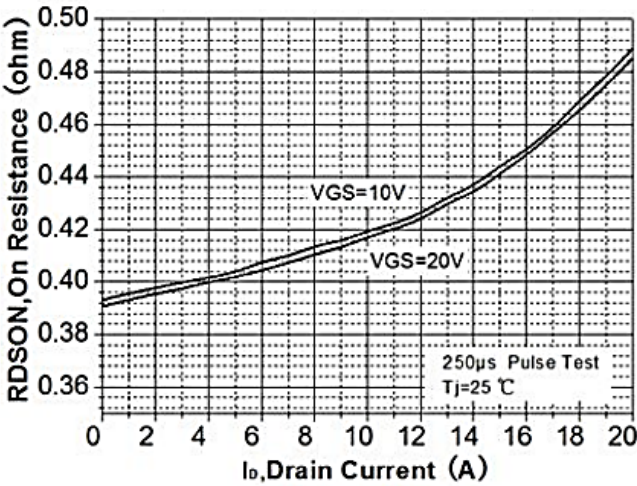
**Typical Characteristics**



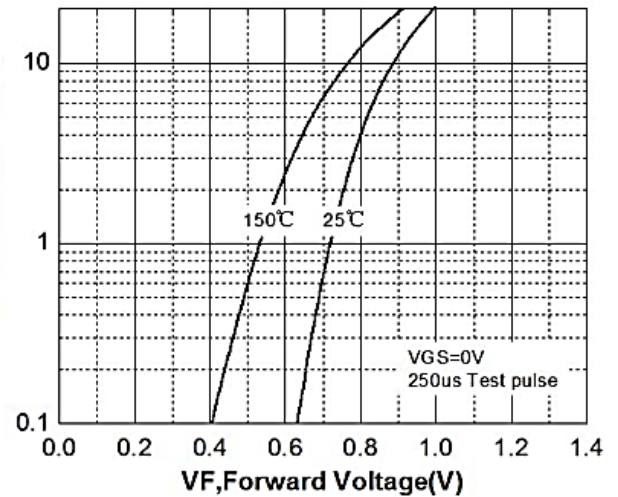
**Figure 1. On-Region Characteristics**



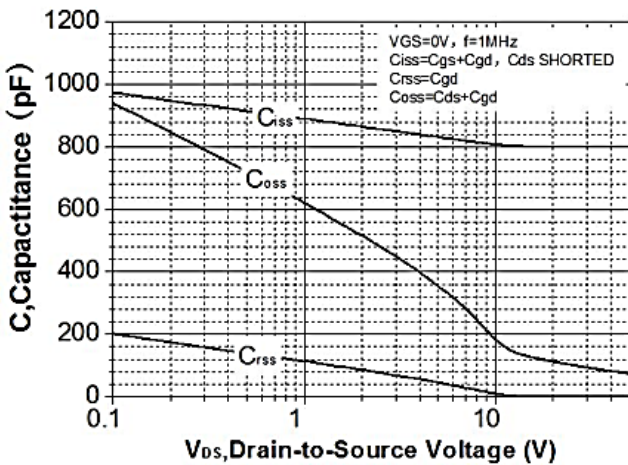
**Figure 2. Transfer Characteristics**



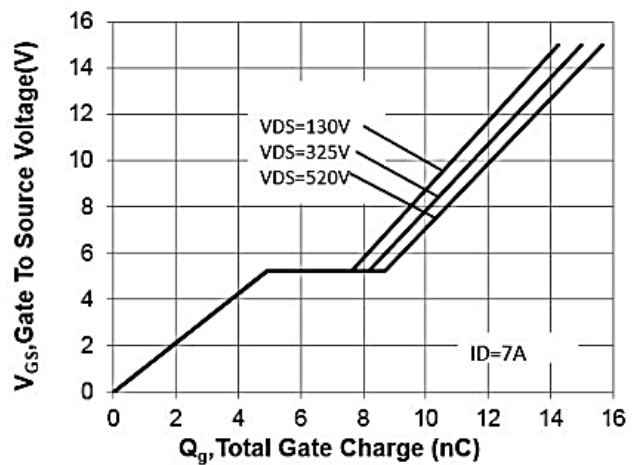
**Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage**



**Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature**



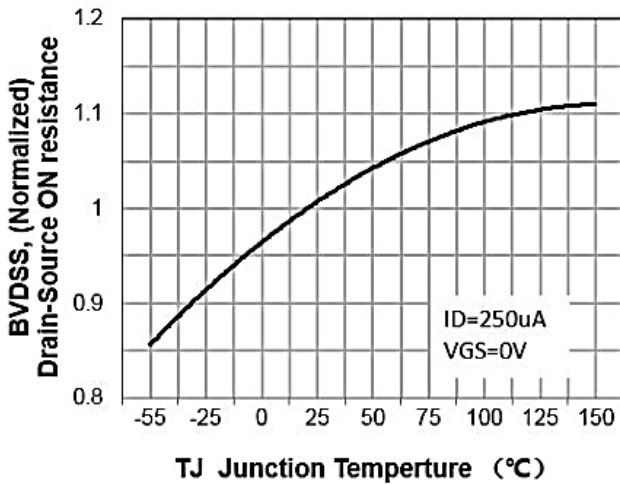
**Figure 5. Capacitance Characteristics**



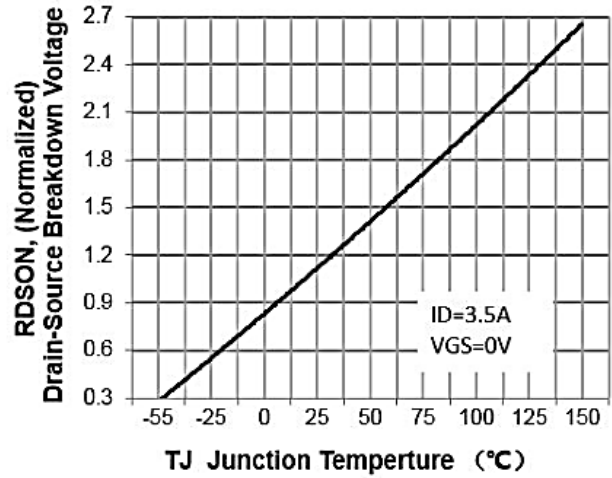
**Figure 6. Gate Charge Characteristics**



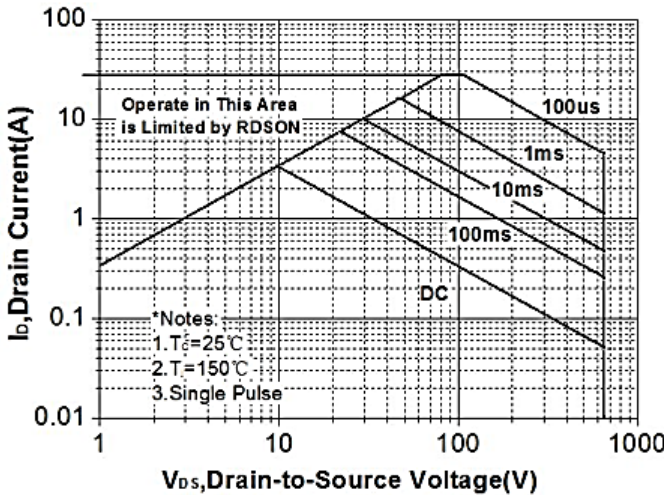
**400V N-Channel Enhancement Mode MOSFET**



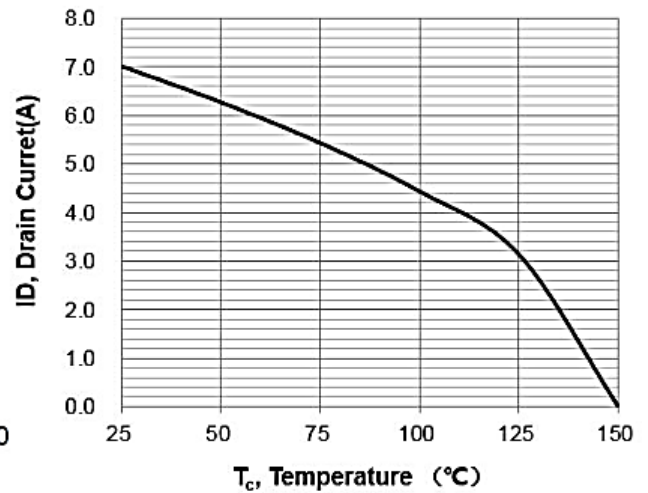
**Figure 7. Breakdown Voltage Variation vs Temperature**



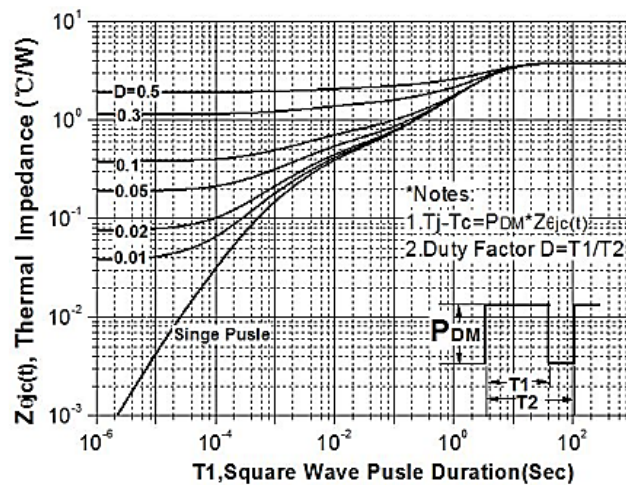
**Figure 8. On-Resistance Variation vs Temperature**



**Figure 9. Maximum Safe Operating Area**



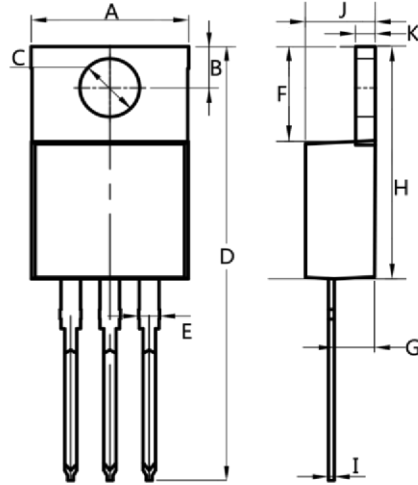
**Figure 10. Maximum Drain Current vs Case Temperature**



**Figure 11. Transient Thermal Response Curve**

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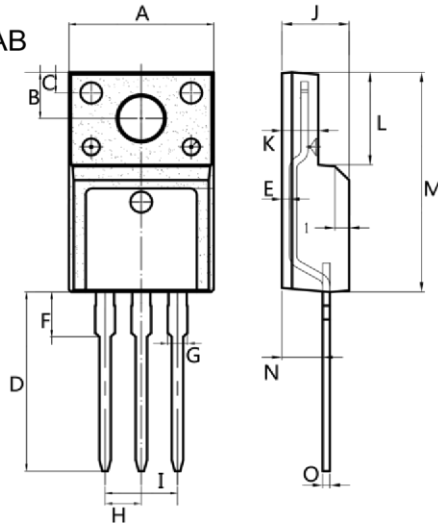
TO-220AB



Dim.	Min.	Max.
A	10.0	10.4
B	2.5	3.0
C	3.5	4.0
D	28.0	30.0
E	1.1	1.5
F	6.2	6.6
G	2.9	3.3
H	15.0	16.0
I	0.35	0.45
J	4.3	4.7
K	1.2	1.4

All Dimensions in millimeter

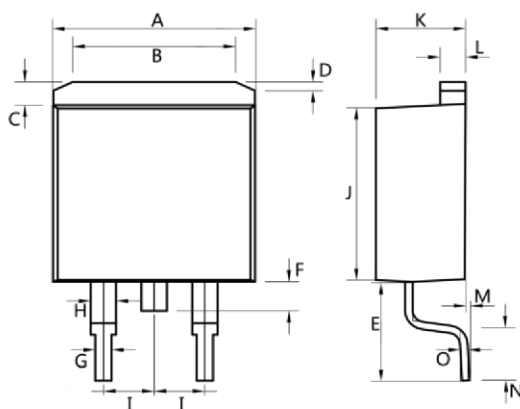
ITO-220AB



Dim.	Min.	Max.
A	9.9	10.3
B	2.9	3.5
C	1.15	1.45
D	12.75	13.25
E	0.55	0.75
F	3.1	3.5
G	1.25	1.45
H	Typ 2.54	
I	Typ 5.08	
J	4.55	4.75
K	2.4	2.7
L	6.35	6.75
M	15.0	16.0
N	2.75	3.15
O	0.45	0.60

All Dimensions in millimeter

TO-263



Dim.	Min.	Max.
A	10.0	10.5
B	7.25	7.75
C	1.3	1.5
D	0.55	0.75
E	5.0	6.0
F	1.4	1.6
G	0.75	0.95
H	1.15	1.35
I	Typ 2.54	
J	8.4	8.6
K	4.4	4.6
L	1.25	1.45
M	0.02	0.1
N	2.4	2.8
O	0.35	0.45

All Dimensions in millimeter

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Edition	Date	Change
Rve1.0	2020/1/31	Initial release

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