

MOSFET

OptiMOS™ 5 Power-Transistor, 100 V

Features

- Optimized for high performance SMPS, e.g. sync. Rec.
- 100% avalanche tested
- Superior thermal resistance
- N-channel, logic level
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

Product validation

Qualified according to JEDEC Standard

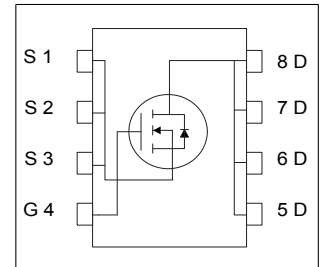
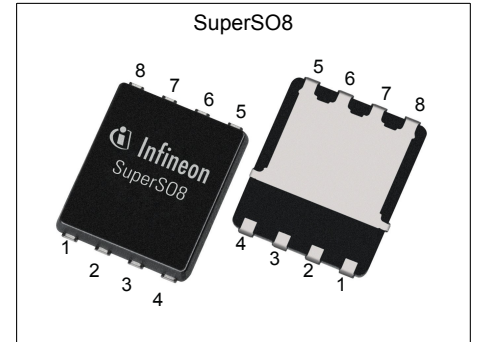


Table 1 Key Performance Parameters

| Parameter | Value | Unit |
|------------------|-------|------|
| V_{DS} | 100 | V |
| $R_{DS(on),max}$ | 3.4 | mΩ |
| I_D | 100 | A |
| Q_{oss} | 91 | nC |
| $Q_G(0V..4.5V)$ | 37 | nC |

| Type / Ordering Code | Package | Marking | Related Links |
|----------------------|------------|---------|---------------|
| BSC0802LS | PG-TDSON-8 | 0802LS | - |

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1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|----------------|--------|------|-----------------|------|---|
| | | Min. | Typ. | Max. | | |
| Continuous drain current | I_D | - | - | 100 99 20 | A | $V_{GS}=10\text{ V}$, $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=10\text{ V}$, $T_A=25\text{ °C}$, $R_{THJA}=50\text{ °C/W}^{(1)}$ |
| Pulsed drain current ²⁾ | $I_{D,pulse}$ | - | - | 400 | A | $T_A=25\text{ °C}$ |
| Avalanche energy, single pulse ³⁾ | E_{AS} | - | - | 301 | mJ | $I_D=50\text{ A}$, $R_{GS}=25\text{ }\Omega$ |
| Gate source voltage | V_{GS} | -20 | - | 20 | V | - |
| Power dissipation | P_{tot} | - | - | 156 2.5 | W | $T_C=25\text{ °C}$ $T_A=25\text{ °C}$, $R_{THJA}=50\text{ °C/W}^{(2)}$ |
| Operating and storage temperature | T_j, T_{stg} | -55 | - | 150 | °C | IEC climatic category; DIN IEC 68-1: 55/150/56 |

2 Thermal characteristics

Table 3 Thermal characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|------------|--------|------|------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| Thermal resistance, junction - case | R_{thJC} | - | 0.5 | 0.8 | °C/W | - |
| Device on PCB, 6 cm ² cooling area ¹⁾ | R_{thJA} | - | - | 50 | °C/W | - |

¹⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

²⁾ See Diagram 3 for more detailed information

³⁾ See Diagram 13 for more detailed information

3 Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 4 Static characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|----------------------------------|---------------|--------|------------|------------|------------------|---|
| | | Min. | Typ. | Max. | | |
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | 100 | - | - | V | $V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$ |
| Gate threshold voltage | $V_{GS(th)}$ | 1.1 | 1.7 | 2.3 | V | $V_{DS}=V_{GS}$, $I_D=115\text{ }\mu\text{A}$ |
| Zero gate voltage drain current | I_{DSS} | - | 0.1 10 | 1 100 | μA | $V_{DS}=100\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$ $V_{DS}=100\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$ |
| Gate-source leakage current | I_{GSS} | - | 10 | 100 | nA | $V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$ |
| Drain-source on-state resistance | $R_{DS(on)}$ | - | 2.8 3.5 | 3.4 4.6 | $\text{m}\Omega$ | $V_{GS}=10\text{ V}$, $I_D=50\text{ A}$ $V_{GS}=4.5\text{ V}$, $I_D=25\text{ A}$ |
| Gate resistance ¹⁾ | R_G | - | 1.5 | 2.3 | Ω | - |
| Transconductance | g_{fs} | 60 | 120 | - | S | $ V_{DS} \geq 2 I_D /R_{DS(on)max}$, $I_D=50\text{ A}$ |

Table 5 Dynamic characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|--------------|--------|------|------|------|--|
| | | Min. | Typ. | Max. | | |
| Input capacitance ¹⁾ | C_{iss} | - | 5000 | 6500 | pF | $V_{GS}=0\text{ V}$, $V_{DS}=50\text{ V}$, $f=1\text{ MHz}$ |
| Output capacitance ¹⁾ | C_{oss} | - | 770 | 1000 | pF | $V_{GS}=0\text{ V}$, $V_{DS}=50\text{ V}$, $f=1\text{ MHz}$ |
| Reverse transfer capacitance ¹⁾ | C_{rss} | - | 34 | 60 | pF | $V_{GS}=0\text{ V}$, $V_{DS}=50\text{ V}$, $f=1\text{ MHz}$ |
| Turn-on delay time | $t_{d(on)}$ | - | 9.6 | - | ns | $V_{DD}=50\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=50\text{ A}$, $R_{G,ext}=3\text{ }\Omega$ |
| Rise time | t_r | - | 10 | - | ns | $V_{DD}=50\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=50\text{ A}$, $R_{G,ext}=3\text{ }\Omega$ |
| Turn-off delay time | $t_{d(off)}$ | - | 40 | - | ns | $V_{DD}=50\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=50\text{ A}$, $R_{G,ext}=3\text{ }\Omega$ |
| Fall time | t_f | - | 16.0 | - | ns | $V_{DD}=50\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=50\text{ A}$, $R_{G,ext}=3\text{ }\Omega$ |

Table 6 Gate charge characteristics²⁾

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|------------------------------------|---------------|--------|------|------|------|--|
| | | Min. | Typ. | Max. | | |
| Gate to source charge | Q_{gs} | - | 14 | - | nC | $V_{DD}=50\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$ |
| Gate charge at threshold | $Q_{g(th)}$ | - | 8 | - | nC | $V_{DD}=50\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$ |
| Gate to drain charge ¹⁾ | Q_{gd} | - | 13 | 19 | nC | $V_{DD}=50\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$ |
| Switching charge | Q_{sw} | - | 18 | - | nC | $V_{DD}=50\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$ |
| Gate charge total ¹⁾ | Q_g | - | 37 | 46 | nC | $V_{DD}=50\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$ |
| Gate plateau voltage | $V_{plateau}$ | - | 2.9 | - | V | $V_{DD}=50\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$ |
| Gate charge total, sync. FET | $Q_{g(sync)}$ | - | 61 | - | nC | $V_{DS}=0.1\text{ V}$, $V_{GS}=0\text{ to }10\text{ V}$ |
| Output charge ¹⁾ | Q_{oss} | - | 91 | 121 | nC | $V_{DS}=50\text{ V}$, $V_{GS}=0\text{ V}$ |

¹⁾ Defined by design. Not subject to production test.

²⁾ See "Gate charge waveforms" for parameter definition

Table 7 Reverse diode

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---------------------------------------|---------------|--------|------|------|------|--|
| | | Min. | Typ. | Max. | | |
| Diode continuous forward current | I_S | - | - | 100 | A | $T_C=25\text{ °C}$ |
| Diode pulse current | $I_{S,pulse}$ | - | - | 400 | A | $T_C=25\text{ °C}$ |
| Diode forward voltage | V_{SD} | - | 0.9 | 1.1 | V | $V_{GS}=0\text{ V}, I_F=50\text{ A}, T_j=25\text{ °C}$ |
| Reverse recovery time ¹⁾ | t_{rr} | - | 40 | 80 | ns | $V_R=50\text{ V}, I_F=50\text{ A}, di_F/dt=100\text{ A}/\mu\text{s}$ |
| Reverse recovery charge ¹⁾ | Q_{rr} | - | 42 | 84 | nC | $V_R=50\text{ V}, I_F=50\text{ A}, di_F/dt=100\text{ A}/\mu\text{s}$ |

¹⁾ Defined by design. Not subject to production test.

4 Electrical characteristics diagrams

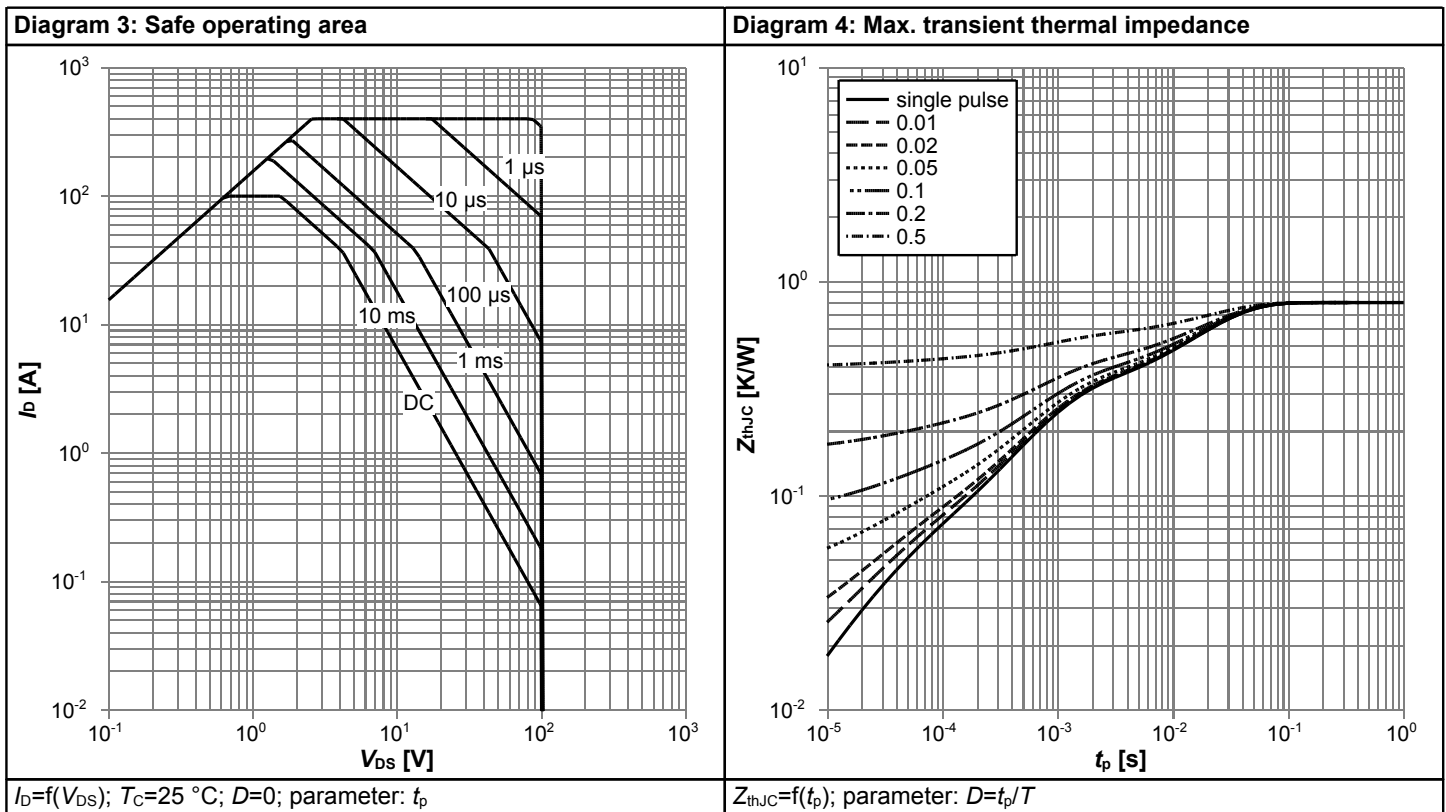
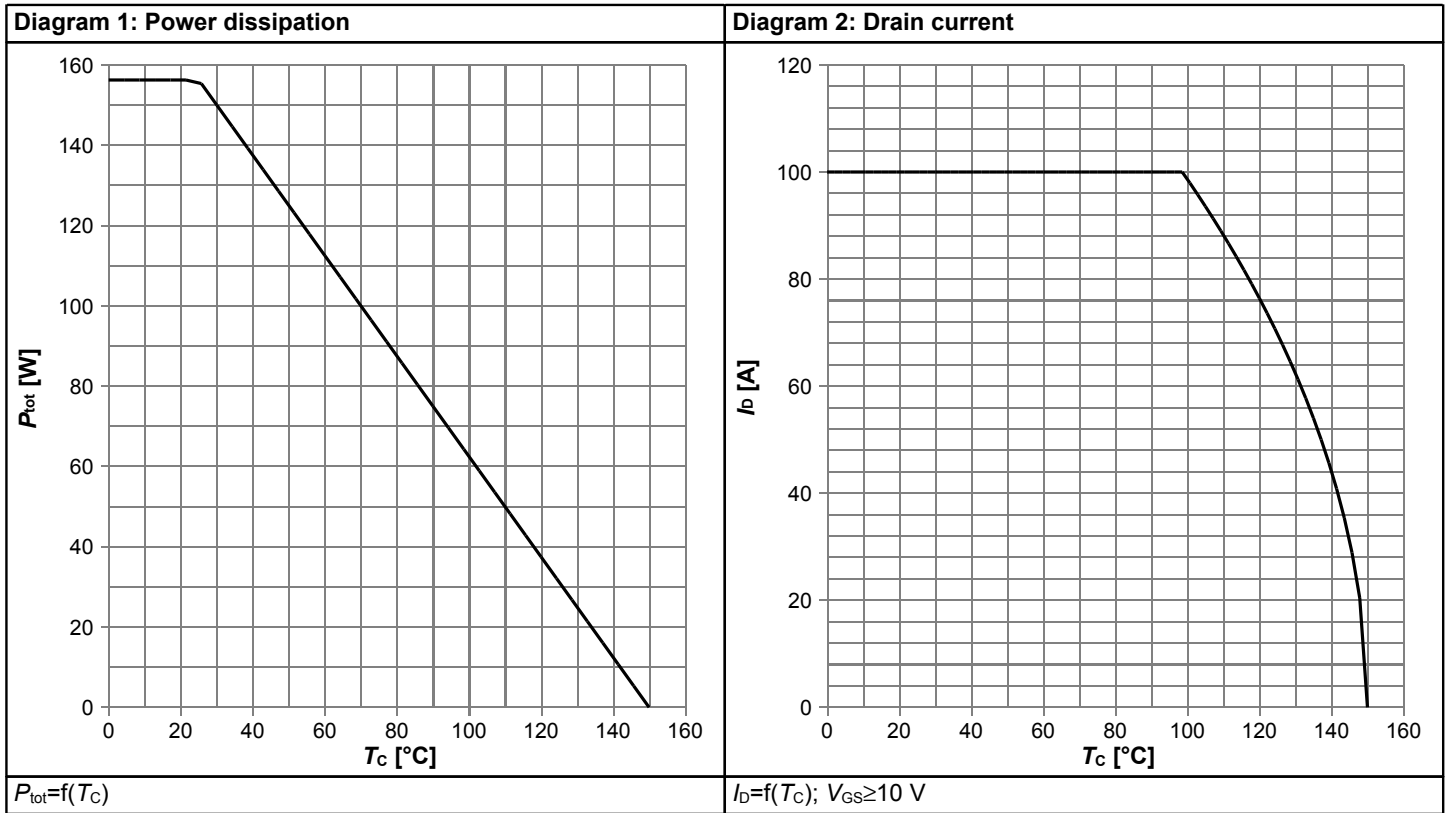
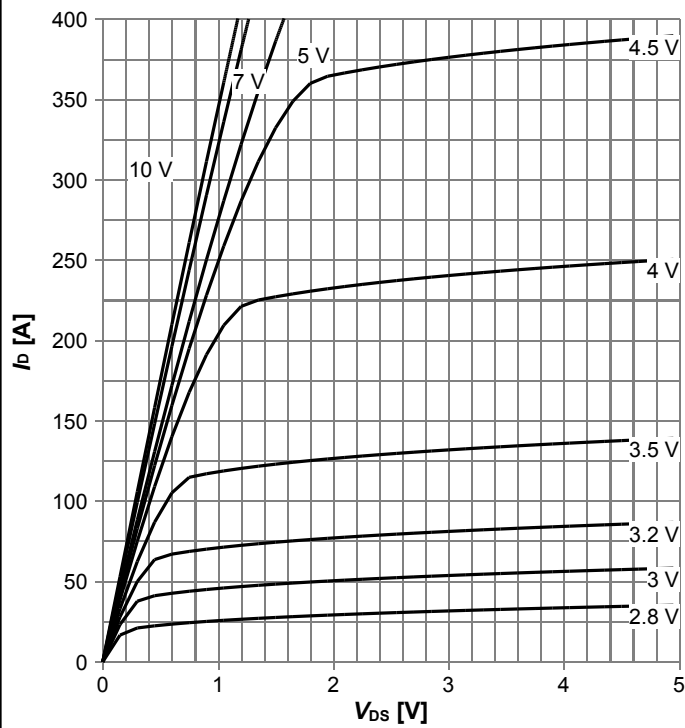
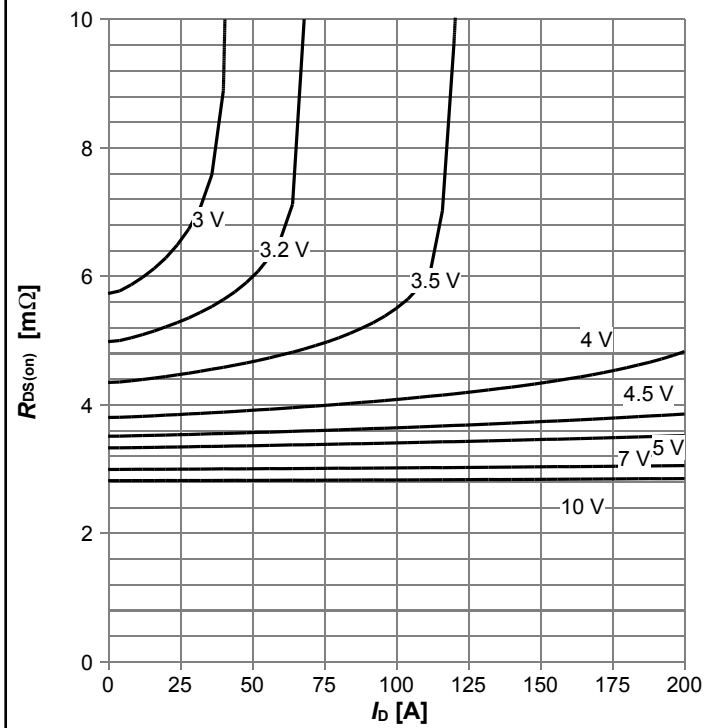


Diagram 5: Typ. output characteristics



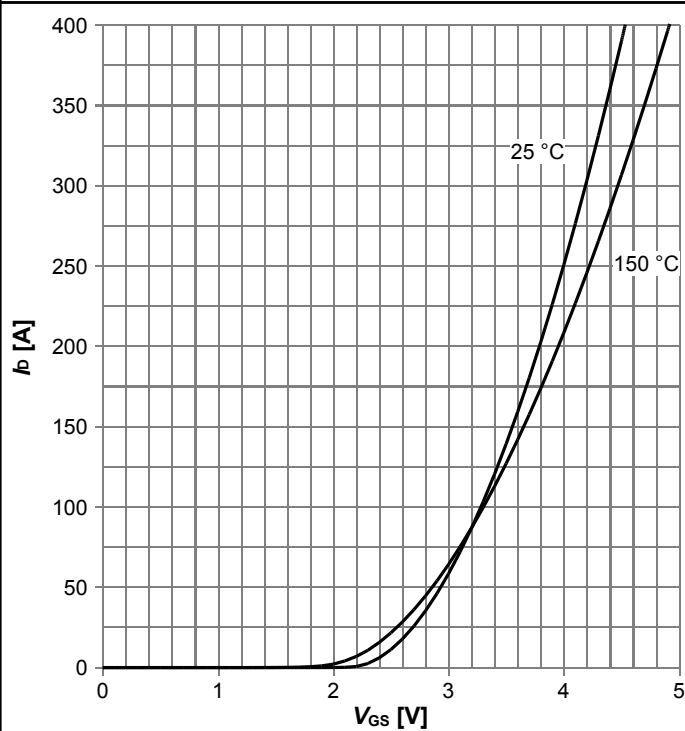
$I_D = f(V_{DS})$, $T_j = 25\text{ °C}$; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



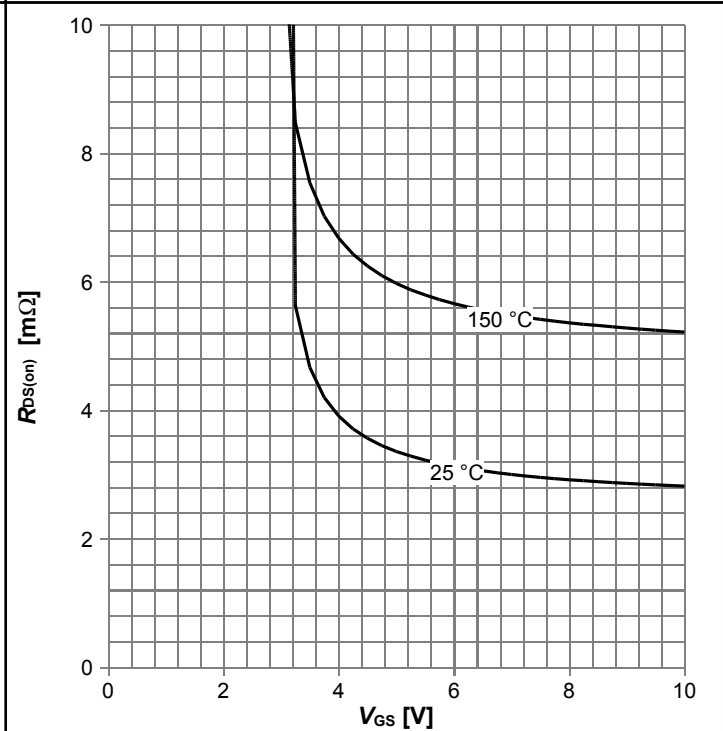
$R_{DS(on)} = f(I_D)$, $T_j = 25\text{ °C}$; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



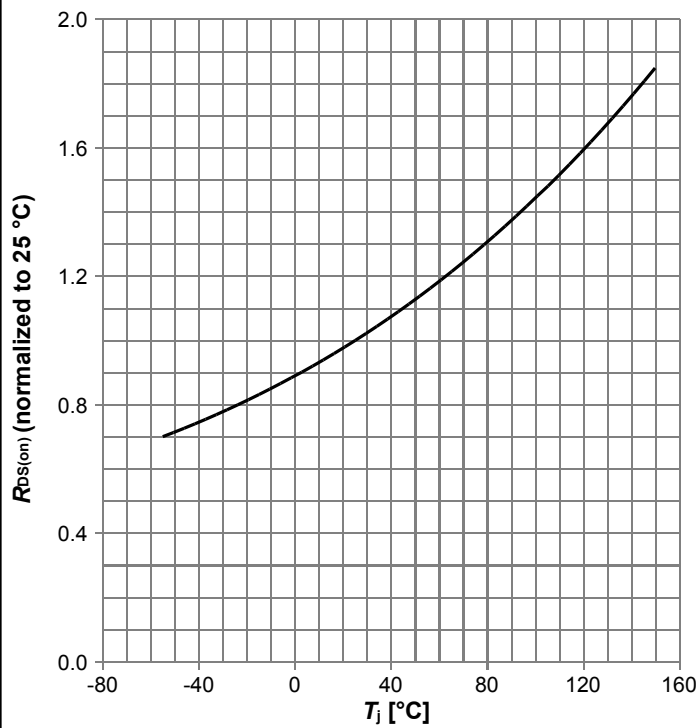
$I_D = f(V_{GS})$, $|V_{DS}| > 2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



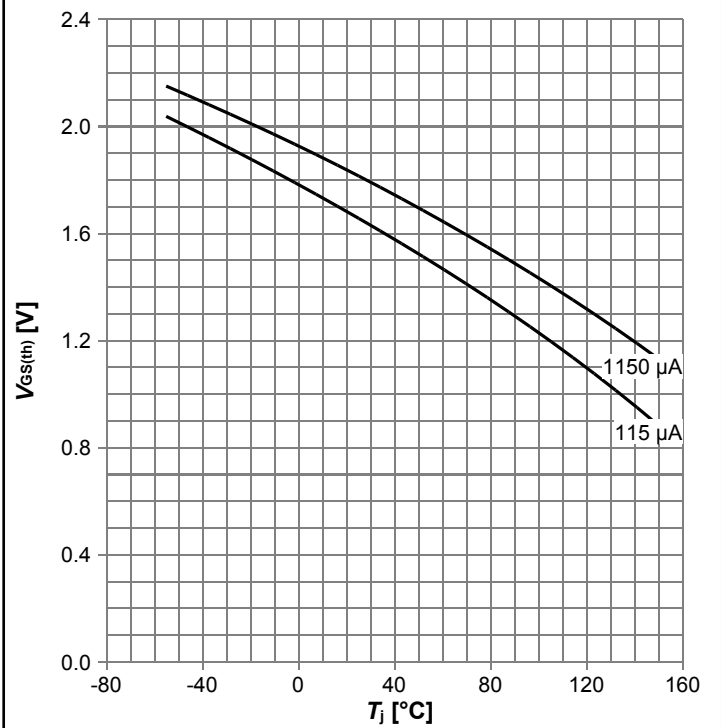
$R_{DS(on)} = f(V_{GS})$, $I_D = 50\text{ A}$; parameter: T_j

Diagram 9: Normalized drain-source on resistance



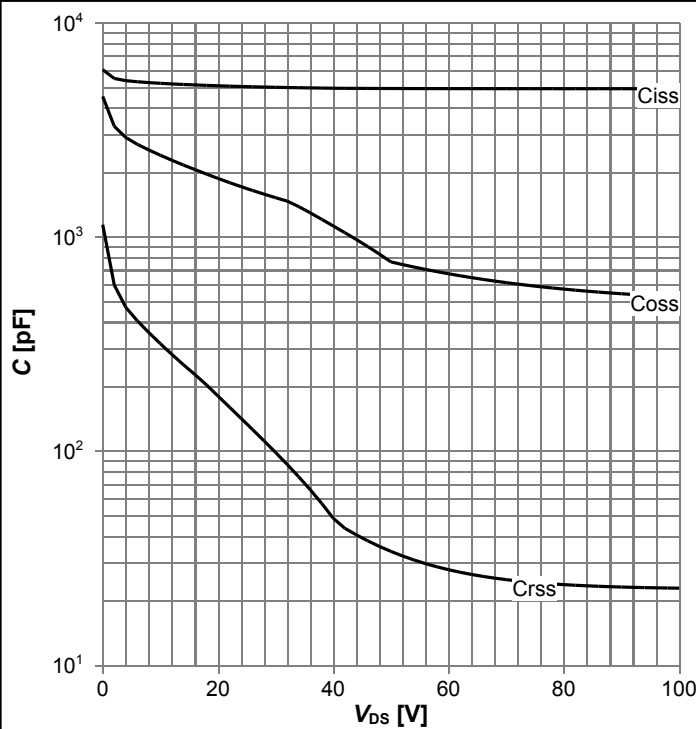
$R_{DS(on)}=f(T_j)$, $I_D=50$ A, $V_{GS}=10$ V

Diagram 10: Typ. gate threshold voltage



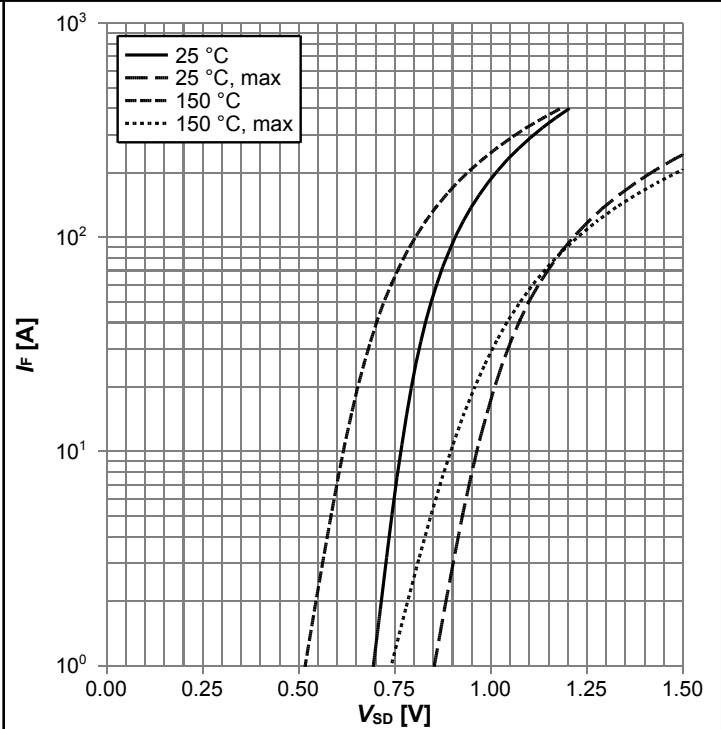
$V_{GS(th)}=f(T_j)$, $V_{GS}=V_{DS}$; parameter: I_D

Diagram 11: Typ. capacitances



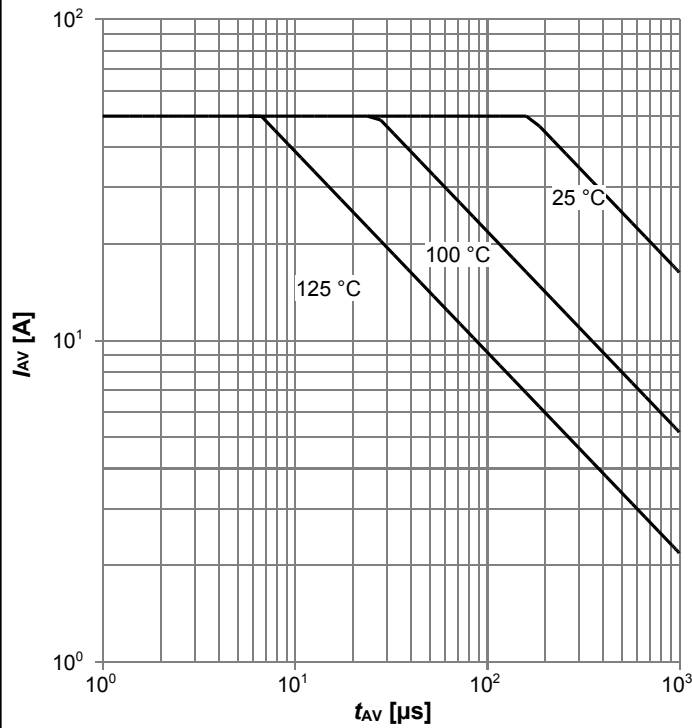
$C=f(V_{DS})$; $V_{GS}=0$ V; $f=1$ MHz

Diagram 12: Forward characteristics of reverse diode



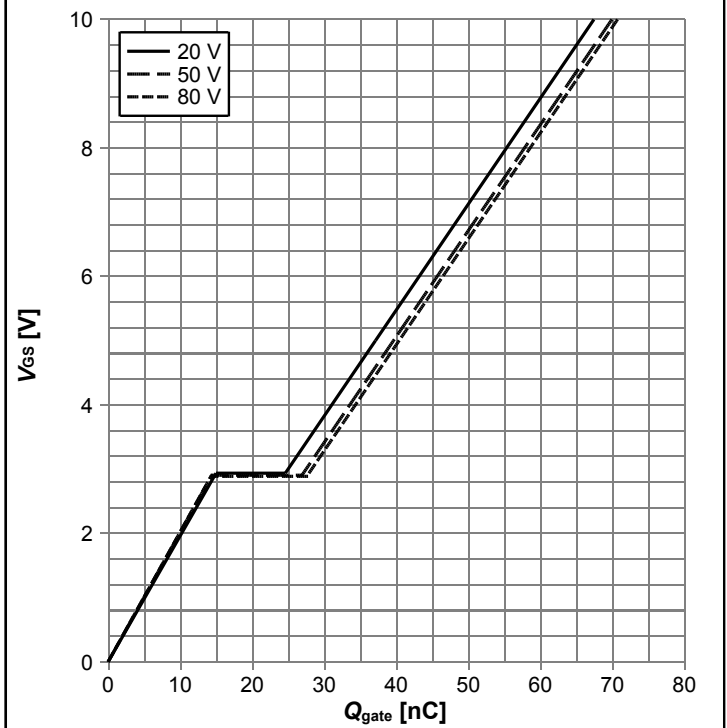
$I_F=f(V_{SD})$; parameter: T_j

Diagram 13: Avalanche characteristics



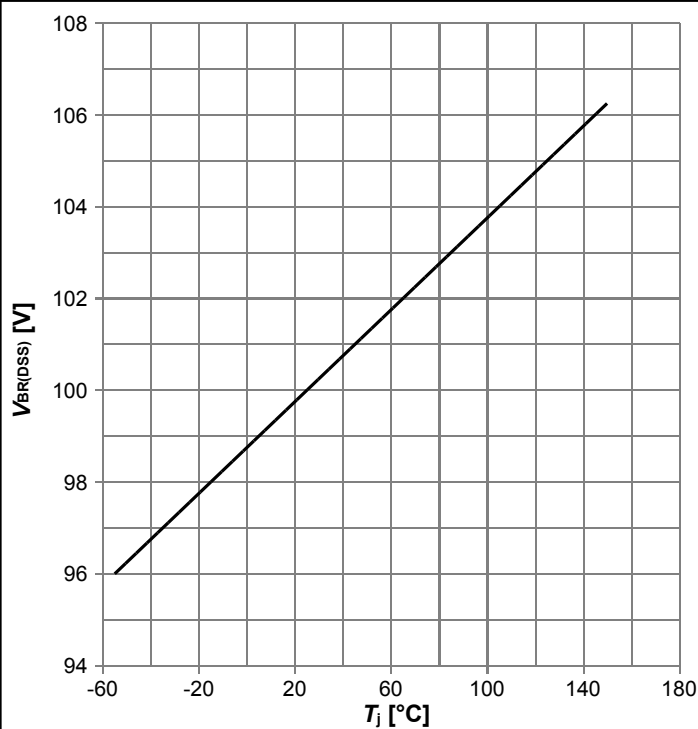
$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



$V_{GS}=f(Q_{gate}), I_D=50 A$ pulsed, $T_j=25 \text{ }^\circ\text{C}$; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage



$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

Diagram Gate charge waveforms



5 Package Outlines



| DIM | MILLIMETERS | |
|-------|-------------|------|
| | MIN | MAX |
| A | 0.90 | 1.10 |
| b | 0.31 | 0.54 |
| b1 | 0.02 | 0.22 |
| c | 0.15 | 0.35 |
| D | 5.15 | 5.49 |
| D1 | 4.95 | 5.35 |
| D2 | 3.70 | 4.40 |
| E | 5.95 | 6.35 |
| E1 | 5.70 | 6.10 |
| E2 | 3.40 | 3.80 |
| e | 1.27 | |
| N | 8 | |
| L | 0.45 | 0.71 |
| M | 0.45 | 0.75 |
| theta | 8.5° | 12° |
| aaa | 0.25 | |
| eee | 0.08 | |

| |
|------------------------------------|
| DOCUMENT NO. Z8B00003332 |
| SCALE 0 2 4mm |
| EUROPEAN PROJECTION |
| ISSUE DATE 10-04-2013 |
| REVISION 04 |

Figure 1 Outline PG-TDSON-8, dimensions in mm

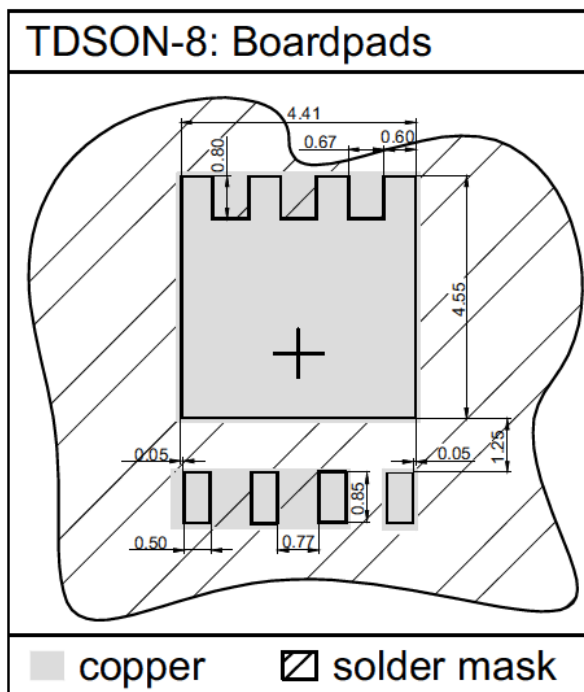


Figure 2 Outline Footprint (TDSO-8)

Revision History

BSC0802LS

Revision: 2019-05-13, Rev. 2.2

Previous Revision

| Revision | Date | Subjects (major changes since last revision) |
|----------|------------|--|
| 2.0 | 2016-09-30 | Release of final version |
| 2.1 | 2016-10-20 | Update " Features " |
| 2.2 | 2019-05-13 | Update Diagrams 5, 8 and 9 |

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