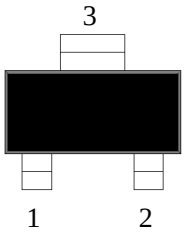
1、Description

PNPN devices designed for high volume, line-powered consumer applications such as relay and lamp drivers, small motor controls, gate drivers for larger thyristors, and sensing and detection circuits. Supplied in an inexpensive plastic **SOT-89-2L** package which is readily adaptable for use in automatic insertion equipment.

2、Features

- Sensitive gate allows triggering by micro-controllers and other logic circuits
- Blocking voltage to 800 volts
- On-state RMS current to 1.0A RMS at 50˚C
- Ultra low gate trigger current
- Glass-Passivated Surface for Reliability and Uniformity

3、Pinning information

PIN	Description	Simplified outline	Symbol
1	Cathode (K)		
2	Gate (G)		
3	Anode (A)		

SOT-89-2L

4、Quick reference data

SYMBOL	PARAMETER	MAX	UNIT
V_{DRM} V_{RRM}	Repetitive peak off-state voltages	800	V
$I_{T(RMS)}$	RMS on-state current	1.0	A
I_{TSM}	Non-repetitive peak on-state current	10	A
I_{GT}	Gate trigger current	100	uA

5、Thermal characteristics

SYMBOL	PARAMETER		Value	UNIT
Rth(j-c)	**junction to case(AC)**	SOT-89-2L	32	°C/W

6、Limiting value

Limiting values in accordance with the Maximum System(IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{DRM} V_{RRM}	Repetitive peak off-state voltages		-	800	V
$I_{T(RMS)}$	RMS on-state current	Full Cycle Sine Wave 50 to 60 Hz (TC = 50°C)	-	1.0	A
I_{TSM}	Non-repetitive peak Surge current	One Full cycle, 60 Hz, T_J = +110°C	-	10	A
I^2t	I^2t for fusing	t =8.3ms	-	0.32	A^2s
V_{GM}	Peak gate voltage	Pulse Width ≤ 1.0 μs, TC = 85°C	-	5	V
P_{GM}	Peak gate power	Pulse Width ≤1.0 μs, TC = 85°C	-	0.5	W
$P_{G(AV)}$	Average gate power	Pulse Width ≤1.0 μs, TC = 85°C	-	0.1	W
T_{stg}	Storage temperature		-40	150	°C
T_j	Operating junction temperature		-40	110	°C

7、Characteristics

T_J = 25℃ unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Static characteristics						
I_{GT}	Gate trigger current	V_D = 12 V; RL =33Ω	-	50	100	uA
I_L	Latching current	I_G=1.2XI_{GT}	-	-	5	mA
I_H	Holding current	IT =0.05mA	-	-	3	mA
V_{TM}	On-state voltage	I_{TM} =1.1A tp=380μs	-	-	1.50	V
V_{GT}	Gate trigger voltage	V_D = 12 V; RL =33Ω	-	-	0.8	V
V_{GD}	Gate Non–Trigger Voltage	VD =VDRM; Tj =110℃	0.2	-	-	V
I_{DRM} I_{RRM}	V_D=V_{DRM} V_R=V_{RRM}	T_J = 25°C	-	-	5	uA
		T_J = 110°C	-	-	500	uA
Dynamic Characteristics						
dV/dt	Critical rate of rise of off-state voltage	V_D=2/3V_{DRM} Gate Open Tj =110°C	10	-	-	V/μs

8、Electrical Characteristics Curve

FIG.1 Maximum power dissipation versus RMS on-state current

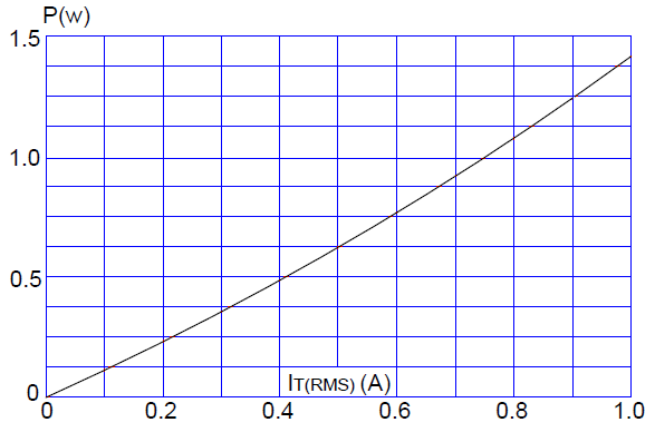


FIG.2: RMS on-state current versus case temperature

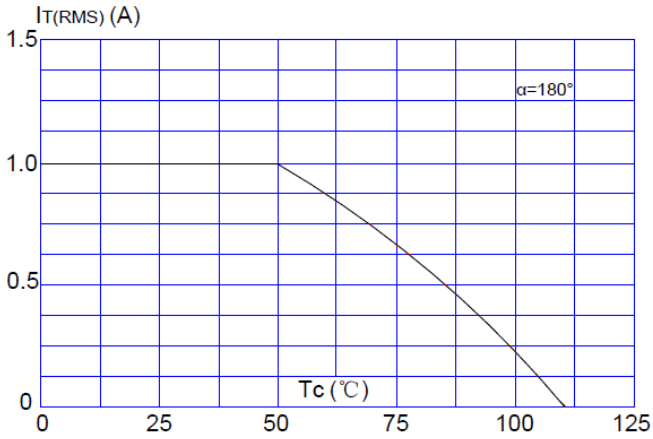


FIG.3: Surge peak on-state current versus number of cycles

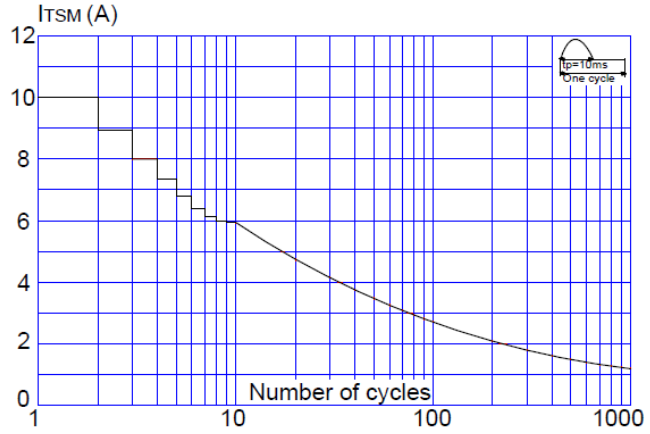


FIG.4: On-state characteristics (maximum values)

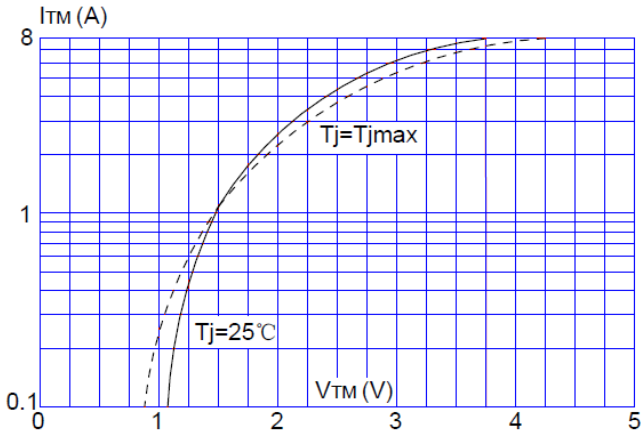


FIG.5: Non-repetitive surge peak on-state current for a sinusoidal pulse with width tp<10ms, and corresponging value of I^2t

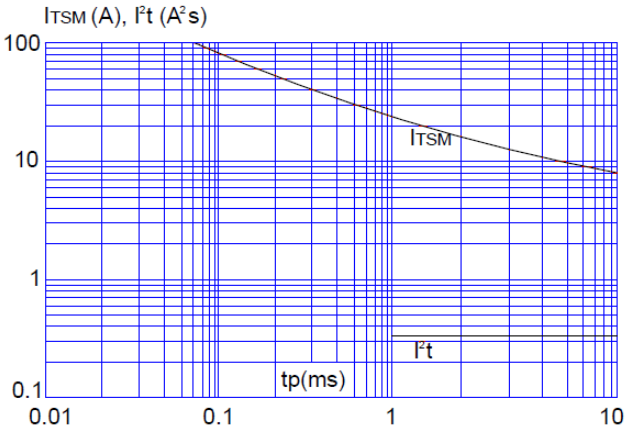
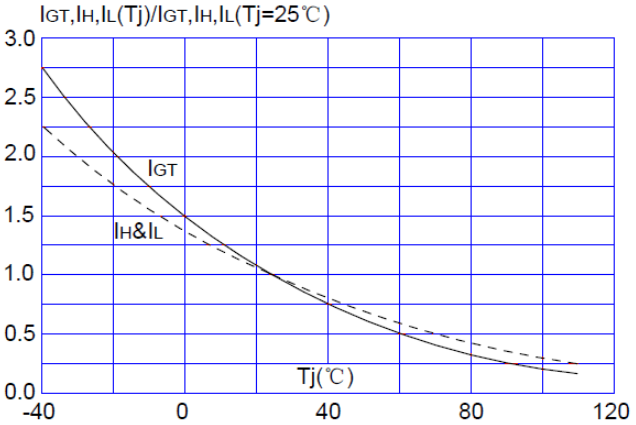
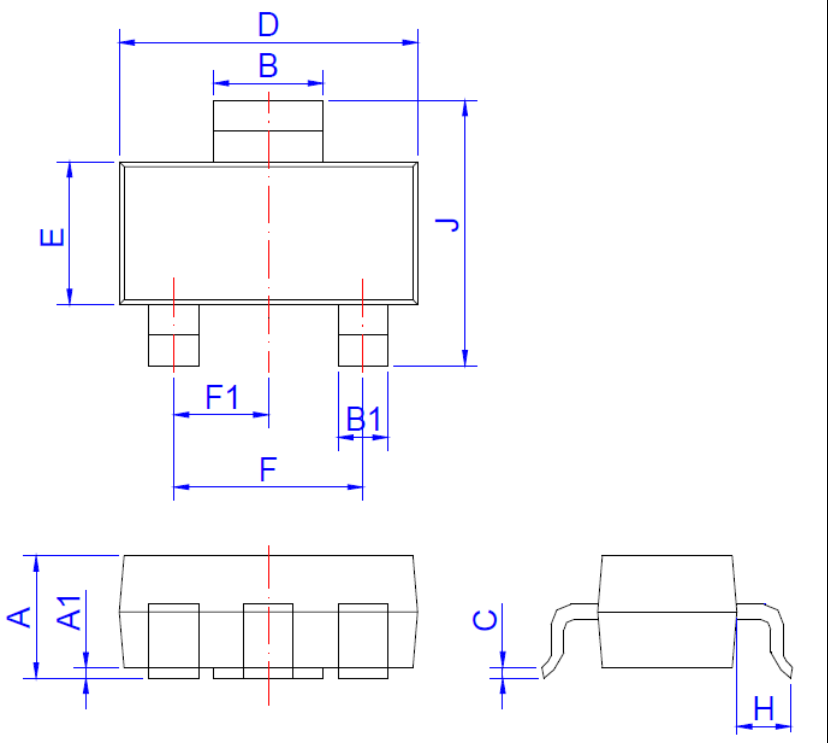


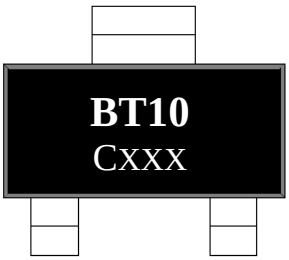
FIG.6: Relative variations of gate trigger current, holding current and latching current versus junction temperature



9、Package outline(SOT-89-2L)



Marking:



DIM	Inches			Milimeters		
	Min	Type	Max	Min	Type	Max
A	0.055	0.039	0.065	1.40	1.50	1.65
A1	0	0.002	0.004	0	0.06	0.10
B	0.063	0.067	0.071	1.60	1.70	1.80
B1	0.012	0.016	0.020	0.30	0.40	0.50
C	0.009	0.010	0.013	0.22	0.26	0.32
D	0.189	0.197	0.209	4.80	5.00	5.30
E	0.110	0.118	0.126	2.80	3.00	3.20
F		0.118			3.00	
F1		0.059			1.50	
H	0.028	0.033	0.039	0.70	0.85	1.00
J	0.169	0.177	0.185	4.30	4.50	4.70