

**N-Channel 250-V (D-S) MOSFET**

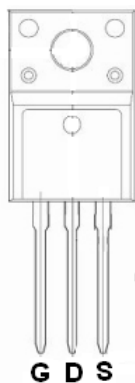
**GENERAL DESCRIPTION**

The ME15N25F is the N-Channel logic enhancement mode power field effect transistors, using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on state resistance.

**PIN CONFIGURATION**

(TO-220F)

Top View

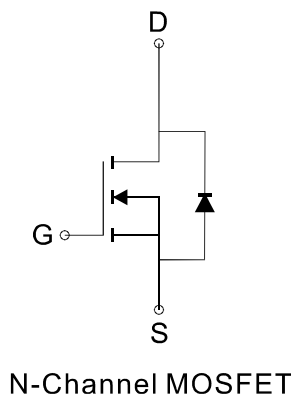


**FEATURES**

- $R_{DS(ON)} \leq 220m\Omega @ V_{GS}=10V$
- Super high density cell design for extremely low  $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

**APPLICATIONS**

- Power Management in Note book
- DC/DC Converter
- Load Switch
- LCD Display inverter



Ordering Information: ME15N25F (Pb-free)

ME15N25F-G (Green product-Halogen free)

**Absolute Maximum Ratings (Tc=25°C Unless Otherwise Noted)**

Parameter	Symbol	Maximum Ratings	Unit
Drain-Source Voltage	$V_{DS}$	250	V
Gate-Source Voltage	$V_{GS}$	$\pm 25$	V
Continuous Drain Current	$I_D$	Tc=25°C	12.5
		Tc=70°C	10.4
Pulsed Drain Current	$I_{DM}$	50	A
Maximum Power Dissipation	$P_D$	Tc=25°C	61.9
		Tc=70°C	43.3
Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to 175	°C
Thermal Resistance-Junction to Case *	$R_{\theta JC}$	2.42	°C/W

\* The device mounted on 1in<sup>2</sup> FR4 board with 2 oz copper

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**Electrical Characteristics** ( $T_c = 25^\circ\text{C}$  Unless Otherwise Specified)

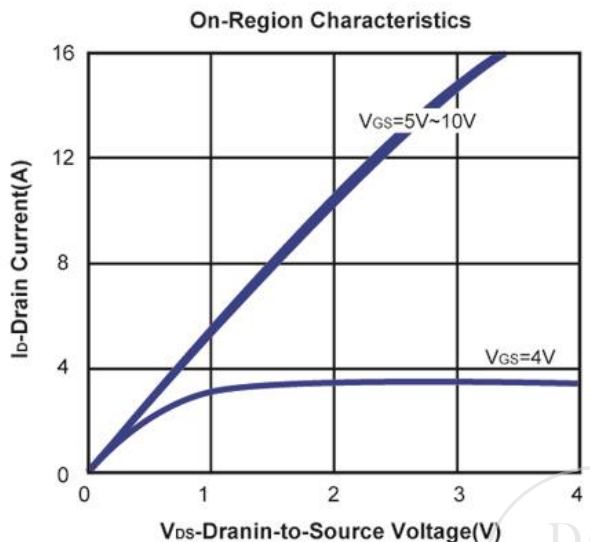
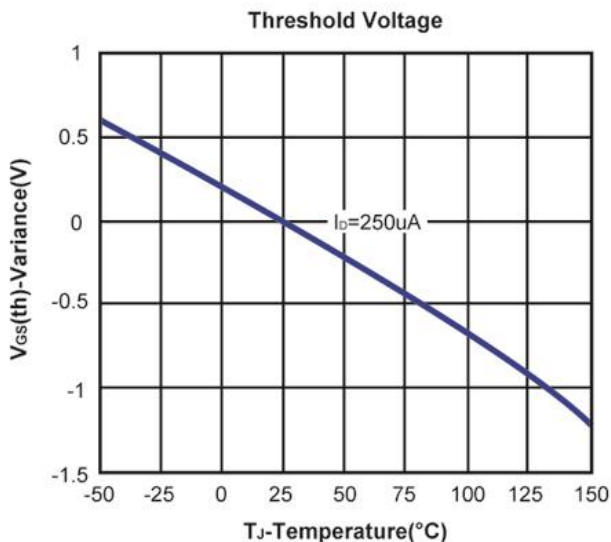
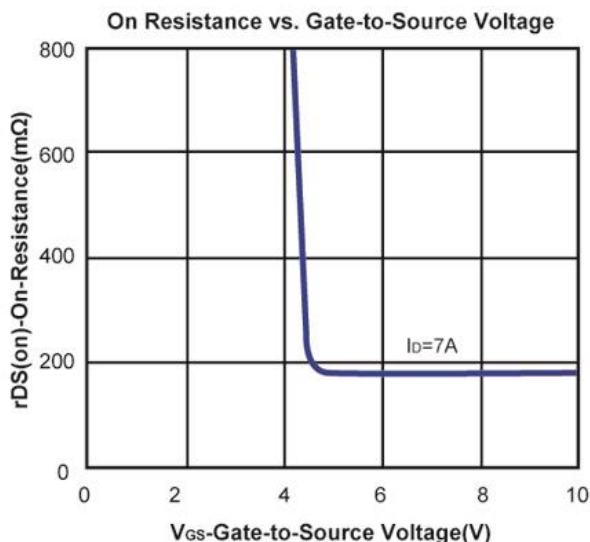
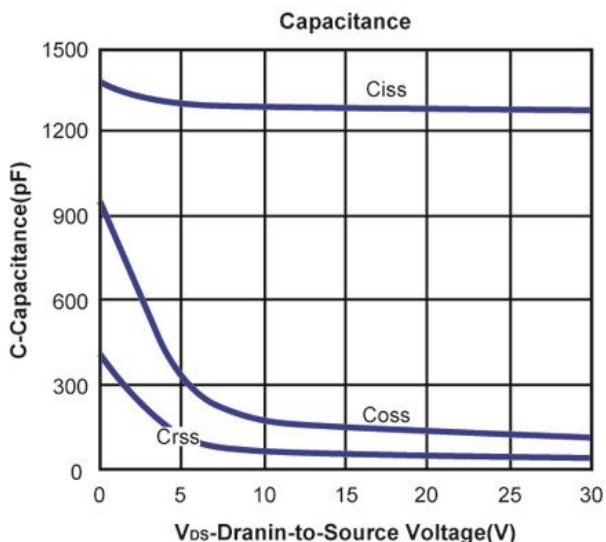
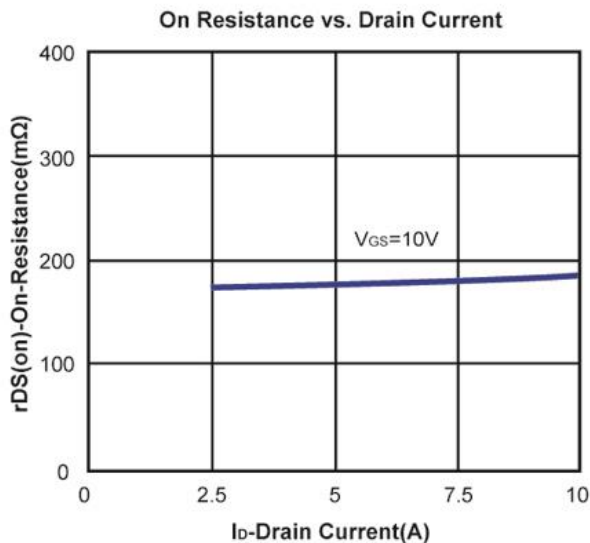
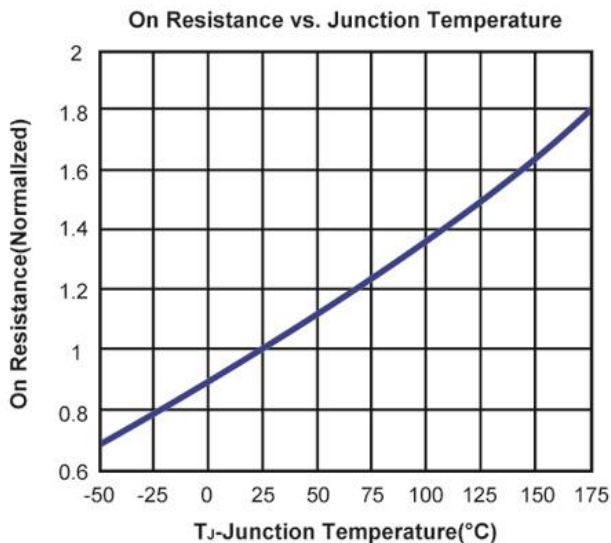
Symbol	Parameter	Limit	Min	Typ	Max	Unit
<b>STATIC</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\ \mu A$	250			V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\ \mu A$	2		4	V
$I_{GSS}$	Gate Leakage Current	$V_{DS}=0V, V_{GS}=\pm 25V$			$\pm 100$	nA
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=200V, V_{GS}=0V$			1	$\mu A$
$R_{DS(ON)}$	Drain-Source On-Resistance <sup>a</sup>	$V_{GS}=10V, I_D=7A$		180	220	$m\Omega$
$V_{SD}$	Diode Forward Voltage	$I_S=1A, V_{GS}=0V$		0.74	1	V
<b>DYNAMIC</b>						
$Q_g$	Total Gate Charge	$V_{DS}=200V, V_{GS}=10V, I_D=14A$		70		nC
$Q_{gs}$	Gate-Source Charge			16.3		
$Q_{gd}$	Gate-Drain Charge			24.6		
$C_{iss}$	Input Capacitance	$V_{DS}=25V, V_{GS}=0V, f=1MHz$		1277		pF
$C_{oss}$	Output Capacitance			118		
$C_{rss}$	Reverse Transfer Capacitance			39		
$t_{d(on)}$	Turn-On Delay Time	$V_{DS}=125V, R_L=18\Omega, V_{GEN}=10V, R_G=25\Omega$		44.4		ns
$t_r$	Turn-On Rise Time			43.4		
$t_{d(off)}$	Turn-Off Delay Time			199		
$t_f$	Turn-Off Fall Time			75.9		

Notes: a. Pulse test: pulse width  $\leq 300\mu s$ , duty cycle  $\leq 2\%$ , Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

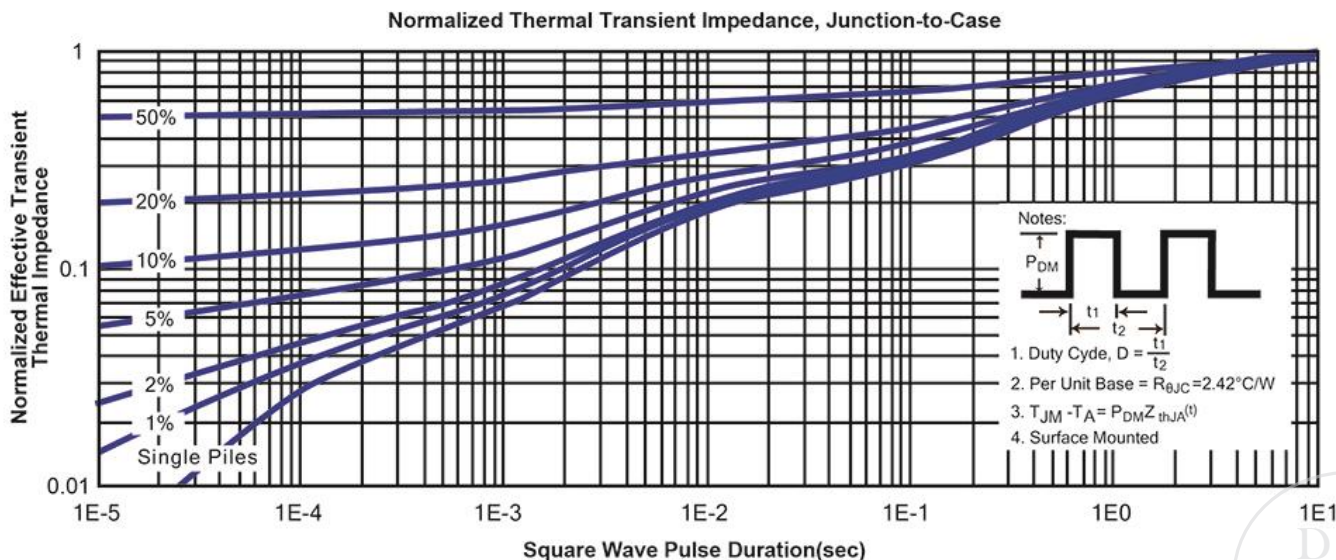
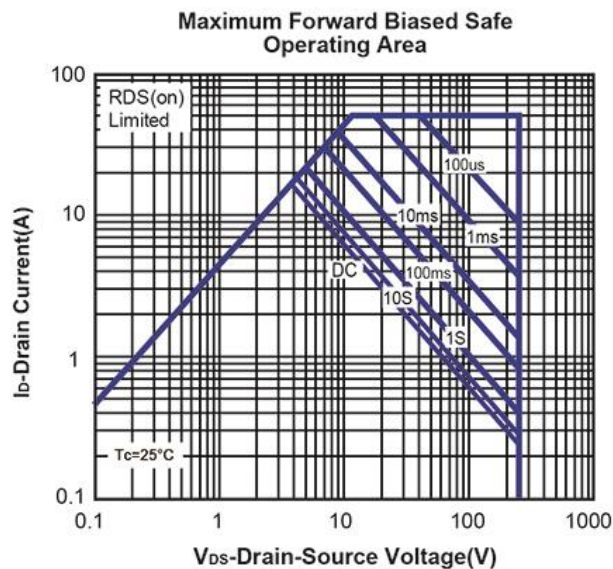
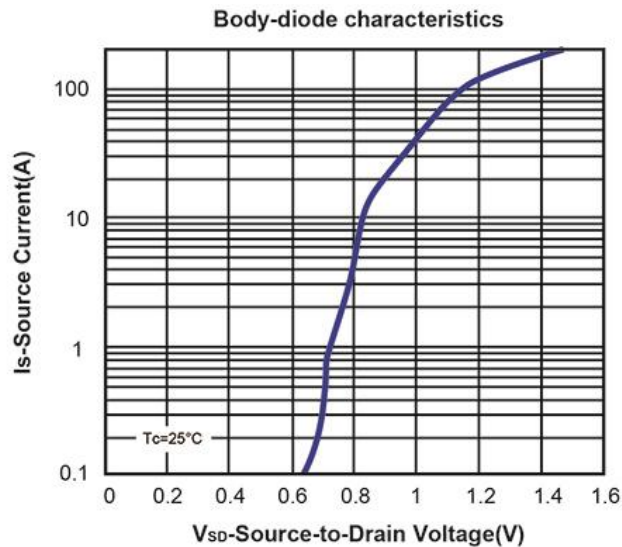
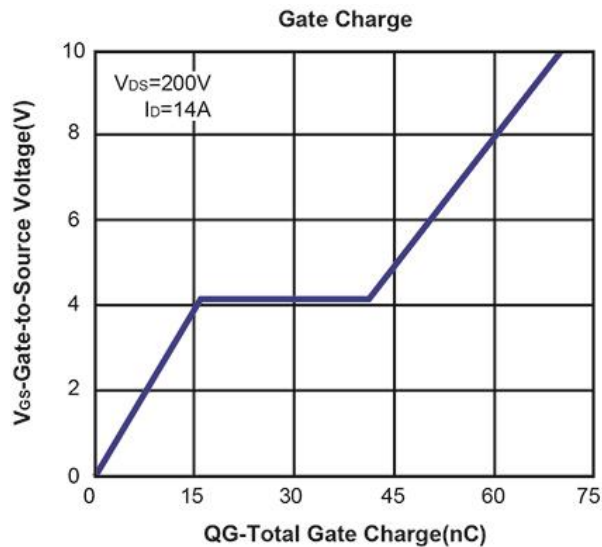
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**Typical Characteristics (T<sub>J</sub> =25°C Noted)**

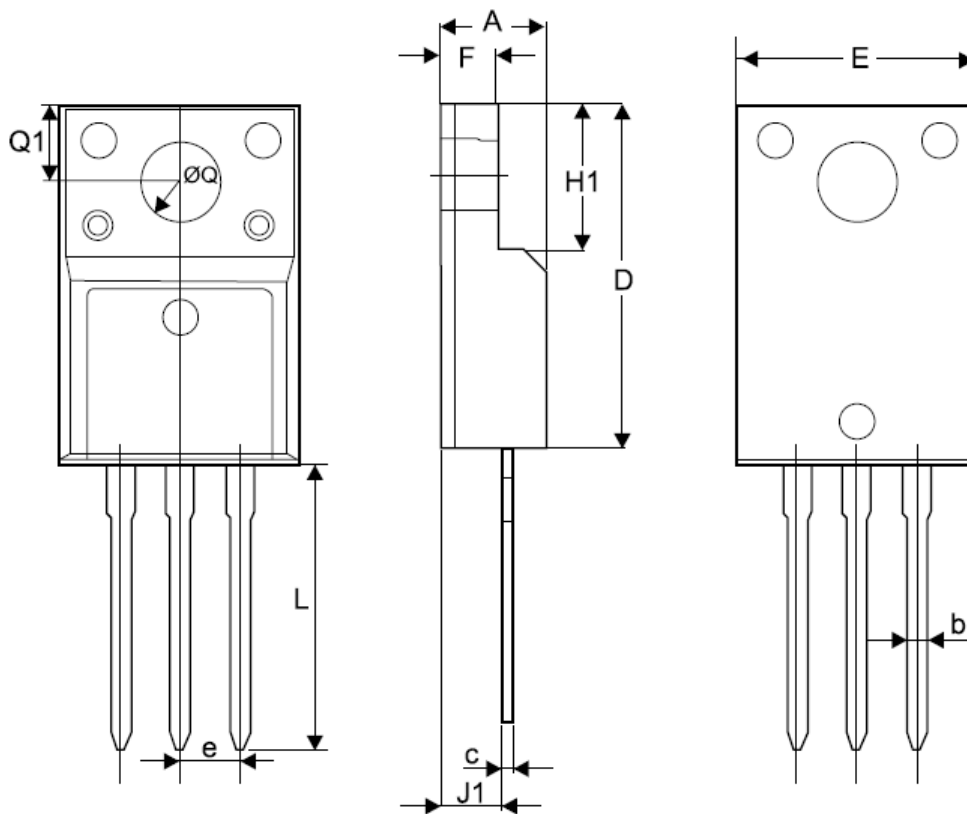


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**TO-220F Package Outline**



Symbol	MILLIMETERS(mm)	
	MIN	MAX
A	4.40	5.00
b	0.60	1.00
C	0.30	0.70
D	15.40	16.40
E	6.96	10.46
F	2.30	2.80
e	2.54 TYP	
H1	6.40	7.00
J1	2.45	3.05
L	12.28	13.68
ØQ	2.92	3.38
Q1	3.05	3.55