A96T418

Datasheet

CMOS Single Chip 8-bit MCU for Touch Sensing, Smart Proximity Sensing Microcontroller

Datasheet Version 1.04

Features

Core
- 8-bit CISC M8051 core

Memory
- 32 KB on-chip flash
- 256 bytes IRAM / 1792 bytes XRAM

General Purpose I/O (GPIO)
- Normal I/O: max 26 ports
- High sink current port: max 8 ports

Timer/counter
- Basic Interval Timer (BIT)
- Watch Dog Timer (WDT)
- 8-bit × 1-ch (T0)
- 16-bit × 5-ch (T1/T2/T3/T4/T5)

20-Ch Self Capacitive Touch Switch
- 10V Conducted Susceptibility (CS) Immunity
- 16-bit Sensing Resolutions
- Key detection mode : Single/Multi-mode

USI (USART + SPI + I2C)
- 8-bit USART × 1-ch, 8-bit SPI × 1-ch and I2C × 1-ch

USART (USART + SPI)
- 8-bit USART × 1-ch and 8-bit SPI × 1-ch

12-bit A/D Converter
- 8 External Input channels
- 1-Channel for internal reference voltage

LED Driver
- 8COM (250mA) / 16SEG (13.61mA)
- Constant Current Segment (3 level)

Power-on Reset
- Reset release level (1.2V)

Low Voltage Reset
- 15 levels detect

Low Voltage Indicator
- 10 levels detect

Power down mode
- STOP / IDLE mode

Operating voltage and frequency
- 2.0V~ 5.5V @ 16MHz
- 2.7V~ 5.5V (Touch, ADC, LED Driver)

Operating temperature
- –40℃ to +85℃

Packages
- 28 / 24 / 20 SOP
- Pb-free package

Product selection table

Table 1. Device Summary

Device Name	FLASH	XRAM	IRAM	Timer (PWM)	Communication function		Touch Switch	LED Driver	ADC	GPIO	Package
					USART	USI					
A96T418GD	32KB	1792B	256B	6	1	1	20-ch	8COM / 16SEG	8-ch	25	28 SOP
A96T418LD	32KB	1792B	256B	5	1	1	17-ch	8COM / 16SEG	8-ch	21	24 SOP
A96T418FD	32KB	1792B	256B	4	1	1	13-ch	8COM / 15SEG	8-ch	17	20 SOP

Contents

List of figures

List of tables

1 Description

The A96T418 is an advanced CMOS 8-bit microcontroller with 32Kbytes of FLASH. This is powerful microcontroller which provides a highly flexible and cost effective solution to many embedded control applications.

1.1 Device overview

In this section, features of A96T418 and peripheral counts are introduced.

Table 2. A96T418 Device Features and Peripheral Counts

Peripherals		Description
Core	CPU	8-bit CISC core (M8051, 2 clocks per cycle)
	Interrupt	Up to 23 peripheral interrupts supported. • EINT0 to 7, EINT8, EINT10, EINT11, EINT12 (5) • Timer (0/1/2/3/4/5) (6) • WDT (1) • BIT (1) • WT (1) • USART Rx/Tx (2) • USI 1-ch. *Rx/Tx/I2C (3) • Touch (1) • LED (1) • ADC (1) • LVI (1)
Memory	ROM (FLASH) capacity	• 32Kbytes FLASH with self-read and write capability • In-system programming (ISP) • Endurance: 10,000 times
	IRAM	256Bytes
	XRAM	1792Bytes
Programmable pulse generation		• Pulse generation (by T1/T2/T3/T4/T5) • 8-bit PWM (by T0) • 16-bit PPG (by T1/T2/T3/T4/T5)
Buzzer		8-bit × 1-ch
Minimum instruction execution time		125ns (@ 16MHz, NOP Instruction)
Power down mode		• STOP1 mode • STOP2 mode • IDLE mode
General Purpose I/O (GPIO)		• Normal I/O : 26 ports • High sink current port : 8 ports (P2[7:0])

Table 1. A96T418 Device Features and Peripheral Counts (continued)

Peripherals		Description
Reset	Power on reset	Power on reset : 1.2V
	Low voltage reset	• 15 levels detect • 1.61/1.77/1.88/2.00/2.13/2.28/2.46/2.68/2.81/3.06/ 3.21/3.56/3.73/3.91/4.25V
Low voltage indicator		level detect: 1.88~4.25V with 13 Levels
Watch Timer (WT)		• 14-bit x 1-ch • 3.91ms/0.25s/0.5s/1s/1min interval at 32.768KHz
Timer/counter		• Basic interval timer (BIT) 8-bit x 1-ch. • Watch Dog Timer (WDT) 8-bit x 1-ch. • 8-bit x 1-ch (Timer 0) • 16-bit x 5-ch (Timer 1/2/3/4/5)
Communication function	USI	• USART + SPI + I2C • 8-bit USART × 1-ch, 8-bit SPI × 1-ch and I2C × 1-ch
	USART	• USART + SPI • 8-bit USART × 1-ch and 8-bit SPI × 1-ch • Receiver timer out (RTO) • 0% error baud rate
12-bit A/D converter		8 Input channels
20-Ch Self Capacitive Touch Switch		• Fast Initial Self-Calibration • Key detection mode : Single/Multi-mode • CS Immunity : 10V • 16-bit Sensing Resolutions • Support Touch Key Int. Wakeup at Power down
LED Driver		• 8COM (250mA) x 16SEG (13.61mA) • Constant Current Segment (3 level)
Oscillator type		• 2, 4, 8, 16MHz (internal RC oscillator) • 32.768kHz Crystal for sub clock
Internal RC oscillator		• HSIRC 16MHz ±1.5% (TA=0~ +50°C) • HSIRC 16MHz ±2.0% (TA=-10~ +70°C) • HSIRC 16MHz ±2.5% (TA=-40~ +85°C) • LSIRC 128kHz ±20% (TA= -40~ +85°C)
Operating voltage and frequency		• 2.0V~ 5.5V @ 16MHz • 2.7V~ 5.5V (Touch, ADC, LED Driver)
Operating temperature		-40℃ to +85℃
Package		• 28 SOP • 24 SOP • 20 SOP • Pb-free packages

1.2 Block Diagram

In this section, A96T418 devices and peripheral are described in a block diagram.

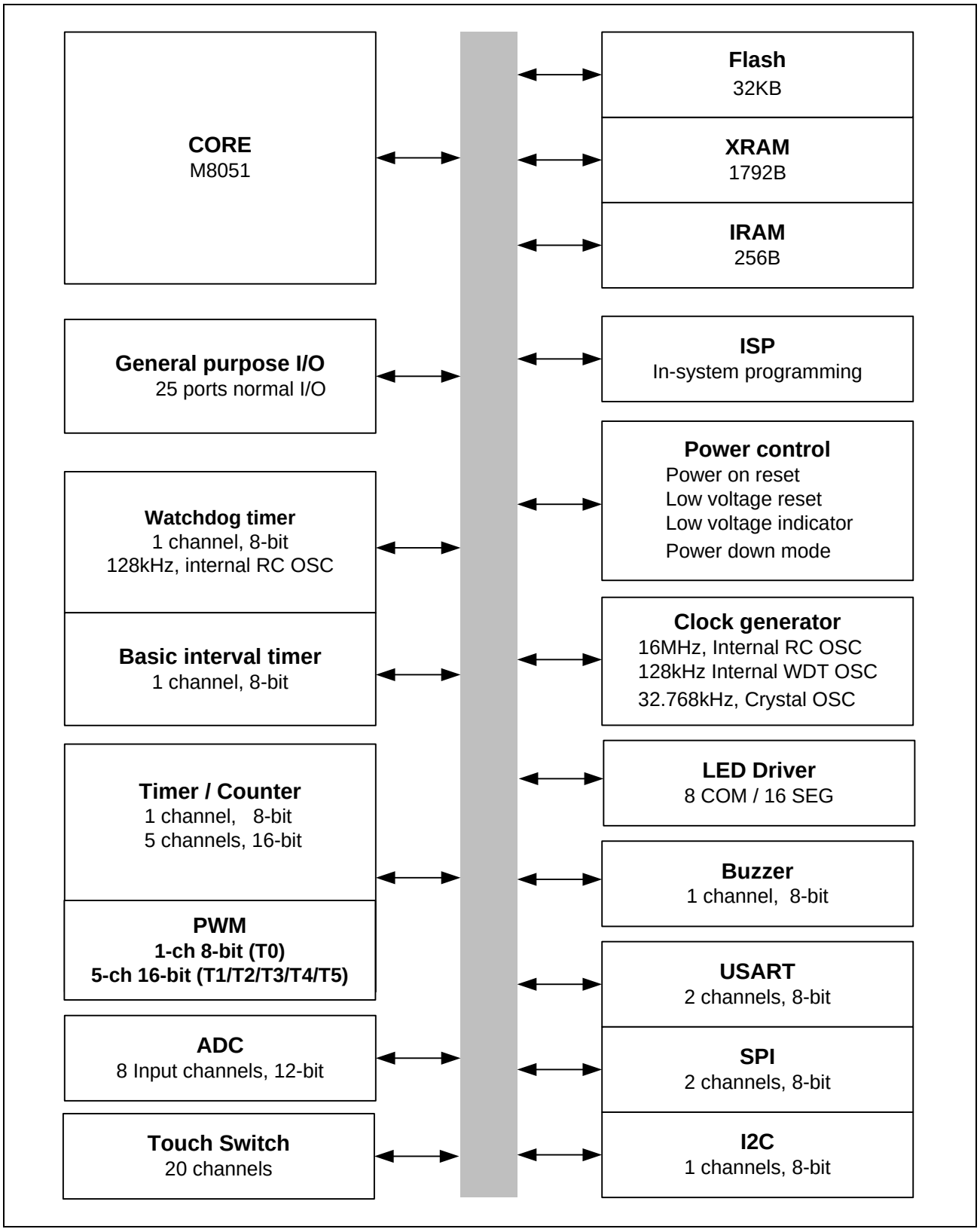
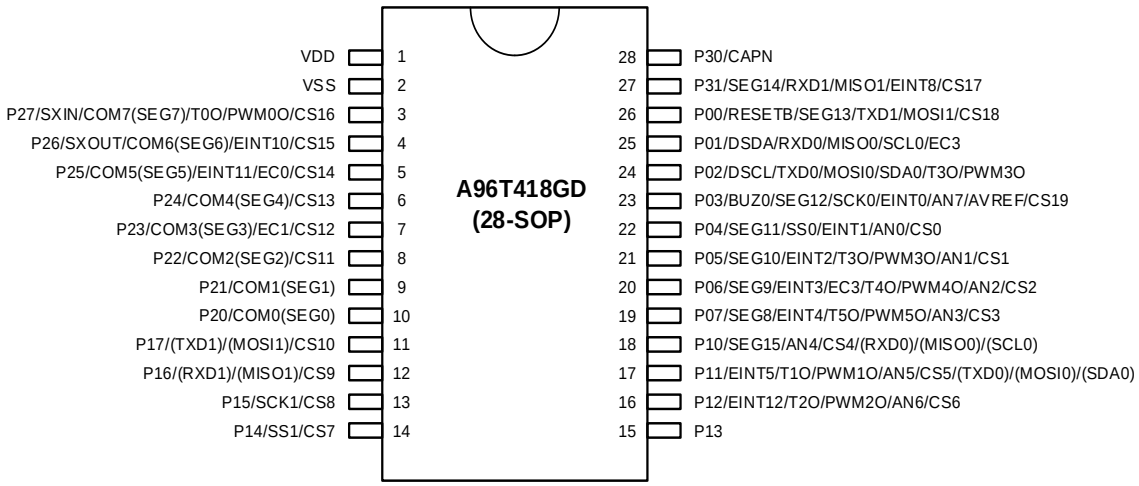


Figure 1. Block diagram of A96T418

2 Pinouts and pin description

Pinouts and pin descriptions of A96T376 device are introduce in the following sections.

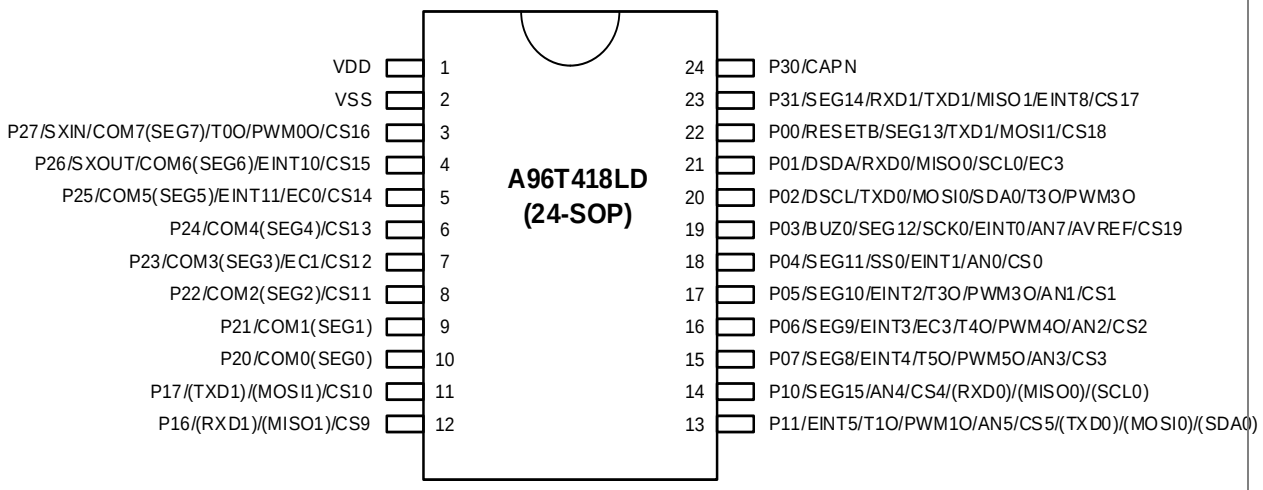
2.1 Pinouts



NOTES:

1. The programmer (E-PGM+, E-Gang4/6) uses P0[2:1] pin as DSCL, DSDA.

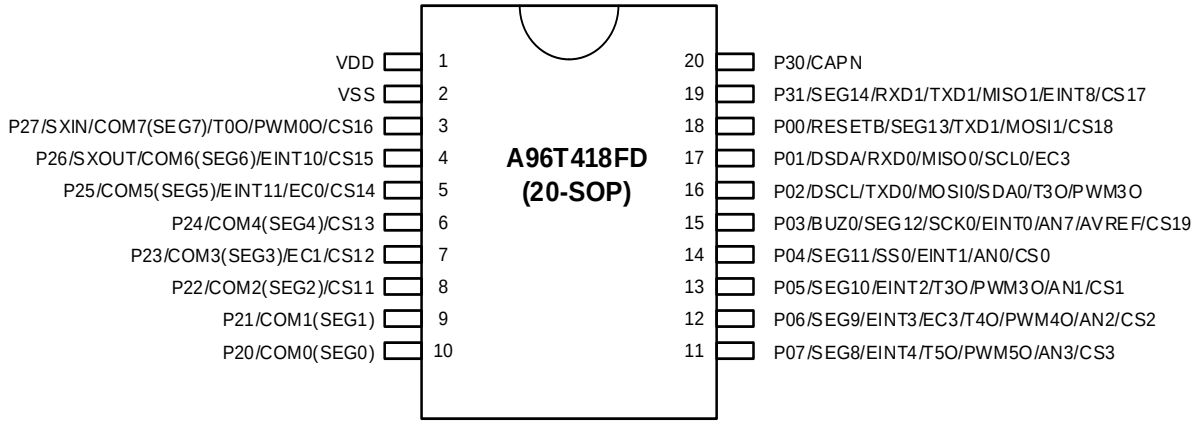
Figure 2. A96T418 28SOP pin assignment (Without VDDLED)



NOTES:

1. The programmer (E-PGM+, E-Gang4/6) uses P0[2:1] pin as DSCL, DSDA.
2. The P12-P15 pins should be selected as a push-pull output or an input with pull-up resistor by software control.

Figure 3. A96T418 24SOP pin assignment (Without VDDLED)



NOTES:

1. The programmer (E-PGM+, E-Gang4/6) uses P0[2:1] pin as DSCL, DSDA.
2. The P10-P17 pins should be selected as a push-pull output or an input with pull-up resistor by software control.

Figure 4. A96T418 20SOP pin assignment (Without VDDLED)

2.2 Pin Description

Table 3. Normal Pin Description

PIN Name	I/O	Function	@RESET	Shared with
P00	I/O	Port P0 8-Bit I/O Port Can be set in input or output mode in 1-bit units Internal pull-up register can be used via software when this port is used as input port Open Drain enable register can be used via software when this port is used as output port	Input	RESETB/SEG13/TXD1/MOSI1/CS18
P01				DSDA/RXD0/MISO0/SCL0/EC3
P02				DSCL/TXD0/MOSI0/SDA0/T3O/PWM3O
P03				BUZ0/SEG12/SCK0/EINT0/AN7/AVREF/CS19
P04				SEG11/SS0/EINT1/AN0/CS0
P05				SEG10/EINT2/T3O/PWM3O/AN1/CS1
P06				SEG9/EINT3/EC3/T4O/PWM4O/AN2/CS2
P07				SEG8/EINT4/T5O/PWM5O/AN3/CS3
P10	I/O	Port P1 8-Bit I/O Port Can be set in input or output mode in 1-bit units Internal pull-up register can be used via software when this port is used as input port Open Drain enable register can be used via software when this port is used as output port. The P12 – P15 are not in the 24-pin package. The P10 – P17 are not in the 20-pin package.	Input	SEG15/AN4/CS4/(RXD0)/(MISO0)/(SCL0)
P11				EINT5/T1O/PWM1O/AN5/CS5/(TXD0)/(MOSI0)/(SDA0)
P12				EINT12/T2O/PWM2O/AN6/CS6
P13				
P14				SS1/CS7
P15				SCK1/CS8
P16				(RXD1)/(MISO1)/CS9
P17				(TXD1)/(MOSI1)/CS10
P20	I/O	Port P2 8-Bit I/O Port Can be set in input or output mode in 1-bit units Internal pull-up register can be used via software when this port is used as input port Open Drain enable register can be used via software when this port is used as output port.	Input	COM0(SEG0)
P21				COM1(SEG1)
P22				COM2(SEG2)/CS11
P23				COM3(SEG3)/EC1/CS12
P24				COM4(SEG4)/CS13
P25				COM5(SEG5)/EINT11/EC0/CS14
P26				SXOUT/COM6(SEG6)/EINT10/CS15
P27				SXIN/COM7(SEG7)/T0O/PWM0O/CS16

Table 3. Normal Pin Description (continued)

PIN Name	I/O	Function	@RESET	Shared with
P30	I/O	Port P3 2-Bit I/O Port Can be set in input or output mode in 1-bit units Internal pull-up register can be used via software when this port is used as input port Open Drain enable register can be used via software when this port is used as output port. The P31 is not in the package with VDDLED pin.	Input	CAPN
P31				SEG14/RXD1/MISO1/EINT8/CS17
EINT0	I/O	External interrupt inputs	Input	P03/BUZ0/SEG12/SCK0/AN7/AVREF/CS19
EINT1				P04/SEG11/SS0/AN0/CS0
EINT2	I/O	External interrupt input and Timer 3 capture input	Input	P05/SEG10/T3O/PWM3O/AN1/CS1
EINT3	I/O	External interrupt input and Timer 4 capture input	Input	P06/SEG9/EC3/T4O/PWM4O/AN2/CS2
EINT4	I/O	External interrupt input and Timer 5 capture input	Input	P07/SEG8/T5O/PWM5O/AN3/CS3
EINT5	I/O	External interrupt input and Timer 1 capture input	Input	P11/T1O/PWM1O/AN5/CS5/(TXD0)/(MOSI0)/(SDA0)
EINT8	I/O	External Interrupt input	Input	P31/SEG14/RXD1/MISO1/CS17
EINT10	I/O	External interrupt input	Input	P26/SXOUT/COM6(SEG6)/CS15
EINT11	I/O	External interrupt input	Input	P25/COM5(SEG5)/EC0/CS14
EINT12	I/O	External interrupt input and Timer 2 capture input	Input	P12/T2O/PWM2O/AN6/CS6
T0O	I/O	Timer 0 interval output	Input	P27/SXIN/COM7(SEG7)/PWM0O/CS16
T1O	I/O	Timer 1 interval output	Input	P11/EINT5/PWM1O/AN5/CS5/(TXD0)/(MOSI0)/(SDA0)
T2O	I/O	Timer 2 interval output	Input	P12/EINT12/PWM2O/AN6/CS6

Table 3. Normal Pin Description (continued)

PIN Name	I/O	Function	@RESET	Shared with
T3O	I/O	Timer 3 interval output	Input	P02/DSCL/TXD0/MOSI0/SDA0/PWM3O P05/ SEG10/EINT2/PWM3O/AN1/CS1
T4O	I/O	Timer 4 interval output	Input	P06/SEG9/EINT3/EC3/PWM4O/AN2/CS2
T5O	I/O	Timer 5 interval output	Input	P07/SEG8/EINT4/PWM5O/AN3/CS3
PWM0O	I/O	Timer 0 PWM output	Input	P27/SXIN/T0O/COM7/CS16
PWM1O	I/O	Timer 1 PWM output	Input	P11/EINT5/T1O/AN5/CS5/(TXD0)/(MOSI0)/(SDA0)
PWM2O	I/O	Timer 2 PWM output	Input	P12/EINT12/T2O/AN6/CS6
PWM3O	I/O	Timer 3 PWM output	Input	P02/DSCL/TXD0/MOSI0/SDA0/T3O P05/ SEG10/EINT2/T3O/AN1/CS1
PWM4O	I/O	Timer 4 PWM output	Input	P06/SEG9/EINT3/EC3/T4O/AN2/CS2
PWM5O	I/O	Timer 5 PWM output	Input	P07/SEG8/EINT4/T5O/AN3/CS3
EC0	I/O	Timer 0 event count input	Input	P25/COM5(SEG5)/EINT11/CS14
EC1	I/O	Timer 1 event count input	Input	P23/COM3(SEG3)/CS12
EC3	I/O	Timer 3 event count input	Input	P01/DSDA/RXD0/MISO0/SCL0 P06/SEG9/EINT3/T4O/PWM4O/AN2/CS2
BUZ0	I/O	Buzzer signal output	Input	P03/SEG12/SCK0/AN7/EINT0/AVREF/CS19
SCK0	I/O	Serial 0 clock input/output	Input	P03/BUZ0/SEG12/AN7/EINT0/AVREF/CS19
SCK1	I/O	Serial 1 clock input/output	Input	P15/CS8
MOSI0	I/O	SPI 0 master output, slave input	Input	P02/DSCL/TXD0/SDA0/T3O/PWM3O P11/EINT5/T1O/PWM1O/AN5/CS5/(TXD0)/(SDA0)
MOSI1	I/O	SPI 1 master output, slave input	Input	P00/RESETB/SEG13/TXD1/CS18 P17/(TXD1)/CS10
MISO0	I/O	SPI 0 master input, slave output	Input	P01/DSDA/RXD0/SCL0/EC3 P10/SEG15/AN4/CS4/(RXD0)/(SCL0)
MISO1	I/O	SPI 1 master input, slave output	Input	P16/(RXD1)/CS9 P31/SEG14/RXD1/EINT8/CS17
SS0	I/O	SPI 0 slave select input (Slave mode only)	Input	P04/SEG11/SS0/EINT1/AN0/CS0
SS1	I/O	SPI 1 slave select input (Slave mode only)	Input	P14/CS7
TXD0	I/O	UART 0 data output	Input	P02/DSCL/MOSI0/SDA0/T3O/PWM3O P11/EINT5/T1O/PWM1O/AN5/CS5/(MOSI0)/(SDA0)
TXD1	I/O	UART 1 data output	Input	P00/RESETB/SEG13/MOSI1/CS18 P17/(MOSI1)/CS10
RXD0	I/O	UART 0 data input	Input	P01/DSDA/MISO0/SCL0/EC3 P10/SEG15/AN4/CS4/(MISO0)/(SCL0)
RXD1	I/O	UART 1 data input	Input	P16/(MISO1)/CS9 P31/SEG14/MISO1/EINT8/CS17

Table 3. Normal Pin Description (continued)

PIN Name	I/O	Function	@RESET	Shared with
SCL0	I/O	I2C 0 clock input/output	Input	P01/DSDA/RXD0/MISO0/EC3 P10/SEG15/AN4/CS4/(RXD0)/(MISO0)
SDA0	I/O	I2C 0 data input/output	Input	P02/DSCL/TXD0/MOSI0/T3O/PWM3O P11/EINT5/T1O/PWM1O/AN5/CS5/(TXD0)/(MOSI0)
AVREF	I/O	A/D converter reference voltage	Input	P03/BUZ0/SEG12/SCK0/AN7/EINT0/CS19
AN0	I/O	A/D converter analog input channels	Input	P04/SEG11/SS0/EINT1/CS0
AN1				P05/SEG10/EINT2/T3O/PWM3O/CS1
AN2				P06/SEG9/EINT3/EC3/T4O/PWM4O/CS2
AN3				P07/SEG8/EINT4/T5O/PWM5O/CS3
AN4				P10/SEG15/CS4/(RXD0)/(MISO0)/(SCL0)
AN5				P11/EINT5/T1O/PWM1O/CS5/(TXD0)/(MOSI0)/(SDA0)
AN6				P12/EINT12/T2O/PWM2O/CS6
AN7				P03/BUZ0/SEG12/SCK0/AVREF/EINT0/CS19
COM0		LED COM ports	Input	P20/(SEG0)
COM1				P21/(SEG1)
COM2				P22/(SEG2)/CS11
COM3				P23/(SEG3)EC1/CS12
COM4				P24/(SEG4)/CS13
COM5				P25/(SEG5)/EINT11/EC0/CS14
COM6				P26/(SEG6)/SXOUT/EINT10/CS15
COM7				P27/(SEG7)SXIN/T0D/PWM0O/CS16
SEG0	I/O	LED SEG ports	Input	P20/(COM0)
SEG1				P21/(COM1)
SEG2				P22/(COM2)/CS11
SEG3				P23/(COM3)EC1/CS12
SEG4				P24/(COM4)/CS13
SEG5				P25/(COM5)/EINT11/EC0/CS14
SEG6				P26/(COM6)/SXOUT/EINT10/CS15
SEG7				P27/(COM7)SXIN/T0D/PWM0O/CS16
SEG8				P07/EINT4/T5O/PWM5O/AN3/CS3
SEG9				P06/EINT3/EC3/T4O/PWM4O/AN2/CS2
SEG10				P05/EINT2/T3O/PWM3O/AN1/CS1
SEG11				P04/SS0/EINT1/AN0/CS0
SEG12				P03/BUZ0/SCK0/EINT0/AN7/AVREF/CS19
SEG13				P00/RESETB/TXD1/MOSI1/CS18
SEG14				P31/RXD1/MISO1/EINT8/CS17
CAPN	I/O	Modulation CAP	Input	P30

Table 3. Normal Pin Description (continued)

PIN Name	I/O	Function	@RESET	Shared with
CS0	I/O	Touch Switch Inputs	Input	P04/SEG11/SS0/EINT1/AN0
CS1				P05/SEG10/EINT2/T3O/PWM3O/AN1
CS2				P06/SEG9/EINT3/EC3/T4O/PWM4O/AN2
CS3				P07/SEG8/EINT4/T5O/PWM5O/AN3
CS4				P10/SEG15/AN4/(RXD0)/(MISO0)/(SCL0)
CS5				P11/EINT5/T1O/PWM1O/AN5/(TXD0)/(MOSI0)/(SDA0)
CS6				P12/EINT12/T2O/PWM2O/AN6
CS7				P14/SS1
CS8				P15/SCK1
CS9				P16/(RXD1)/(MISO1)
CS10				P17/(TXD1)/(MOSI1)
CS11				P22/COM2(SEG2)
CS12				P23/COM3(SEG3)/EC1
CS13				P24/COM4(SEG4)
CS14				P25/COM5(SEG5)/EINT11/EC0
CS15				P26/SXOUT/COM6(SEG6)/EINT10
CS16				P27/SXIN/COM7(SEG7)/T0O/PWM0O
CS17				P31/SEG14/RXD1/MISO1/EINT8
CS18				P00/RESETB/SEG13/TXD1/MOSI1
CS19				P03/BUZ0/SEG12/SCK0/EINT0/AN7/AVREF
RESETB	I/O	System reset pin with a pull-up resistor when it is selected as the RESETB by CONFIGURE OPTION	Input	P00/SEG13/TXD1/MOSI1/CS18
DSDA	I/O	In-system programming data input/output	Input	P01/RXD0/MISO0/SCL0/EC3
DSCL	I/O	In-system programming clock input	Input	P02/TXD0/MOSI0/SDA0/T3O/PWM3O
SXIN	I/O	Sub oscillator pins	Input	P27/T0O/PWM0O/COM7(SEG7)/CS16
SXOUT				P26/COM6(SEG6)/EINT10/CS15
VDD, VSS	–	Power input pins	–	–
VDDLED	–	Power input pin for LED	–	–

NOTES:

1. The P12–P15 are not in the 24-pin package.
2. The P10–P17 are not in the 20-pin package.
3. The P00/RESETB pin is configured as one of the P00 and RESETB pin by the “CONFIGURE OPTION.”
4. If the P01/EC3/MISO0/RXD0/SCL0/DSDA and P02/T3O/PWM3O/MOSI0/TXD0/SDA0/DSCL pins are connected to the programmer during power-on reset, the pins are automatically configured as In-system programming pins.
5. The P01/EC3/MISO0/RXD0/SCL0/DSDA and P02/T3O/PWM3O/MOSI0/TXD0/SDA0/DSCL pins are configured as inputs with internal pull-up resistor only during the reset or power-on reset.
6. The P00/RESETB/SEG13/TXD1/MOSI1/CS18, P27/T0O/PWM0O/COM7/CS16/SXIN, and P26/COM6/EINT10/CS15/SXOUT pins are configured as a function pin by software control.

3 Port Structures

3.1 General Purpose I/O Port

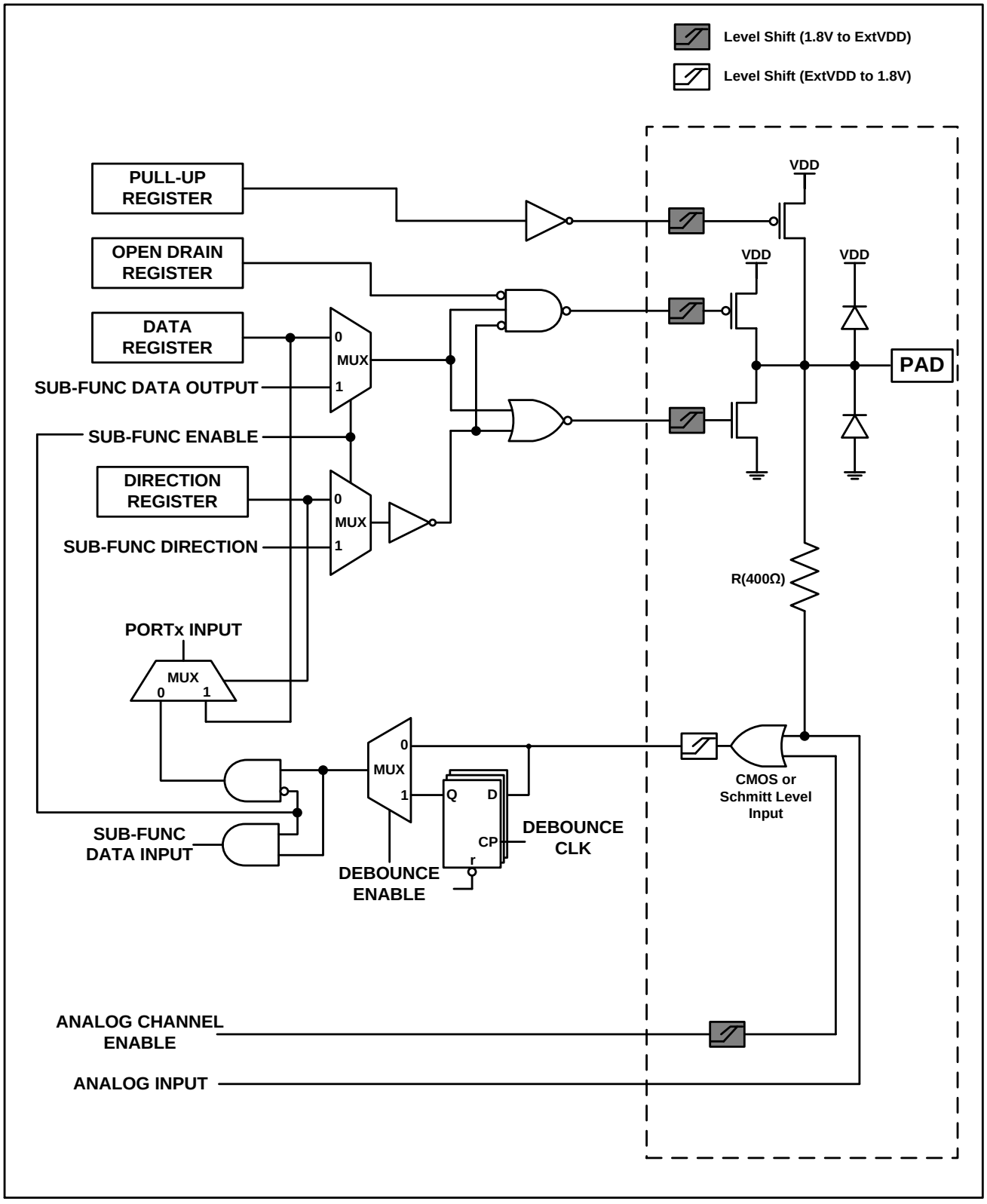


Figure 5. General Purpose I/O Port

3.2 SEG I/O Port

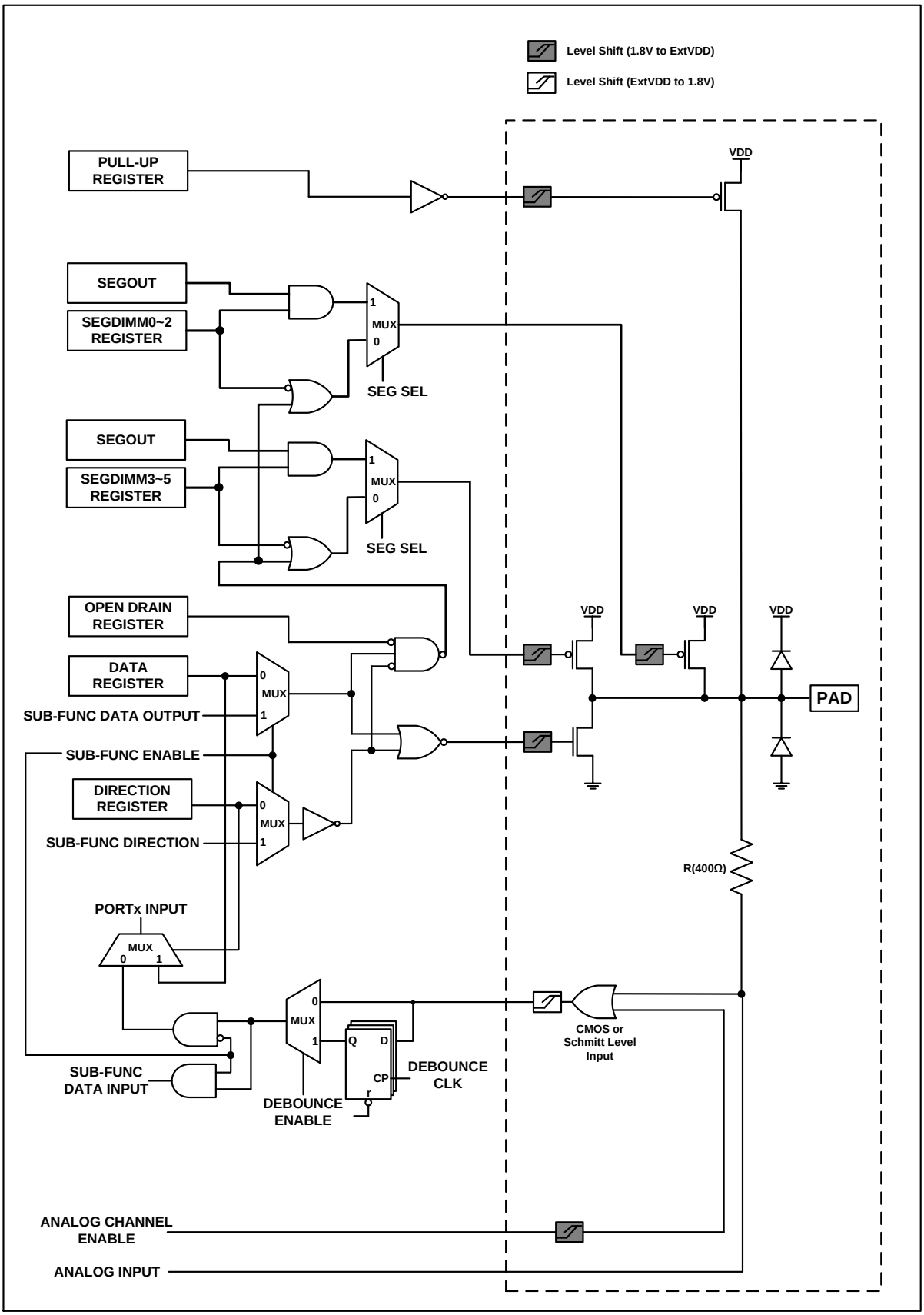


Figure 6. SEG I/O Port

3.3 COM & SEG I/O Port

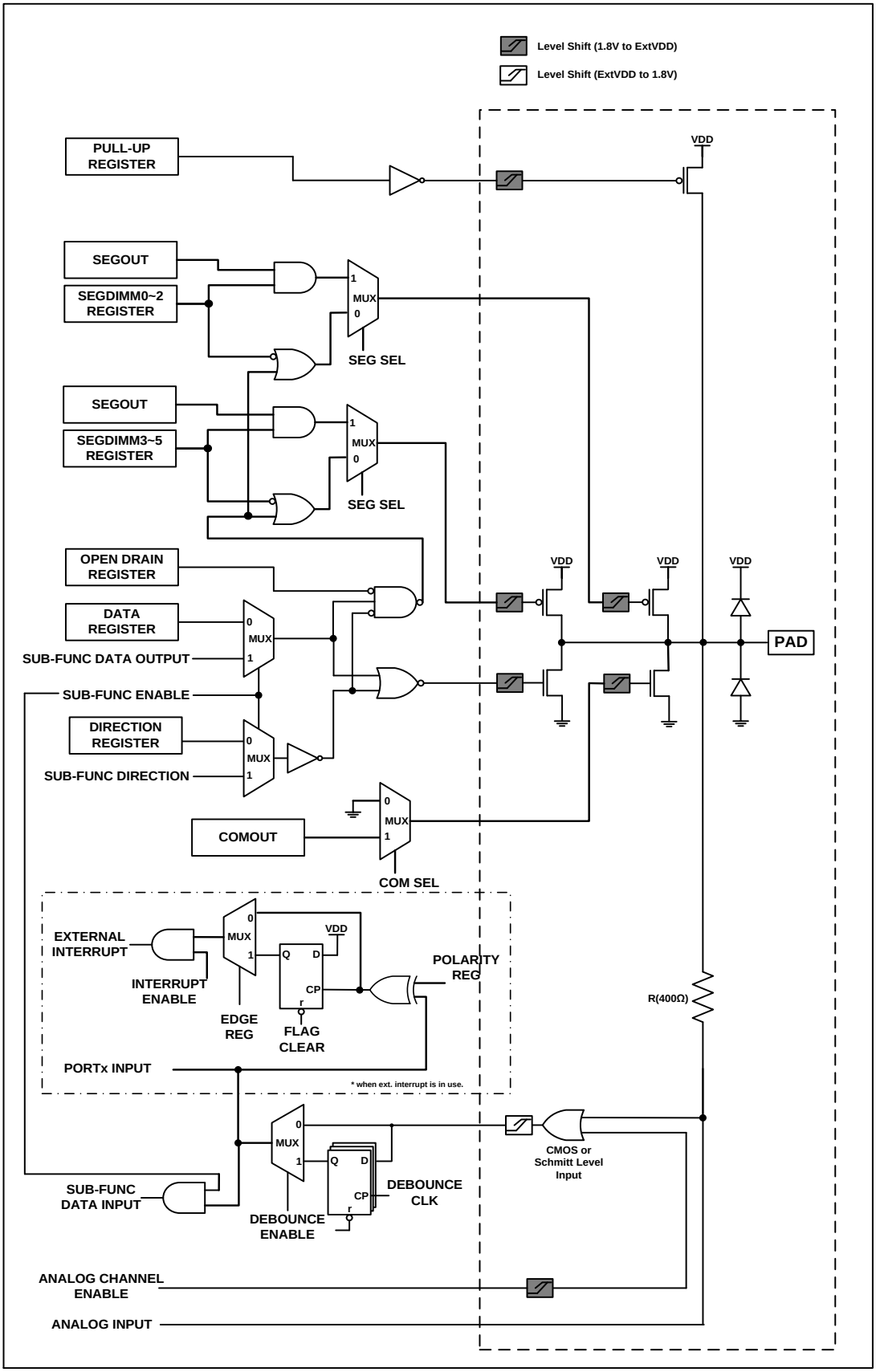


Figure 7. COM & SEG I/O Port

4 Memory organization

The A96T418 addresses two separate address memory stores:Program memory and Data memory. The logical separation of Program and Data memory allows Data memory to be accessed by 8-bit addresses, which makes the 8-bit CPU access the data memory more rapidly. Nevertheless, 16-bit Data memory addresses can also be generated through the DPTR register.

A96T418 provides on-chip 32Kbytes of the ISP type flash program memory, which can be read and written to. Internal data memory (IRAM) is 256bytes and it includes the stack area. External data memory (XRAM) is 1792bytes.

4.1 Program Memory

A 16-bit program counter is capable of addressing up to 64Kbytes, but this device has just 32Kbytes program memory space.

Figure 8 shows the map of the lower part of the program memory. After reset, the CPU begins execution from location 0000H. Each interrupt is assigned a fixed location in program memory. The interrupt causes the CPU to jump to that location, where it commences execution of the service routine. External interrupt 3, for example, is assigned to location 001BH. If external interrupt 3 is going to be used, its service routine must begin at location 001BH. If the interrupt is not going to be used, its service location is available as general purpose program memory. If an interrupt service routine is short enough (as is often the case in control applications), it can reside entirely within that 8bytes interval. Longer service routines can use a jump instruction to skip over subsequent interrupt locations, if other interrupts are in use.

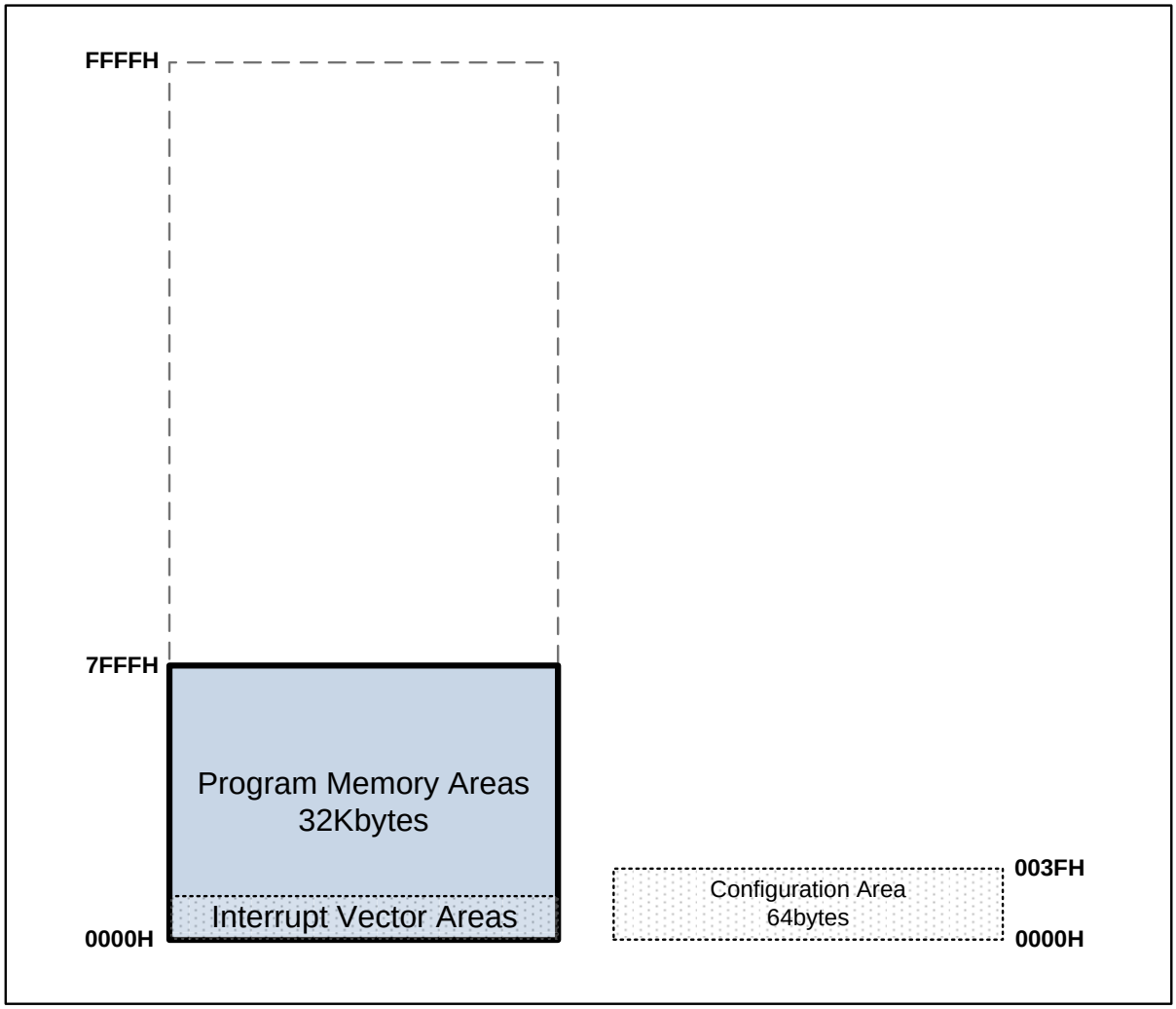


Figure 8. Program Memory

NOTES:

1. 32Kbytes Including Interrupt Vector Region

4.2 Data Memory

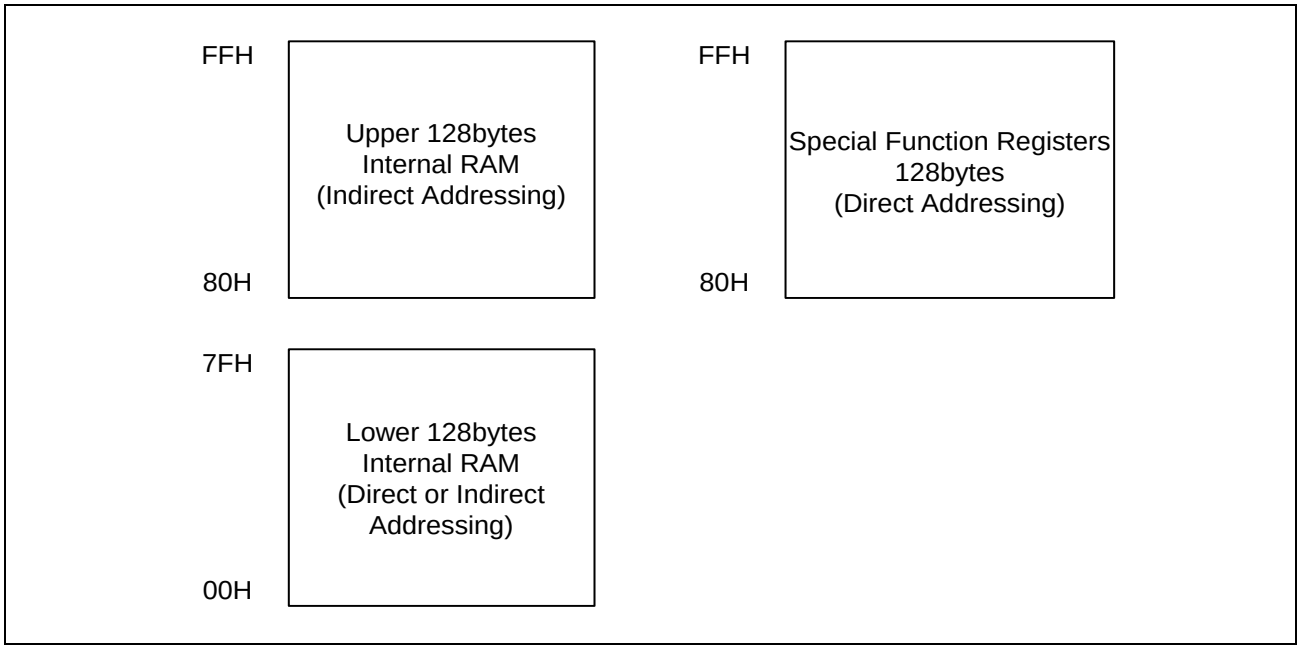


Figure 9. Data Memory Map

The internal data memory space is divided into three blocks, which are generally referred to as the lower 128bytes, upper 128bytes, and SFR space.

Internal data memory addresses are always one byte wide, which implies an address space of only 256bytes. However, in fact, the addressing modes for internal RAM can accommodate up to 384bytes by using a simple trick. Direct addresses higher than 7FH access one memory space and indirect addresses higher than 7FH access a different memory space. Thus Figure 9 shows the upper 128bytes and SFR space occupying the same block of addresses, 80H through FFH, although they are physically separate entities.

The lower 128bytes of RAM are present in all 8051 devices as mapped in Figure 10. The lowest 32bytes are grouped into 4 banks of 8 registers. Program instructions call out these registers as R0 through R7. Two bits in the Program Status Word select which register bank is in use. This allows more efficient use of code space, since register instructions are shorter than instructions that use direct addressing.

The next 16bytes above the register banks form a block of bit-addressable memory space. The 8051 instruction set includes a wide selection of single-bit instructions, and the 128 bits in this area can be directly addressed by these instructions. The bit addresses in this area are 00H through 7FH.

All of the bytes in the lower 128bytes can be accessed by either direct or indirect addressing. The upper 128bytes RAM can only be accessed by indirect addressing. These spaces are used for data RAM and stack.

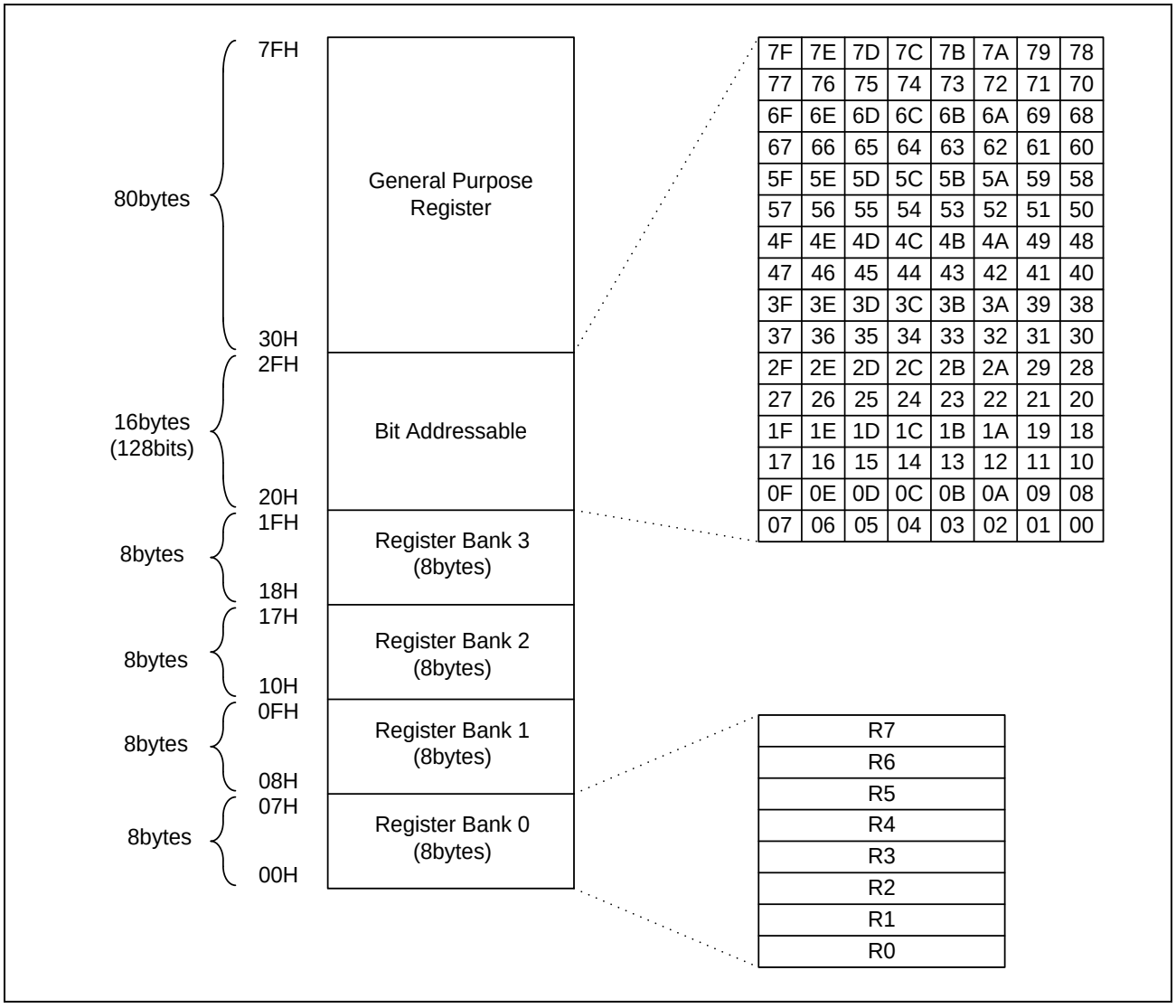


Figure 10. Lower 128bytes RAM

4.3 External Data Memory

A96T418 has 1792bytes XRAM and XSFR. This area has no relation with RAM/FLASH. It can be read and written to through SFR with 8-bit unit.

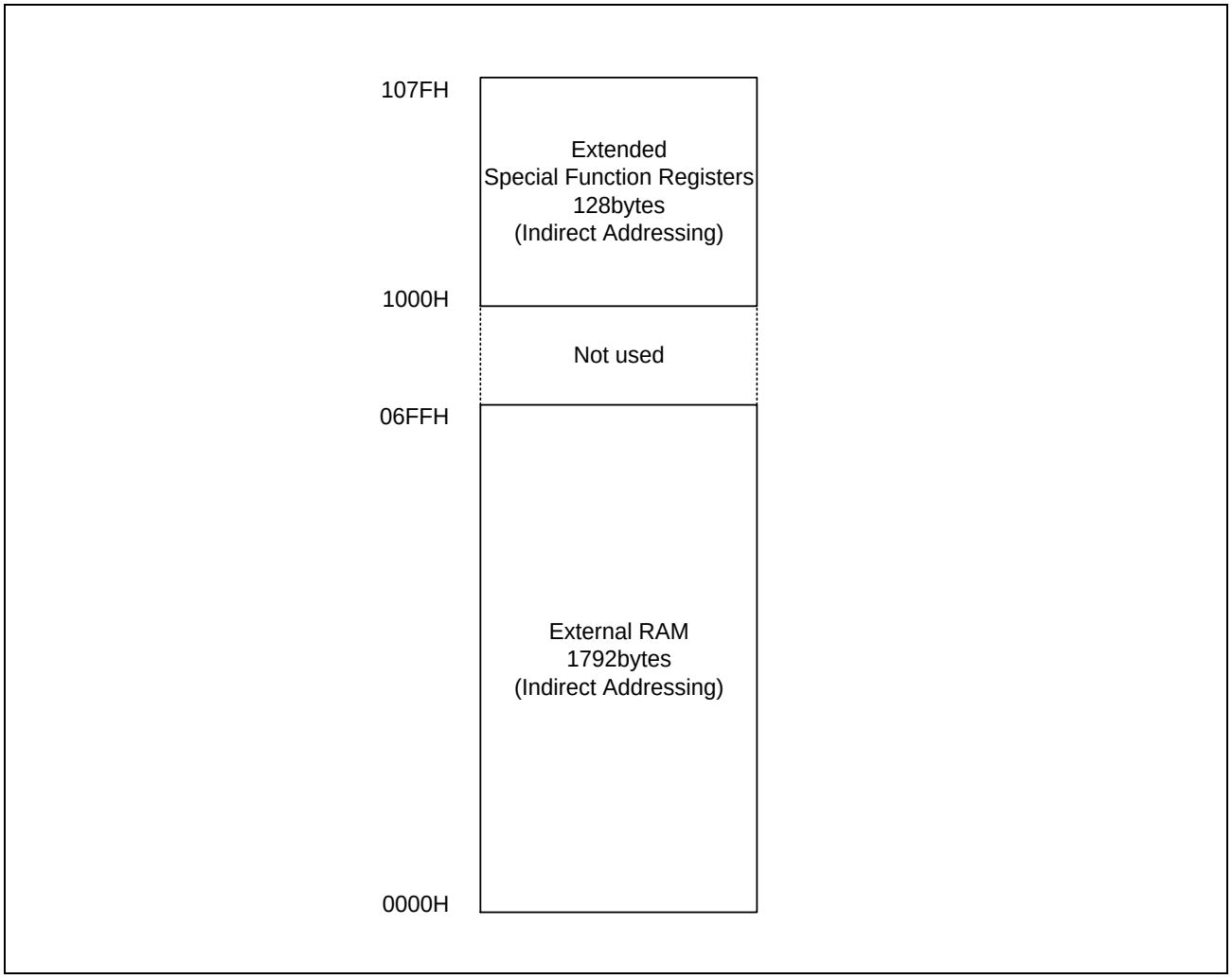


Figure 11. XDATA Memory Area

4.4 SFR Map

4.4.1 SFR Map Summary

Table 4. SFR Map Summary

- Reserved
- M8051 compatible

	00H/8H(1)	01H/9H	02H/0AH	03H/0BH	04H/0CH	05H/0DH	06H/0EH	07H/0FH
0F8H	IP1	–	–	–	UBAUD	UDATA	–	–
0F0H	B	–	–	–	–	–	–	–
0E8H	RSTFR	–	–	–	–	–	P3FSR	–
0E0H	ACC	USI0ST1	USI0ST2	USI0BD	USI0SDHR	USI0DR	USI0SCLR	USI0SCHR
0D8H	LVRCR	USI0CR1	USI0CR2	USI0CR3	USI0CR4	USI0SAR	P0DB	P123DB
0D0H	PSW	–	P0FSRL	P0FSRH	P1FSRL	P1FSRH	P2FSRL	P2FSRH
0C8H	OSCCR	–	–	UCTRL1	UCTRL2	UCTRL3	–	USTAT
0C0H	EIFLAG0	P3IO	T2CRL	T2CRH	T2ADRL	T2ADRH	T2BDRL	T2BDRH
0B8H	IP	P2IO	T1CRL	T1CRH	T1ADRL	T1ADRH	T1BDRL	T1BDRH
0B0H	–	P1IO	T0CR	T0CNT	T0DR/ T0CDR	–	–	–
0A8H	IE	IE1	IE2	IE3	P0PU	P1PU	P2PU	P3PU
0A0H	–	P0IO	EO	–	EIPOL0L	EIPOL0H	EIFLAG1	EIPOL1
98H	P3	–	–	–	ADCCRL	ADCCRH	ADCDRL	ADCDRH
90H	P2	P0OD	P1OD	P2OD	–	–	WTCR	BUZCR
88H	P1	WTDR/ WTCNT	SCCR	BITCR	BITCNT	WDTCR	WDTDR/ WDTCNT	BUZDR
80H	P0	SP	DPL	DPH	DPL1	DPH1	LVICR	PCON

NOTES:

1. 00H/8H, These registers are bit-addressable.

Table 5. XSFR Map Summary

	00H/8H[1]	01H/9H	02H/0AH	03H/0BH	04H/0CH	05H/0DH	06H/0EH	07H/0FH
1078H	–	–	–	–	–	–	–	–
1070H	–	–	–	–	–	–	–	–
1068H	–	–	–	–	–	–	–	–
1060H	–	–	–	–	–	–	–	–
1058H	–	–	–	–	–	–	–	–
1050H	–	–	–	–	–	–	–	–
1048H	–	–	–	–	–	–	–	–
1040H	–	–	–	–	–	–	–	–
1038H	–	–	–	–	–	–	–	–
1030H	–	–	–	–	–	–	–	–
1028H	FEARH	FEARM	FEARL	FEDR	FETR	–	–	–
1020H	FEMR	FECR	FESR	FETCR	FEARM1	FEARL1	–	–
1018H	UCTRL4	FPCR	RTOCH	RTOCL	–	–	–	–
1010H	T5CRH	T5CRL	T5ADRH	T5ADRL	T5BDRH	T5BDRL	–	–
1008H	T4CRH	T4CRL	T4ADRH	T4ADRL	T4BDRH	T4BDRL	–	–
1000H	T3CRH	T3CRL	T3ADRH	T3ADRL	T3BDRH	T3BDRL	–	–

4.4.2 SFR Map

Table 6. SFR Map

Address	Function	Symbol	R/W	@Reset							
				7	6	5	4	3	2	1	0
80H	P0 Data Register	P0	R/W	0	0	0	0	0	0	0	0
81H	Stack Pointer	SP	R/W	0	0	0	0	0	1	1	1
82H	Data Pointer Register Low	DPL	R/W	0	0	0	0	0	0	0	0
83H	Data Pointer Register High	DPH	R/W	0	0	0	0	0	0	0	0
84H	Data Pointer Register Low 1	DPL1	R/W	0	0	0	0	0	0	0	0
85H	Data Pointer Register High 1	DPH1	R/W	0	0	0	0	0	0	0	0
86H	Low Voltage Indicator Control Register	LVICR	R/W	–	–	0	0	0	0	0	0
87H	Power Control Register	PCON	R/W	0	–	–	–	0	0	0	0
88H	P1 Data Register	P1	R/W	0	0	0	0	0	0	0	0
89H	Watch Timer Data Register	WTDR	W	0	1	1	1	1	1	1	1
	Watch Timer Counter Register	WTCNT	R	–	0	0	0	0	0	0	0
8AH	System and Clock Control Register	SCCR	R/W	–	–	–	–	–	–	0	0
8BH	Basic Interval Timer Control Register	BITCR	R/W	0	1	0	0	0	1	0	1
8CH	Basic Interval Timer Counter Register	BITCNT	R	0	0	0	0	0	0	0	0
8DH	Watch Dog Timer Control Register	WDTCR	R/W	0	0	0	–	–	–	0	0
8EH	Watch Dog Timer Data Register	WDTDR	W	1	1	1	1	1	1	1	1
	Watch Dog Timer Counter Register	WDTCNT	R	0	0	0	0	0	0	0	0
8FH	BUZZER Data Register	BUZDR	R/W	1	1	1	1	1	1	1	1
90H	P2 Data Register	P2	R/W	0	0	0	0	0	0	0	0
91H	P0 Open-drain Selection Register	P0OD	R/W	0	0	0	0	0	0	0	0
92H	P1 Open-drain Selection Register	P1OD	R/W	0	0	0	0	0	0	0	0
93H	P2 Open-drain Selection Register	P2OD	R/W	0	0	0	0	0	0	0	0
94H	Reserved	–	–	–	–	–	–	–	–	–	–
95H	Reserved	–	–	–	–	–	–	–	–	–	–
96H	Watch Timer Control Register	WTCR	R/W	0	–	–	0	0	0	0	0
97H	BUZZER Control Register	BUZCR	R/W	–	–	–	–	–	0	0	0
98H	P3 Data Register	P3	R/W	–	–	–	–	–	–	0	0
99H	Reserved	–	–	–	–	–	–	–	–	–	–
9AH	Reserved	–	–	–	–	–	–	–	–	–	–
9BH	Reserved	–	–	–	–	–	–	–	–	–	–
9CH	A/D Converter Control Low Register	ADCCRL	R/W	0	0	0	0	–	0	0	0
9DH	A/D Converter Control High Register	ADCCRH	R/W	0	0	0	0	0	0	0	1
9EH	A/D Converter Data Low Register	ADCDRL	R	0	0	0	0	0	0	0	0
9FH	A/D Converter Data High Register	ADCDRH	R	0	0	0	0	0	0	0	0

Table 5. SFR Map (Continued)

Address	Function	Symbol	R/W	@Reset							
				7	6	5	4	3	2	1	0
A0H	Reserved	–	–	–	–	–	–	–	–	–	–
A1H	P0 Direction Register	P0IO	R/W	0	0	0	0	0	0	0	0
A2H	Extended Operation Register	EO	R/W	–	–	–	0	–	0	0	0
A3H	Reserved	–	–	–	–	–	–	–	–	–	–
A4H	External Interrupt Polarity 0 Low Register	EIPOL0L	R/W	0	0	0	0	0	0	0	0
A5H	External Interrupt Polarity 0 High Register	EIPOL0H	R/W	–	–	–	–	0	0	0	0
A6H	External Interrupt Flag 1 Register	EIFLAG1	R/W	0	0	–	–	0	0	0	0
A7H	External Interrupt Polarity 1 Register	EIPOL1	R/W	0	0	0	0	0	0	0	0
A8H	Interrupt Enable Register	IE	R/W	0	–	0	0	0	0	0	0
A9H	Interrupt Enable Register 1	IE1	R/W	–	–	0	0	0	0	–	0
AAH	Interrupt Enable Register 2	IE2	R/W	–	–	0	0	0	0	0	0
ABH	Interrupt Enable Register 3	IE3	R/W	–	–	0	0	0	0	0	0
ACH	P0 Pull-up Resistor Selection Register	P0PU	R/W	0	0	0	0	0	0	0	0
ADH	P1 Pull-up Resistor Selection Register	P1PU	R/W	0	0	0	0	0	0	0	0
AEH	P2 Pull-up Resistor Selection Register	P2PU	R/W	0	0	0	0	0	0	0	0
AFH	P3 Pull-up Resistor Selection Register	P3PU	R/W	–	–	–	–	–	–	0	0
B0H	Reserved	–	–	–	–	–	–	–	–	–	–
B1H	P1 Direction Register	P1IO	R/W	0	0	0	0	0	0	0	0
B2H	Timer 0 Control Register	T0CR	R/W	0	–	0	0	0	0	0	0
B3H	Timer 0 Counter Register	T0CNT	R	0	0	0	0	0	0	0	0
B4H	Timer 0 Data Register	T0DR	R/W	1	1	1	1	1	1	1	1
	Timer 0 Capture Data Register	T0CDR	R	0	0	0	0	0	0	0	0
B5H	Reserved	–	–	–	–	–	–	–	–	–	–
B6H	Reserved	–	–	–	–	–	–	–	–	–	–
B7H	Reserved	–	–	–	–	–	–	–	–	–	–
B8H	Interrupt Priority Register	IP	R/W	–	–	0	0	0	0	0	0
B9H	P2 Direction Register	P2IO	R/W	0	0	0	0	0	0	0	0
BAH	Timer 1 Control Low Register	T1CRL	R/W	0	0	0	0	–	0	0	0
BBH	Timer 1 Counter High Register	T1CRH	R/W	0	–	0	0	–	–	–	0
BCH	Timer 1 A Data Low Register	T1ADRL	R/W	1	1	1	1	1	1	1	1
BDH	Timer 1 A Data High Register	T1ADRH	R/W	1	1	1	1	1	1	1	1
BEH	Timer 1 B Data Low Register	T1BDRL	R/W	1	1	1	1	1	1	1	1
BFH	Timer 1 B Data High Register	T1BDRH	R/W	1	1	1	1	1	1	1	1

Table 5. SFR Map (Continued)

Address	Function	Symbol	R/W	@Reset							
				7	6	5	4	3	2	1	0
C0H	External Interrupt Flag 0 Register	EIFLAG0	R/W	–	–	0	0	0	0	0	0
C1H	P3 Direction Register	P3IO	R/W	–	–	–	–	–	–	0	0
C2H	Timer 2 Control Low Register	T2CRL	R/W	0	0	0	0	–	0	–	0
C3H	Timer 2 Control High Register	T2CRH	R/W	0	–	0	0	–	–	–	0
C4H	Timer 2 A Data Low Register	T2ADRL	R/W	1	1	1	1	1	1	1	1
C5H	Timer 2 A Data High Register	T2ADRH	R/W	1	1	1	1	1	1	1	1
C6H	Timer 2 B Data Low Register	T2BDRL	R/W	1	1	1	1	1	1	1	1
C7H	Timer 2 B Data High Register	T2BDRH	R/W	1	1	1	1	1	1	1	1
C8H	Oscillator Control Register	OSCCR	R/W	0	0	1	0	1	0	–	0
C9H	Reserved	–	–	–	–	–	–	–	–	–	–
CAH	Reserved	–	–	–	–	–	–	–	–	–	–
CBH	USART Control Register 1	UCTRL1	R/W	0	0	0	0	0	0	0	0
CCH	USART Control Register 2	UCTRL2	R/W	0	0	0	0	0	0	0	0
CDH	USART Control Register 3	UCTRL3	R/W	0	0	0	0	–	0	0	0
CEH	Reserved	–	–	–	–	–	–	–	–	–	–
CFH	USART Status Register	USTAT	R/W	1	0	0	0	0	0	0	0
D0H	Program Status Word Register	PSW	R/W	0	0	0	0	0	0	0	0
D1H	Reserved	-	-	-	-	-	-	-	-	-	-
D2H	P0 Function Selection Low Register	P0FSRL	R/W	0	0	0	0	0	0	0	0
D3H	P0 Function Selection High Register	P0FSRH	R/W	0	0	0	0	0	0	0	0
D4H	P1 Function Selection Low Register	P1FSRL	R/W	0	0	0	0	0	0	0	0
D5H	P1 Function Selection High Register	P1FSRH	R/W	0	0	0	0	0	0	0	0
D6H	P2 Function Selection Low Register	P2FSRL	R/W	0	0	0	0	0	0	0	0
D7H	P2 Function Selection High Register	P2FSRH	R/W	0	0	0	0	0	0	0	0
D8H	Low Voltage Reset Control Register	LVRCR	R/W	–	–	–	0	0	0	0	0
D9H	USI0 Control Register 1	USI0CR1	R/W	0	0	0	0	0	0	0	0
DAH	USI0 Control Register 2	USI0CR2	R/W	0	0	0	0	0	0	0	0
DBH	USI0 Control Register 3	USI0CR3	R/W	0	0	0	0	0	0	0	0
DCH	USI0 Control Register 4	USI0CR4	R/W	0	–	0	0	0	0	0	0
DDH	USI0 Slave Address Register	USI0SAR	R/W	0	0	0	0	0	0	0	0
DEH	P0 De-bounce Enable Register	P0DB	R/W	0	0	–	0	0	0	0	0
DFH	P1/P2/P3 De-bounce Enable Register	P123DB	R/W	–	–	–	0	0	0	0	0

Table 5. SFR Map (Continued)

Address	Function	Symbol	R/W	@Reset							
				7	6	5	4	3	2	1	0
E0H	Accumulator Register	ACC	R/W	0	0	0	0	0	0	0	0
E1H	USI0 Status Register 1	USI0ST1	R/W	1	0	0	0	0	0	0	0
E2H	USI0 Status Register 2	USI0ST2	R	0	0	0	0	0	0	0	0
E3H	USI0 Baud Rate Generation Register	USI0BD	R/W	1	1	1	1	1	1	1	1
E4H	USI0 SDA Hold Time Register	USI0SHDR	R/W	0	0	0	0	0	0	0	1
E5H	USI0 Data Register	USI0DR	R/W	0	0	0	0	0	0	0	0
E6H	USI0 SCL Low Period Register	USI0SCLR	R/W	0	0	1	1	1	1	1	1
E7H	USI0 SCL High Period Register	USI0SCHR	R/W	0	0	1	1	1	1	1	1
E8H	Reset Flag Register	RSTFR	R/W	1	x	0	0	x	–	–	–
E9H	Reserved	–	–	–	–	–	–	–	–	–	–
EAH	Reserved	–	–	–	–	–	–	–	–	–	–
EBH	Reserved	–	–	–	–	–	–	–	–	–	–
ECH	Reserved	–	–	–	–	–	–	–	–	–	–
EDH	Reserved	–	–	–	–	–	–	–	–	–	–
EEH	P3 Function Selection Register	P3FSR	R/W	–	–	–	–	0	0	0	0
EFH	Reserved	–	–	–	–	–	–	–	–	–	–
F0H	B Register	B	R/W	0	0	0	0	0	0	0	0
F1H	Reserved	–	–	–	–	–	–	–	–	–	–
F2H	Reserved	–	–	–	–	–	–	–	–	–	–
F3H	Reserved	–	–	–	–	–	–	–	–	–	–
F4H	Reserved	–	–	–	–	–	–	–	–	–	–
F5H	Reserved	–	–	–	–	–	–	–	–	–	–
F6H	Reserved	–	–	–	–	–	–	–	–	–	–
F7H	Reserved	–	–	–	–	–	–	–	–	–	–
F8H	Interrupt Priority Register 1	IP1	R/W	–	–	0	0	0	0	0	0
F9H	Reserved	–	–	–	–	–	–	–	–	–	–
FAH	Reserved	–	–	–	–	–	–	–	–	–	–
FBH	Reserved	–	–	–	–	–	–	–	–	–	–
FCH	USART Baud Rate Generation Register	UBAUD	R/W	1	1	1	1	1	1	1	1
FDH	USART Data Register	UDATA	R/W	0	0	0	0	0	0	0	0
FEH	Reserved	–	–	–	–	–	–	–	–	–	–
FFH	Reserved	–	–	–	–	–	–	–	–	–	–

Table 7. XSFR Map

Address	Function	Symbol	R/W	@Reset							
				7	6	5	4	3	2	1	0
1000H	Timer 3 Control High Register	T3CRH	R/W	0	–	0	0	–	–	–	0
1001H	Timer 3 Control Low Register	T3CRL	R/W	0	0	0	0	–	0	0	0
1002H	Timer 3 A Data High Register	T3ADRH	R/W	1	1	1	1	1	1	1	1
1003H	Timer 3 A Data Low Register	T3ADRL	R/W	1	1	1	1	1	1	1	1
1004H	Timer 3 B Data High Register	T3BDRH	R/W	1	1	1	1	1	1	1	1
1005H	Timer 3 B Data Low Register	T3BDRL	R/W	1	1	1	1	1	1	1	1
1006H	Reserved	–	–	–	–	–	–	–	–	–	–
1007H	Reserved	–	–	–	–	–	–	–	–	–	–
1008H	Timer 4 Control High Register	T4CRH	R/W	0	–	0	0	–	–	–	0
1009H	Timer 4 Control Low Register	T4CRL	R/W	0	0	0	0	–	0	–	0
100AH	Timer 4 A Data High Register	T4ADRH	R/W	1	1	1	1	1	1	1	1
100BH	Timer 4 A Data Low Register	T4ADRL	R/W	1	1	1	1	1	1	1	1
100CH	Timer 4 B Data High Register	T4BDRH	R/W	1	1	1	1	1	1	1	1
100DH	Timer 4 B Data Low Register	T4BDRL	R/W	1	1	1	1	1	1	1	1
100EH	Reserved	–	–	–	–	–	–	–	–	–	–
100FH	Reserved	–	–	–	–	–	–	–	–	–	–
1010H	Timer 5 Control High Register	T5CRH	R/W	0	–	0	0	–	–	–	0
1011H	Timer 5 Control Low Register	T5CRL	R/W	0	0	0	0	–	0	–	0
1012H	Timer 5 A Data High Register	T5ADRH	R/W	1	1	1	1	1	1	1	1
1013H	Timer 5 A Data Low Register	T5ADRL	R/W	1	1	1	1	1	1	1	1
1014H	Timer 5 B Data High Register	T5BDRH	R/W	1	1	1	1	1	1	1	1
1015H	Timer 5 B Data Low Register	T5BDRL	R/W	1	1	1	1	1	1	1	1
1016H	Reserved	–	–	–	–	–	–	–	–	–	–
1017H	Reserved	–	–	–	–	–	–	–	–	–	–
1018H	USART Control Register 4	UCTRL4	R/W	–	–	–	0	0	0	0	0
1019H	USART Floating Point Counter	FPCR	R/W	0	0	0	0	0	0	0	0
101AH	Receiver Time Out Counter High Register	RTOCH	R	0	0	0	0	0	0	0	0
101BH	Receiver Time Out Counter Low Register	RTOCL	R	0	0	0	0	0	0	0	0
101CH	Reserved	–	–	–	–	–	–	–	–	–	–
101DH	Reserved	–	–	–	–	–	–	–	–	–	–
101EH	Reserved	–	–	–	–	–	–	–	–	–	–
101FH	Reserved	–	–	–	–	–	–	–	–	–	–

Table 6. XSFR Map (Continued)

Address	Function	Symbol	R/W	@Reset							
				7	6	5	4	3	2	1	0
1020H	Flash Mode Register	FEMR	R/W	0	–	0	0	0	0	0	0
1021H	Flash Control Register	FECR	R/W	0	–	0	0	0	0	1	1
1022H	Flash Status Register	FESR	R/W	1	–	–	–	0	0	0	0
1023H	Flash Time Control Register	FETCR	R/W	0	0	0	0	0	0	0	0
1024H	Flash Address Middle Register 1	FEARM1	R/W	0	0	0	0	0	0	0	0
1025H	Flash Address Low Register 1	FEARL1	R/W	0	0	0	0	0	0	0	0
1026H	Reserved	–	–	–	–	–	–	–	–	–	–
1027H	Reserved	–	–	–	–	–	–	–	–	–	–
1028H	Flash Address High Register	FEARH	R/W	0	0	0	0	0	0	0	0
1029H	Flash Address Middle Register	FEARM	R/W	0	0	0	0	0	0	0	0
102AH	Flash Address Low Register	FEARL	R/W	0	0	0	0	0	0	0	0
102BH	Flash Data Register	FEDR	R/W	0	0	0	0	0	0	0	0
102CH	Flash Test Register	FETR	R/W	0	0	0	0	0	0	0	0
102DH	Reserved	–	–	–	–	–	–	–	–	–	–
102EH	Reserved	–	–	–	–	–	–	–	–	–	–
102FH	Reserved	–	–	–	–	–	–	–	–	–	–
1030H	Reserved	–	–	–	–	–	–	–	–	–	–
1031H	Reserved	–	–	–	–	–	–	–	–	–	–
1032H	Reserved	–	–	–	–	–	–	–	–	–	–
1033H	Reserved	–	–	–	–	–	–	–	–	–	–
1034H	Reserved	–	–	–	–	–	–	–	–	–	–
1035H	Reserved	–	–	–	–	–	–	–	–	–	–
1036H	Reserved	–	–	–	–	–	–	–	–	–	–
1037H	Reserved	–	–	–	–	–	–	–	–	–	–

5 I/O Ports

5.1 P0 Port

5.1.1 P0 Port Description

P0 is 8-bit I/O port. P0 control registers consist of P0 data register (P0), P0 direction register (P0IO), de-bounce enable register (P0DB), P0 pull-up resistor selection register (P0PU), and P0 open-drain selection register (P0OD). Refer to the port function selection registers for the P0 function selection.

5.2 P1 Port

5.2.1 P1 Port Description

P1 is 8-bit I/O port. P1 control registers consist of P1 data register (P1), P1 direction register (P1IO), debounce enble register (P123DB), P1 pull-up resistor selection register (P1PU), and P1 open-drain selection register (P1OD). Refer to the port function selection registers for the P1 function selection.

5.3 P2 Port

5.3.1 P2 Port Description

P2 is 8-bit I/O port. P2 control registers consist of P2 data register (P2), P2 direction register (P2IO), P2 pull-up resistor selection register (P2PU) and P2 open-drain selection register (P2OD). Refer to the port function selection registers for the P2 function selection.

5.4 P3 Port

5.4.1 P3 Port Description

P3 is 2-bit I/O port. P3 control registers consist of P3 data register (P3), P3 direction register (P3IO) and P3 pull-up resistor selection register (P3PU). Refer to the port function selection registers for the P3 function selection.

6 Interrupt Controller

6.1 Overview

The A96T418 supports up to 23 interrupt sources. The interrupts have separate enable register bits associated with them, allowing software control. They can also have four levels of priority assigned to them. The non-maskable interrupt source is always enabled with a higher priority than any other interrupt source, and is not controllable by software. The interrupt controller has following features:

Receive the request from 23 interrupt source

6 group priority

4 priority levels

Multi Interrupt possibility

If the requests of different priority levels are received simultaneously, the request of higher priority level is served first.

Each interrupt source can be controlled by EA bit and each IEx bit

Interrupt latency: 3~9 machine cycles in single interrupt system

The non-maskable interrupt is always enabled. The maskable interrupts are enabled through four pair of interrupt enable registers (IE, IE1, IE2, and IE3). Each bit of IE, IE1, IE2, IE3 register individually enables/disables the corresponding interrupt source. Overall control is provided by bit 7 of IE (EA). When EA is set to ‘0’, all interrupts are disabled: when EA is set to ‘1’, interrupts are individually enabled or disabled through the other bits of the interrupt enable registers. The EA bit is always cleared to ‘0’ jumping to an interrupt service vector and set to ‘1’ executing the [RETI] instruction. The A96T418 supports a four-level priority scheme. Each maskable interrupt is individually assigned to one of four priority levels according to IP and IP1.

Default interrupt mode is level-trigger mode basically, but if needed, it is possible to change to edge-trigger mode. Table 8 shows the Interrupt Group Priority Level that is available for sharing interrupt priority. Priority of a group is set by two bits of interrupt priority registers (one bit from IP, another one from IP1). Interrupt service routine serves higher priority interrupt first. If two requests of different priority levels are received simultaneously, the request of higher priority level is served prior to the lower one.

Table 8. Interrupt Group Priority Level

Interrupt Group	Highest → Lowest			
0 (Bit0)	Interrupt 0	Interrupt 6	Interrupt 12	Interrupt 18
1 (Bit1)	Interrupt 1	Interrupt 7	Interrupt 13	Interrupt 19
2 (Bit2)	Interrupt 2	Interrupt 8	Interrupt 14	Interrupt 20
3 (Bit3)	Interrupt 3	Interrupt 9	Interrupt 15	Interrupt 21
4 (Bit4)	Interrupt 4	Interrupt 10	Interrupt 16	Interrupt 22
5 (Bit5)	Interrupt 5	Interrupt 11	Interrupt 17	Interrupt 23

Highest

Lowest

6.2 External Interrupt

The external interrupt on INT0, INT1, INT5, INT6 and INT11 receive various interrupt request depending on the external interrupt polarity 0 high/low register (EIPOL0H/L) and external interrupt polarity 1 register (EIPOL1) as shown in Figure 12. Also each external interrupt source has enable/disable bits.The External interrupt flag 0 register (EIFLAG0) and external interrupt flag 1 register 1 (EIFLAG1) provides the status of external interrupts.

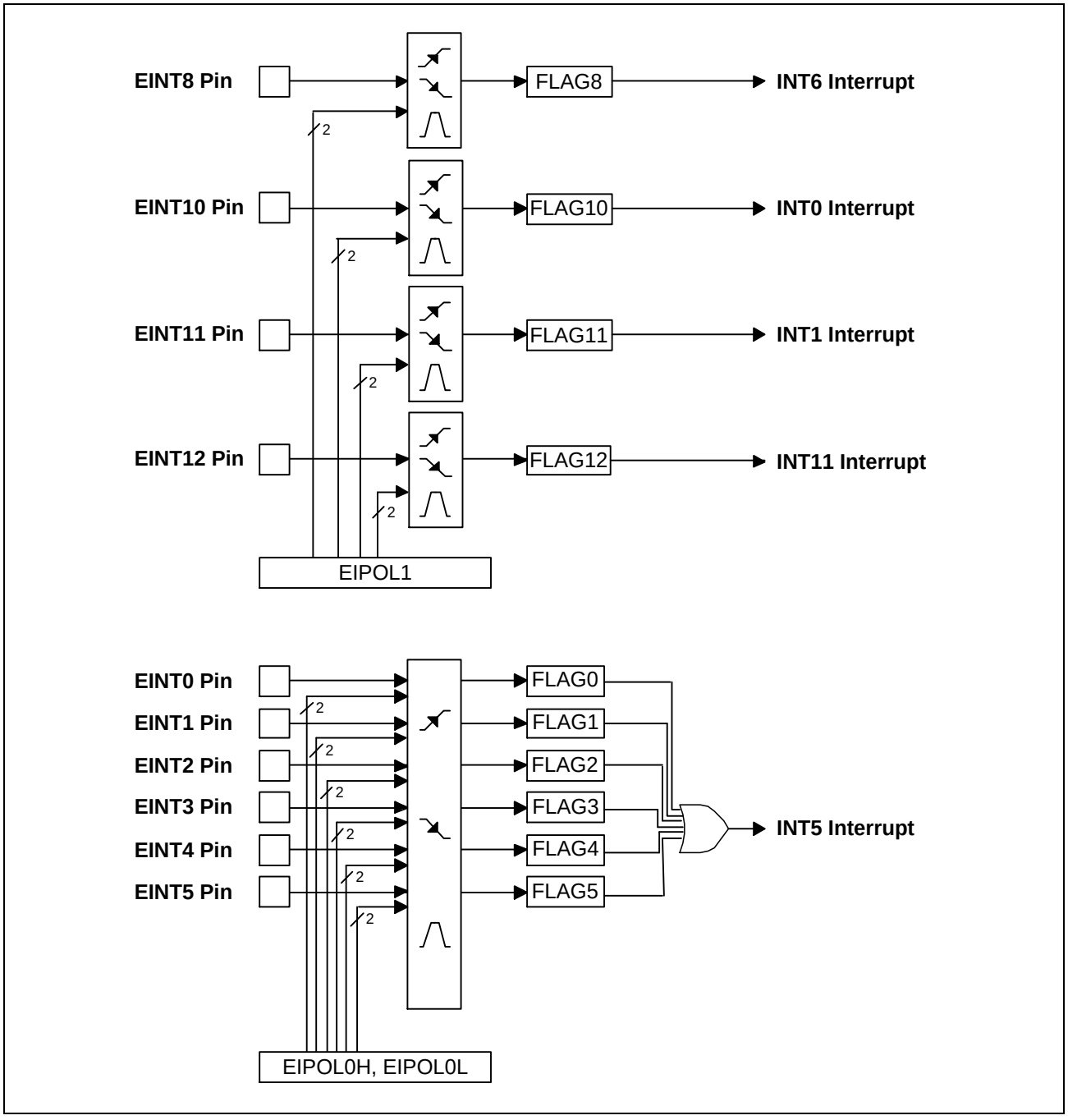


Figure 12. External Interrupt Description

6.3 Block Diagram

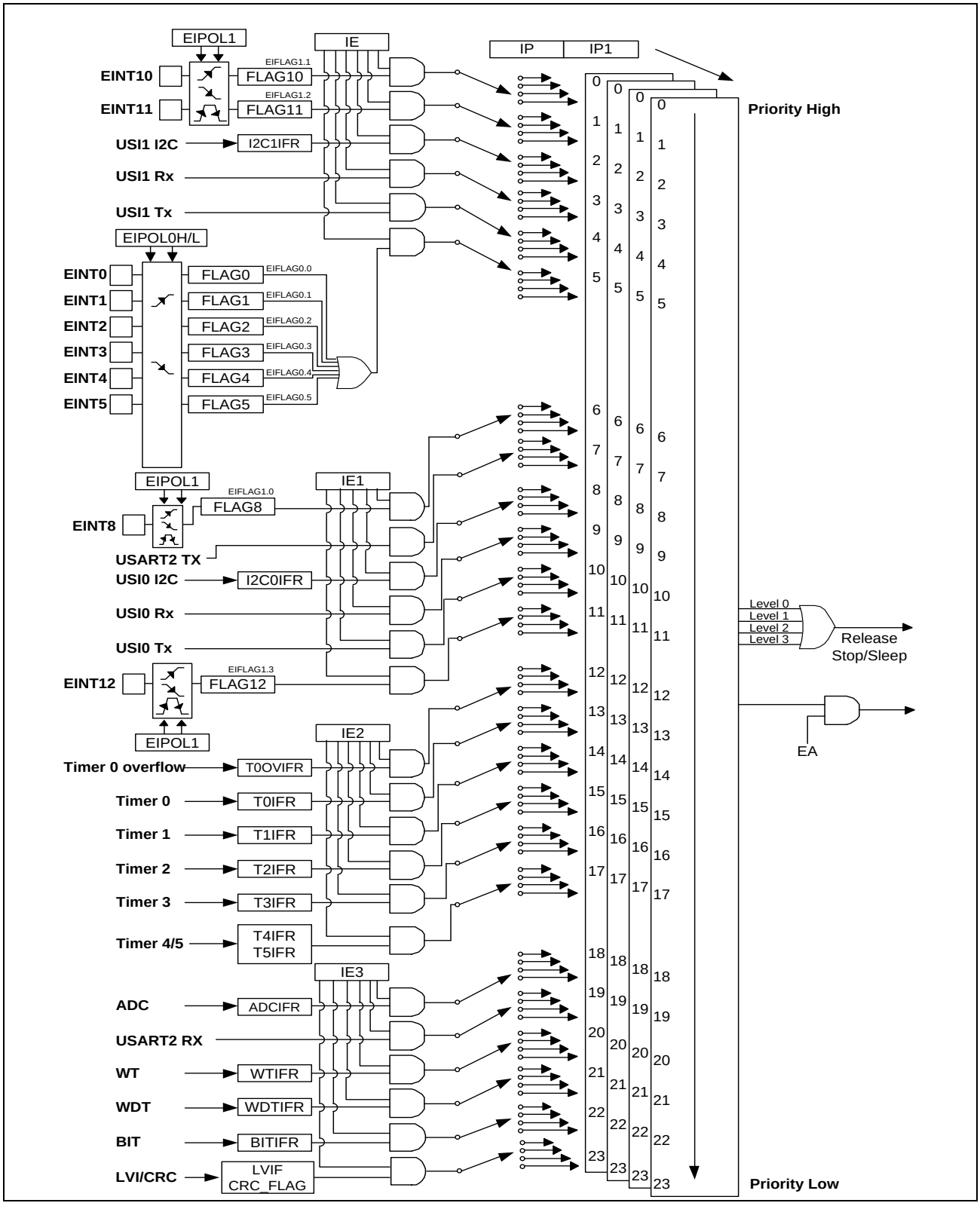


Figure 13. Block Diagram of Interrupt

NOTES:

1. The release signal for stop/idle mode may be generated by all interrupt sources which are enabled without reference to the priority level.
2. An interrupt request is delayed while data are written to IE, IE1, IE2, IE3, IP, IP1, and PCON register.

6.4 Interrupt Vector Table

The interrupt controller supports 23 interrupt sources as shown in the Table 9. When interrupt is served, long call instruction (LCALL) is executed and program counter jumps to the vector address. All interrupt requests have their own priority order.

Table 9. Interrupt Vector Address Table

Interrupt Source	Symbol	Interrupt Enable Bit	Polarity	Mask	Vector Address
Hardware Reset	RESETB	-	0	Non-Maskable	0000H
External Interrupt 10	INT0	IE.0	1	Maskable	0003H
External Interrupt 11	INT1	IE.1	2	Maskable	000BH
LED Interrupt	INT2	IE.2	3	Maskable	0013H
Touch Interrupt	INT3	IE.3	4	Maskable	001BH
Reserved	INT4	IE.4	5	Maskable	0023H
External Interrupt 0 – 5	INT5	IE.5	6	Maskable	002BH
External Interrupt 8	INT6	IE1.0	7	Maskable	0033H
USART1 TX Interrupt	INT7	IE1.1	8	Maskable	003BH
USI0 I2C Interrupt	INT8	IE1.2	9	Maskable	0043H
USI0 RX Interrupt	INT9	IE1.3	10	Maskable	004BH
USI0 TX Interrupt	INT10	IE1.4	11	Maskable	0053H
External Interrupt 12	INT11	IE1.5	12	Maskable	005BH
T0 Overflow Interrupt	INT12	IE2.0	13	Maskable	0063H
T0 Match Interrupt	INT13	IE2.1	14	Maskable	006BH
T1 Match Interrupt	INT14	IE2.2	15	Maskable	0073H
T2 Match Interrupt	INT15	IE2.3	16	Maskable	007BH
T3 Match Interrupt	INT16	IE2.4	17	Maskable	0083H
T4/T5 Match Interrupt	INT17	IE2.5	18	Maskable	008BH
ADC Interrupt	INT18	IE3.0	19	Maskable	0093H
USART1 RX Interrupt	INT19	IE3.1	20	Maskable	009BH
WT Interrupt	INT20	IE3.2	21	Maskable	00A3H
WDT Interrupt	INT21	IE3.3	22	Maskable	00ABH
BIT Interrupt	INT22	IE3.4	23	Maskable	00B3H
LVI Interrupt	INT23	IE3.5	24	Maskable	00BBH

For maskable interrupt execution, EA bit must set ‘1’ and specific interrupt must be enabled by writing ‘1’ to associated bit in the IEx. If an interrupt request is received, the specific interrupt request flag is set to ‘1’. And it

remains ‘1’ until CPU accepts interrupt. If the interrupt is served, the interrupt request flag will be cleared automatically.

7 Clock Generator

7.1 Overview

As shown in Figure 14, the clock generator produces the basic clock pulses which provide the system clock to be supplied to the CPU and the peripheral hardware. It contains sub-frequency clock oscillator. The sub clock operation can be easily obtained by attaching a crystal between the SXIN and SXOUT pin. The sub clock can be also obtained from the external oscillator. In this case, it is necessary to put the external clock signal into the SXIN pin and open the SXOUT pin. The default system clock is 1MHz INT-RC Oscillator. In order to stabilize system internally, it is used 128kHz LOW INT-RC oscillator on POR.

- Calibrated High Internal RC Oscillator (f_{HSIRC} =16MHz)
    - HSIRC OSC (16MHz, Default system clock)
    - HSIRC OSC/2 (8MHz)
    - HSIRC OSC/4 (4MHz)
    - HSIRC OSC/8 (2MHz)
    - HSIRC OSC/16 (1MHz)
    - HSIRC OSC/32 (0.5MHz)
- SubCrystal Oscillator (32.768kHz)
- Internal LSIRC Oscillator (128kHz)

7.2 Block Diagram

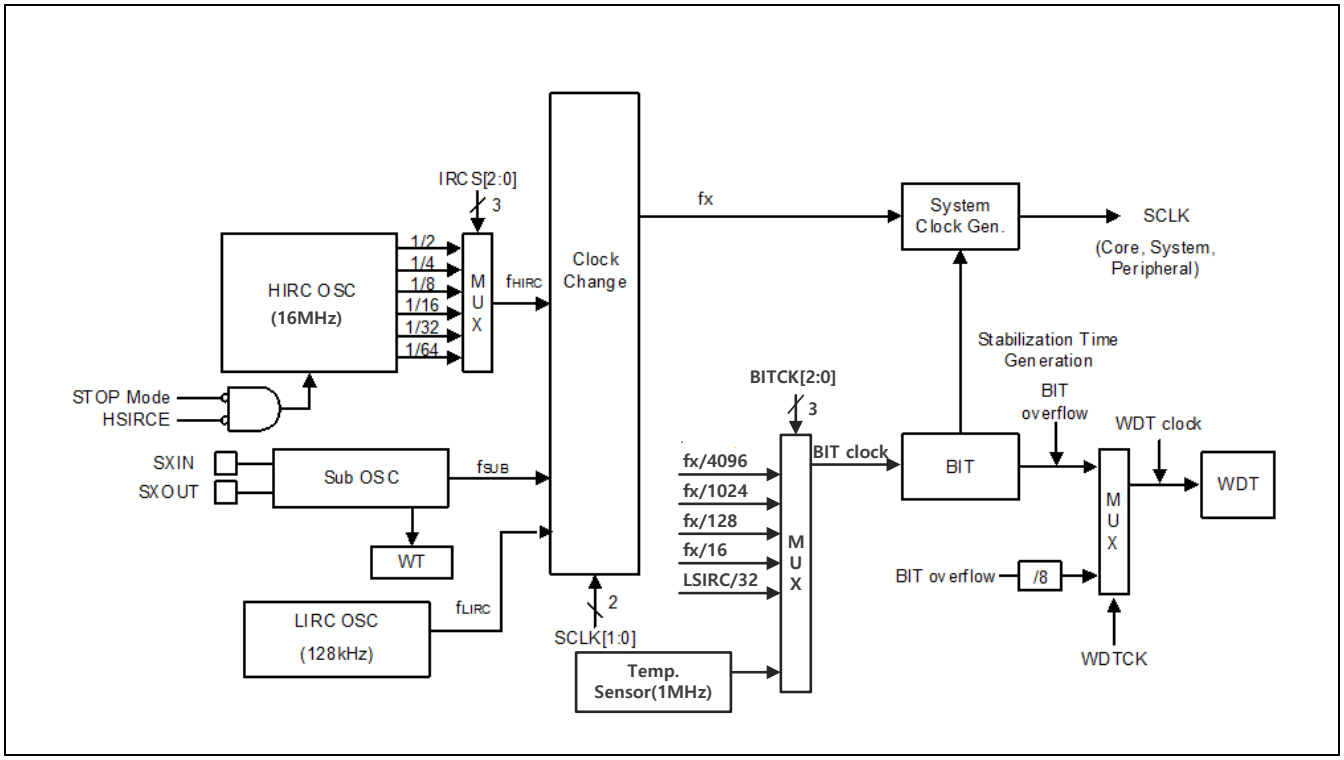


Figure 14. Clock Generator Block Diagram

8 Basic Interval Timer

8.1 Overview

The A96T418 has one 8-bit basic interval timer that is free-run and can't stop. Block diagram is shown in Figure 15. In addition, the basic interval timer generates the time base for watchdog timer counting. It also provides a basic interval timer interrupt (BITIFR).

The A96T418 has these basic interval timer (BIT) features:

- During Power On, BIT gives a stable clock generation time
- On exiting Stop mode, BIT gives a stable clock generation time
- As timer function, timer interrupt occurrence

8.2 Block Diagram

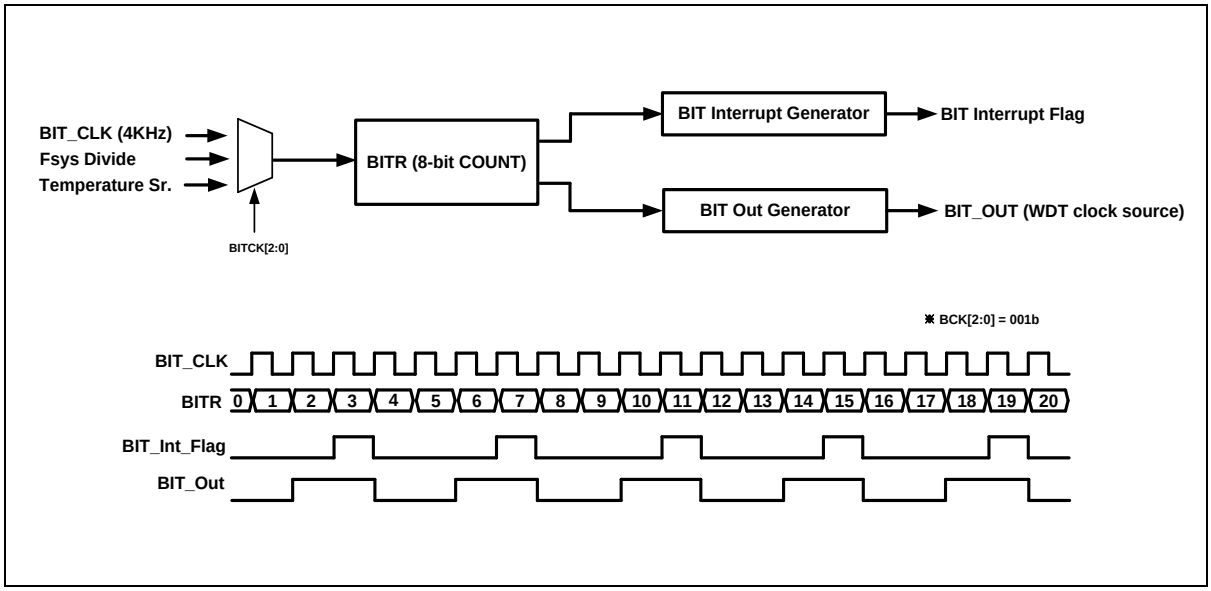


Figure 15. Basic Interval Timer Block Diagram

9 Watch Dog Timer

9.1 Overview

The watchdog timer rapidly detects the CPU malfunction such as endless looping caused by noise or something like that, and resumes the CPU to the normal state. The watchdog timer signal for malfunction detection can be used as either a CPU reset or an interrupt request. When the watchdog timer is not being used for malfunction detection, it can be used as a timer to generate an interrupt at fixed intervals. It is possible to use free running 8-bit timer mode (WDTRSON='0') or watch dog timer mode (WDTRSON='1') as setting WDTCR[6] bit. If WDTCR[5] is written to '1', WDT counter value is cleared and counts up. After 1 machine cycle, this bit is cleared to '0' automatically. The watchdog timer consists of 8-bit binary counter and the watchdog timer data register. When the value of 8-bit binary counter is equal to the 8 bits of WDTCNT, the interrupt request flag is generated. This can be used as Watchdog timer interrupt or reset of CPU in accordance with the bit WDTRSON.

The input clock source of watch dog timer is the BIT overflow. The interval of watchdog timer interrupt is decided by BIT overflow period and WDTDR set value. The equation can be described as

WDT Interrupt Interval = (BIT Interrupt Interval) X (WDTDR Value+1)

9.2 WDT Interrupt Timing Waveform

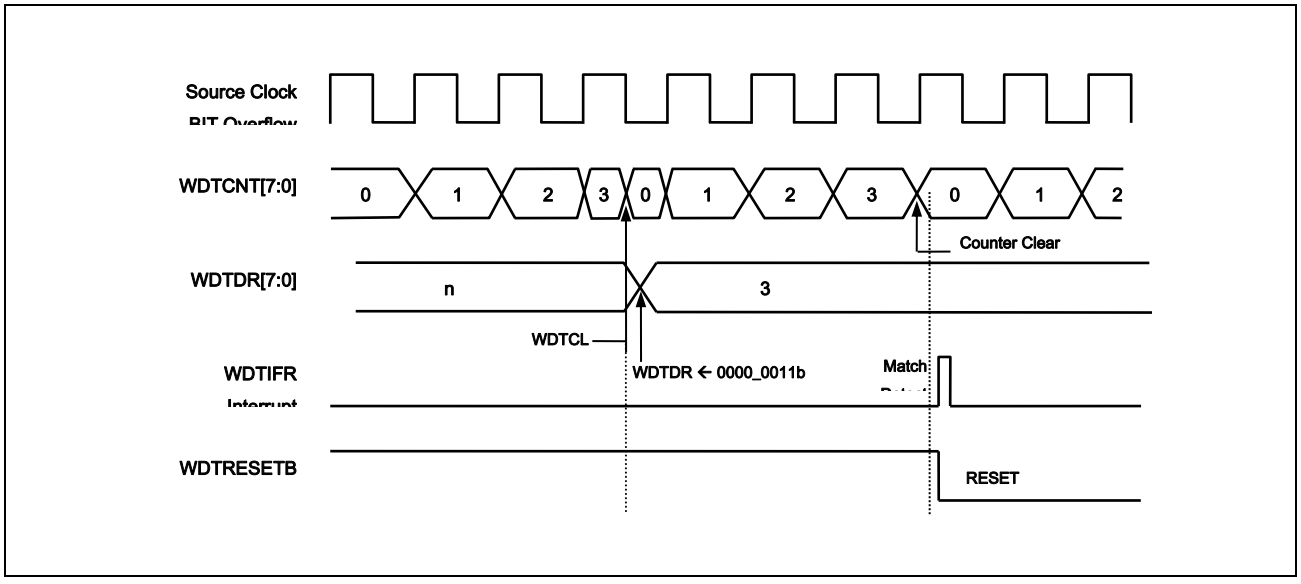


Figure 16. Watch Dog Timer Interrupt Timing Waveform

9.3 Block Diagram

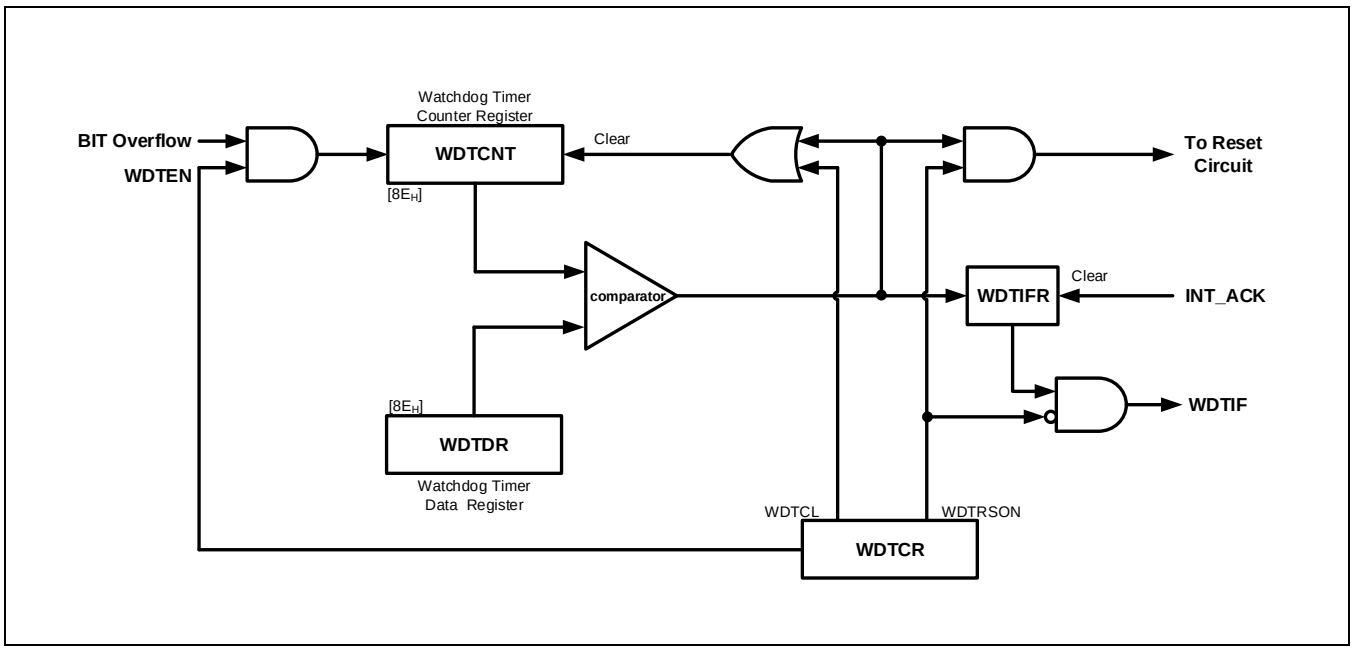


Figure 17. Watch Dog Timer Block Diagram

10 Watch Timer

10.1 Overview

The watch timer has the function for RTC (Real Time Clock) operation. It is generally used for RTC design. The internal structure of the watch timer consists of the clock source select circuit, timer counter circuit, output select circuit, and watch timer control register. To operate the watch timer, determine the input clock source, output interval, and set WTEN to '1' in watch timer control register (WTCR). It is able to execute simultaneously or individually. To stop or reset WT, clear the WTEN bit in WTCR register. Even if CPU is STOP mode, sub clock is able to be so alive that WT can continue the operation. The watch timer counter circuits may be composed of 21-bit counter which contains low 14-bit with binary counter and high 7-bit counter in order to raise resolution. In WTDR, it can control WT clear and set interval value at write time, and it can read 7-bit WT counter value at read time.

10.2 Block Diagram

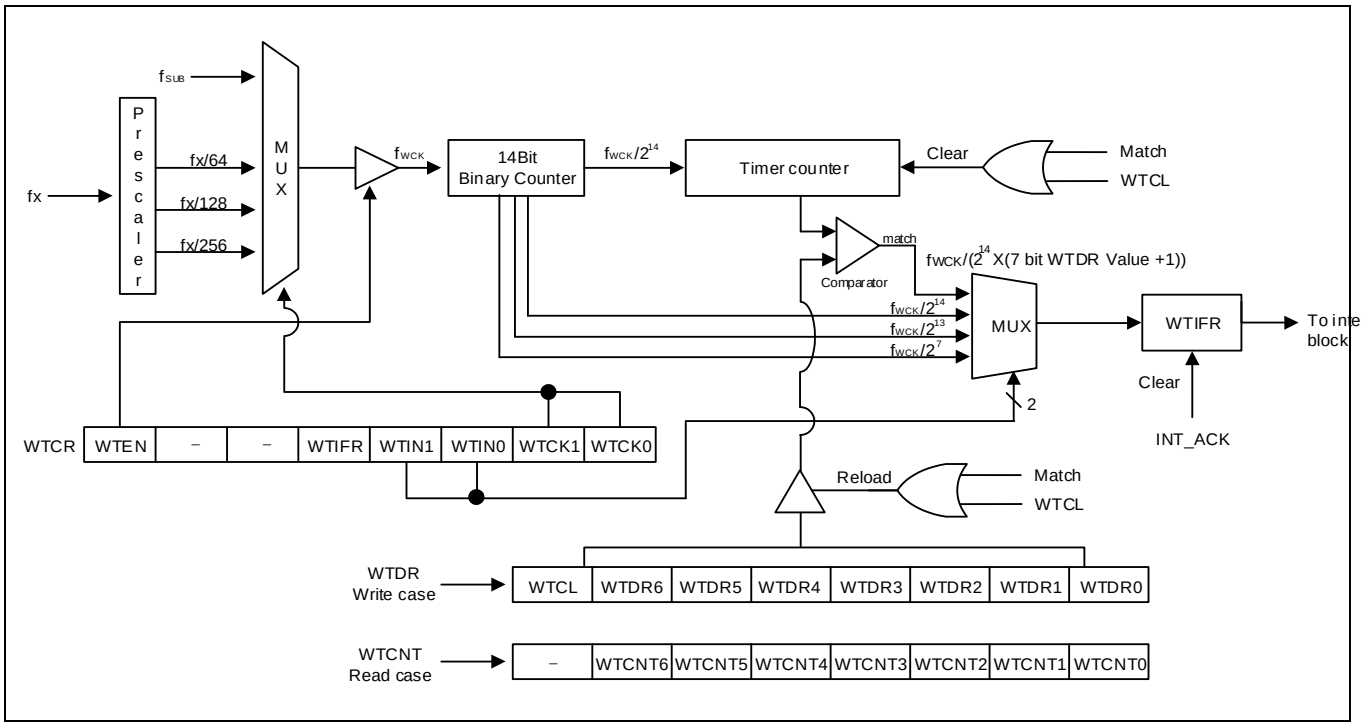


Figure 18. Watch Timer Block Diagram

11 Timer 0/1/2/3/4/5

11.1 Timer 0

11.1.1 Overview

The 8-bit timer 0 consists of multiplexer, timer 0 counter register, timer 0 data register, timer 0 capture data register and timer 0 control register (T0CNT, T0DR, T0CDR, and T0CR).

It has three operating modes:

8-bit timer/counter mode

8-bit PWM output mode

8-bit capture mode

The timer/counter 0 can be clocked by an internal or an external clock source (EC0). The clock source is selected by clock selection logic which is controlled by the clock selection bits (T0CK[2:0]).

TIMER0 clock source: f_X/2, 4, 8, 32, 128, 512, 2048 and EC0

In the capture mode, by EINT10, the data is captured into input capture data register (T0CDR). In timer/counter mode, whenever counter value is equal to T0DR, T0O port toggles. Also the timer 0 outputs PWM waveform through PWM0O port in the PWM mode.

Table 10. Timer 0 Operating Modes

T0EN	T0MS[1:0]	T0CK[2:0]	Timer 0
1	00	XXX	8-bit Timer/Counter Mode
1	01	XXX	8-bit PWM Mode
1	1X	XXX	8-bit Capture Mode

11.1.2 8-bit Timer/Counter Mode

The 8-bit timer/counter mode is selected by control register as shown in Figure 19.

The 8-bit timer have counter and data register. The counter register is increased by internal or external clock input. Timer 0 can use the input clock with one of 2, 4, 8, 32, 128, 512 and 2048 prescaler division rates (T0CK[2:0]). When the value of T0CNT and T0DR is identical in timer 0, a match signal is generated and the interrupt of Timer 0 occurs. T0CNT value is automatically cleared by match signal. It can be also cleared by software (T0CC).

The external clock (EC0) counts up the timer at the rising edge. If the EC0 is selected as a clock source by T0CK[2:0], EC0 port should be set to the input port by P25IO bit.

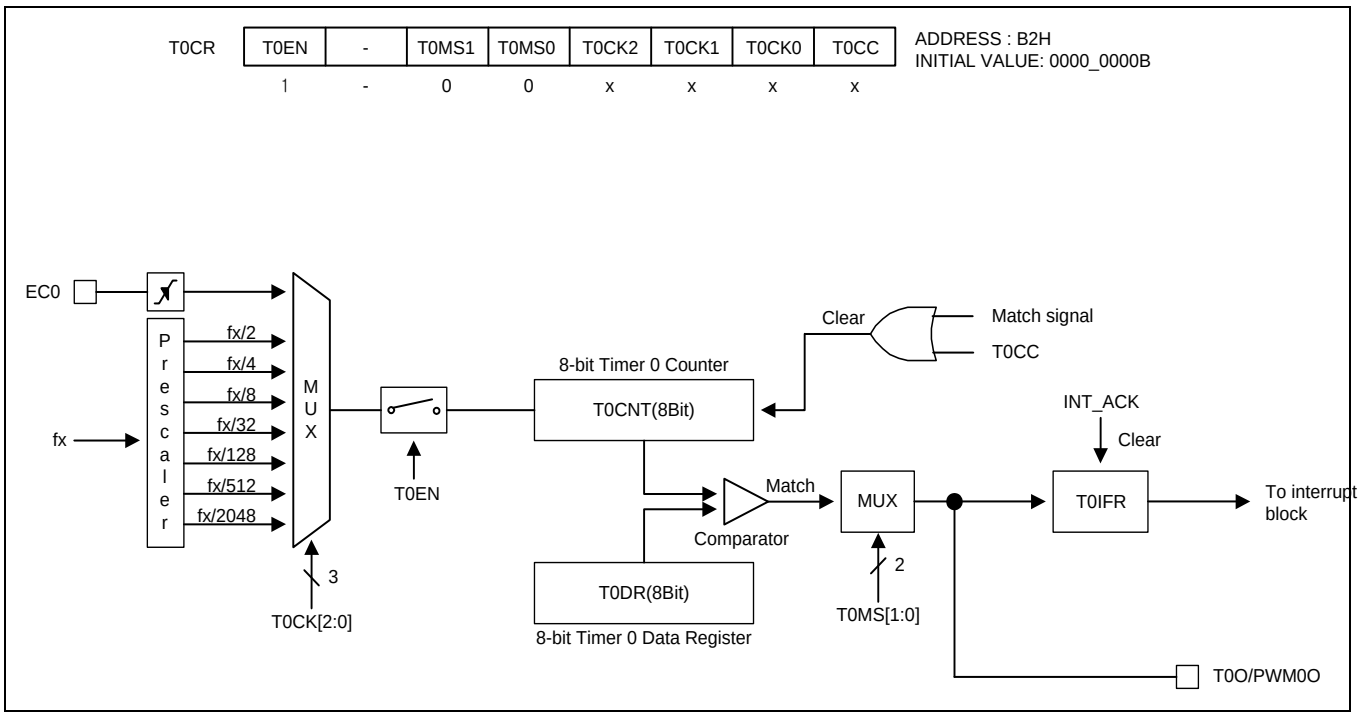


Figure 19. 8-bit Timer/Counter Mode for Timer 0

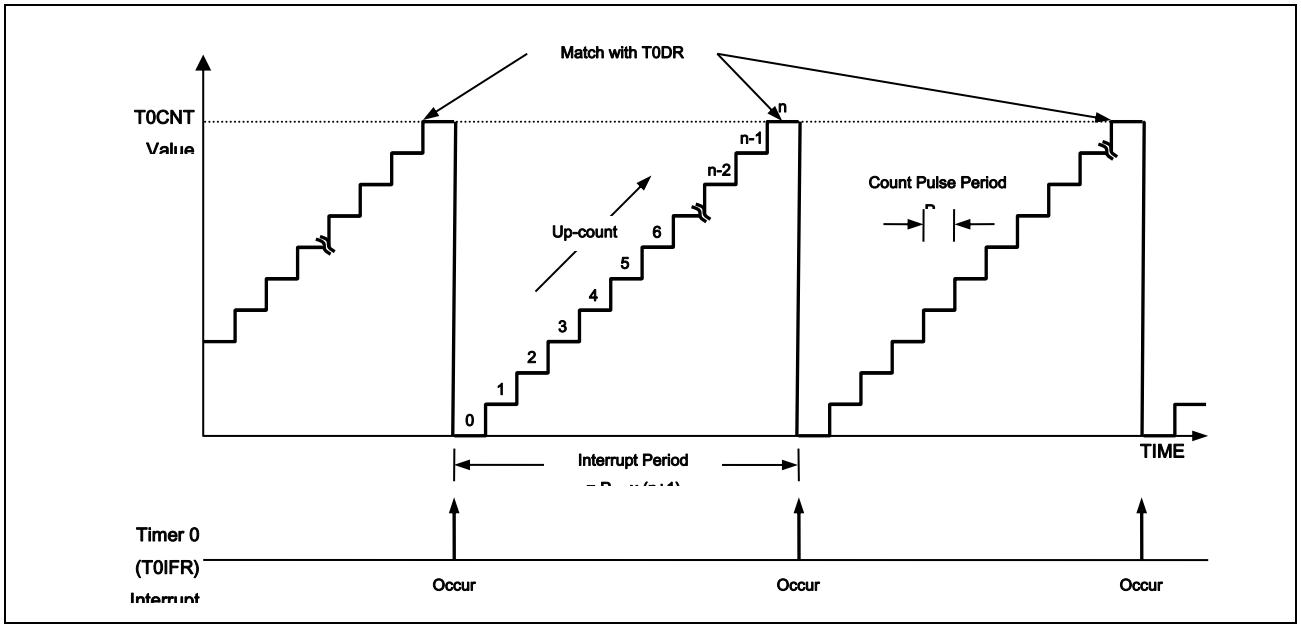


Figure 20. 8-bit Timer/Counter 0 Example

11.1.3 8-bit PWM Mode

The timer 0 has a high speed PWM (Pulse Width Modulation) function. In PWM mode, T0O/PWM0O pin outputs up to 8-bit resolution PWM output. This pin should be configured as a PWM output by setting the T0O/PWM0O function by P2FSRH[7:6] bits. In the 8-bit timer/counter mode, a match signal is generated when the counter value is identical to the value of T0DR. When the value of T0CNT and T0DR is identical in timer 0, a match signal is generated and the interrupt of timer 0 occurs. In PWM mode, the match signal does not clear the counter. Instead, it runs continuously, overflowing at “FFH”, and then continues incrementing from “00H”. The timer 0 overflow interrupt is generated whenever a counter overflow occurs. T0CNT value is cleared by software (T0CC) bit.

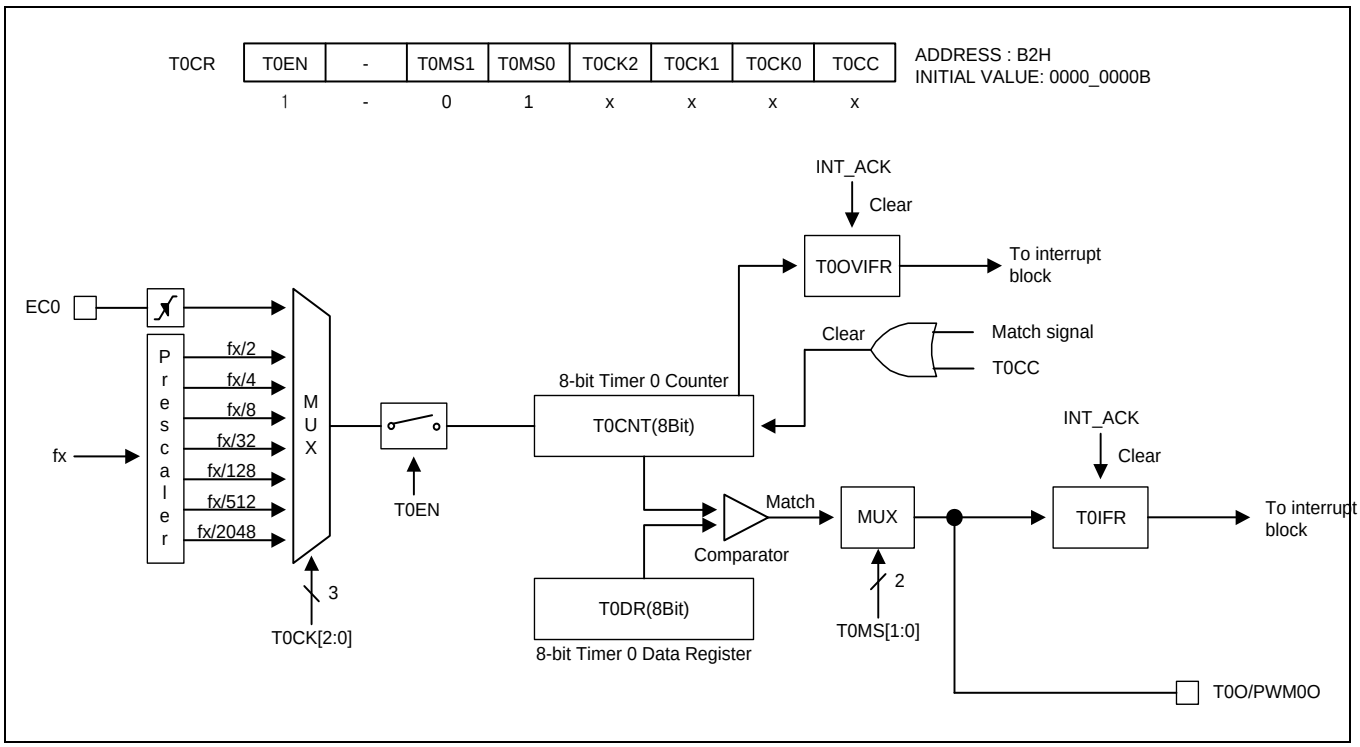


Figure 21. 8-bit PWM Mode for Timer 0

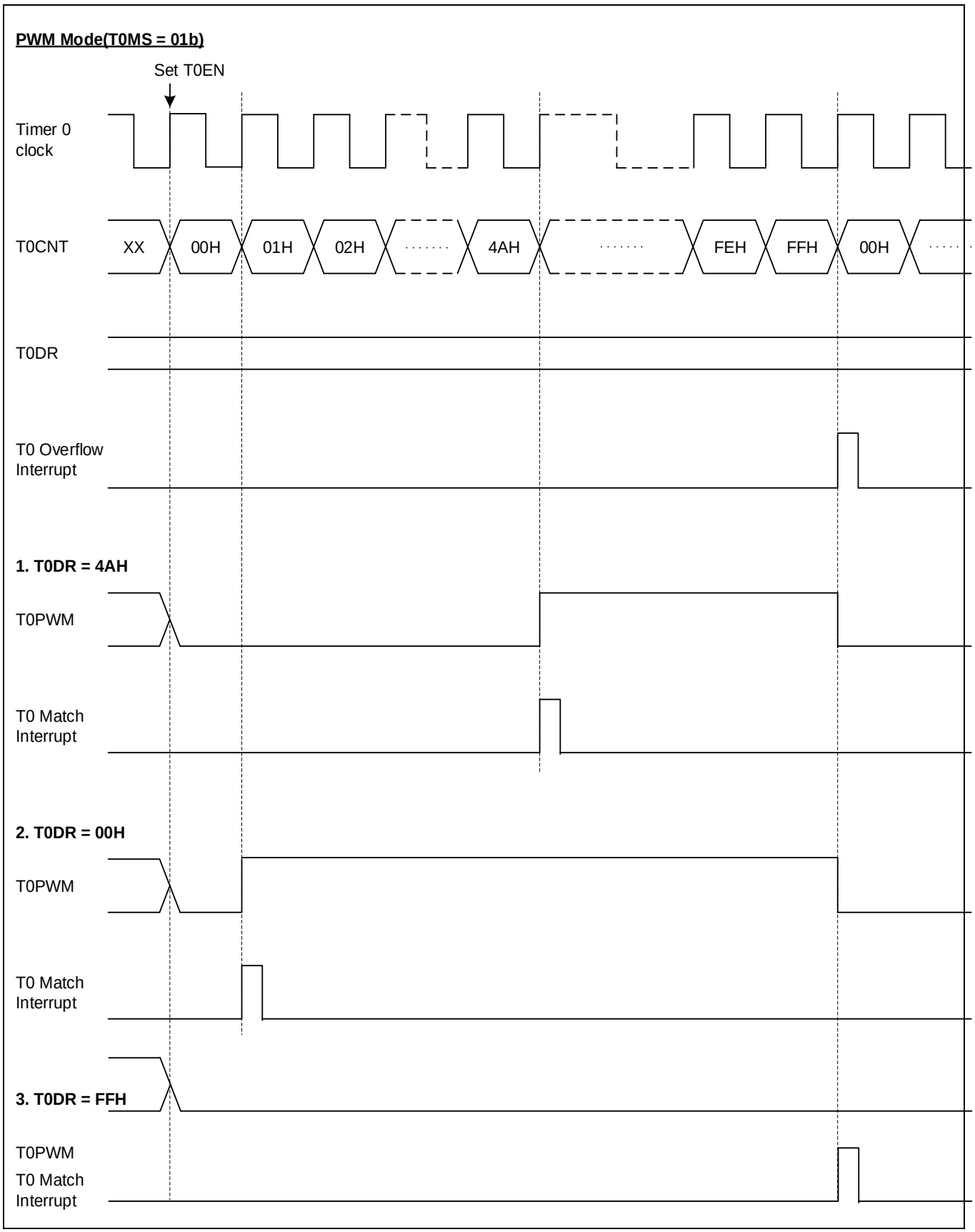


Figure 22. PWM Output Waveforms in PWM Mode for Timer 0

11.1.4 8-bit Capture Mode

The timer 0 capture mode is set by T0MS[1:0] as '1x'. The clock source can use the internal/external clock. Basically, it has the same function as the 8-bit timer/counter mode and the interrupt occurs when T0CNT is equal to T0DR. T0CNTvalue is automatically cleared by match signal and it can be also cleared by software (T0CC).

This timer interrupt in capture mode is very useful when the pulse width of captured signal is wider than the maximum period of timer.

The capture result is loaded into T0CDR. In the timer 0 capture mode, timer 0 output (T0O) waveform is not available.

T0CDR and T0DR are in the same address. In the capture mode, reading operation readsT0CDR, not T0DR and writing operation will update T0DR.

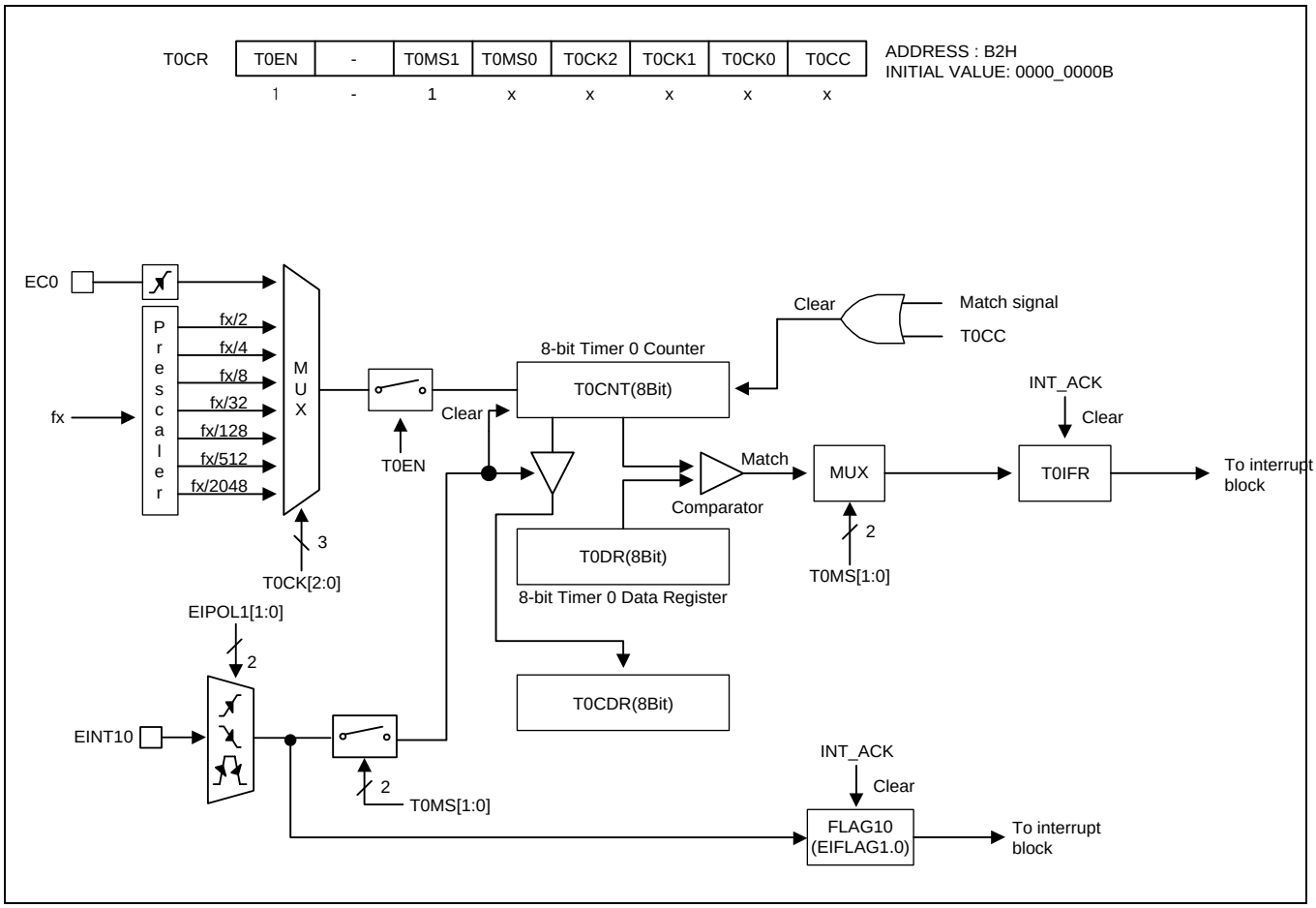


Figure 23. 8-bit Capture Mode for Timer 0

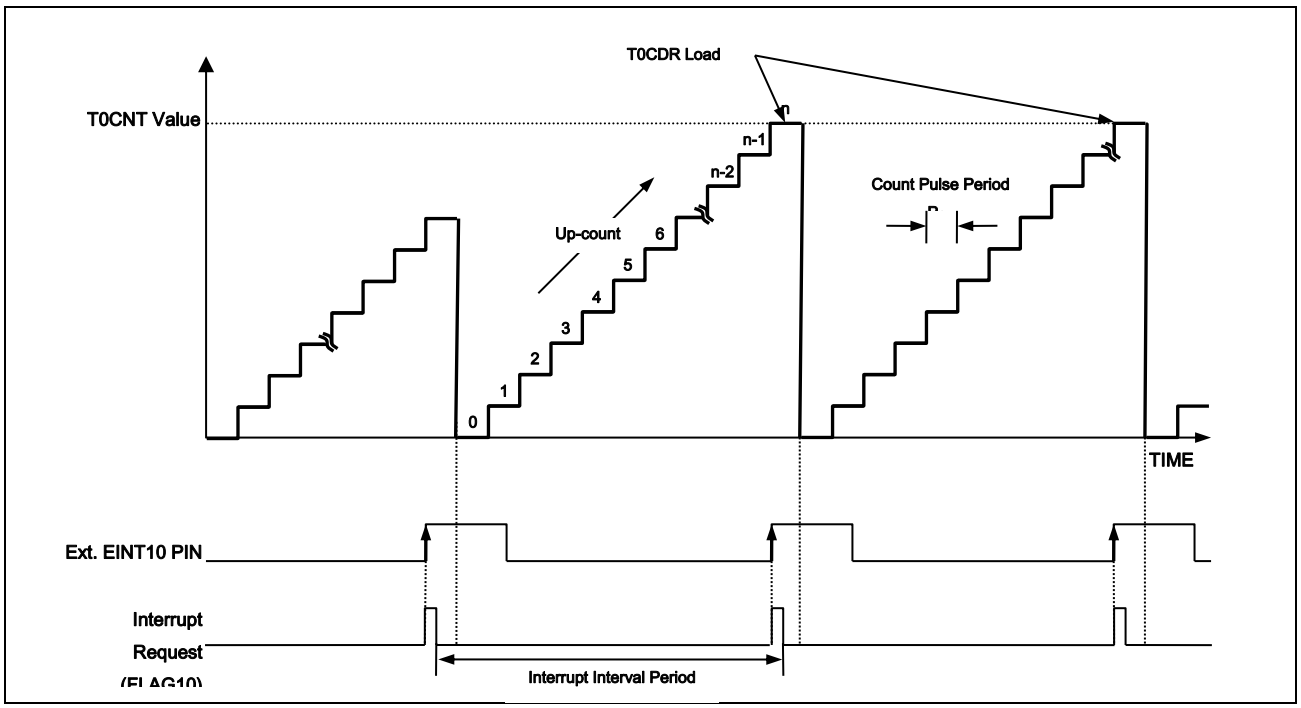


Figure 24. Input Capture Mode Operation for Timer 0

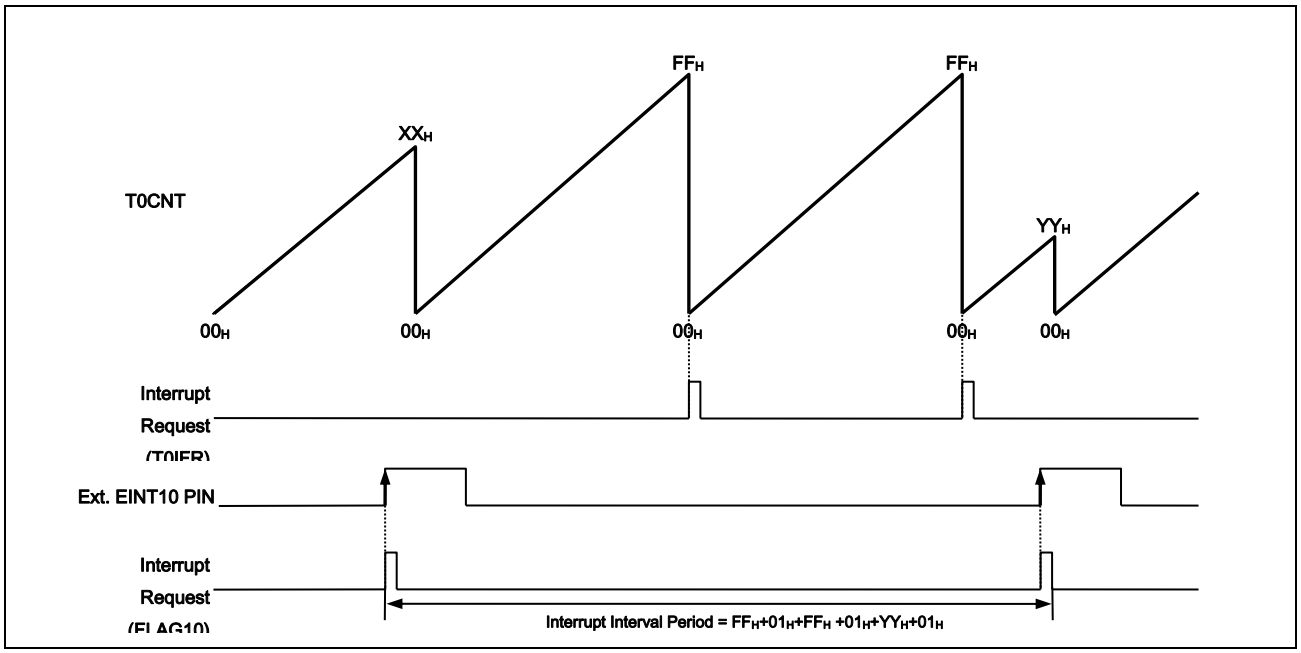


Figure 25. Express Timer Overflow in Capture Mode

11.1.5 Block Diagram

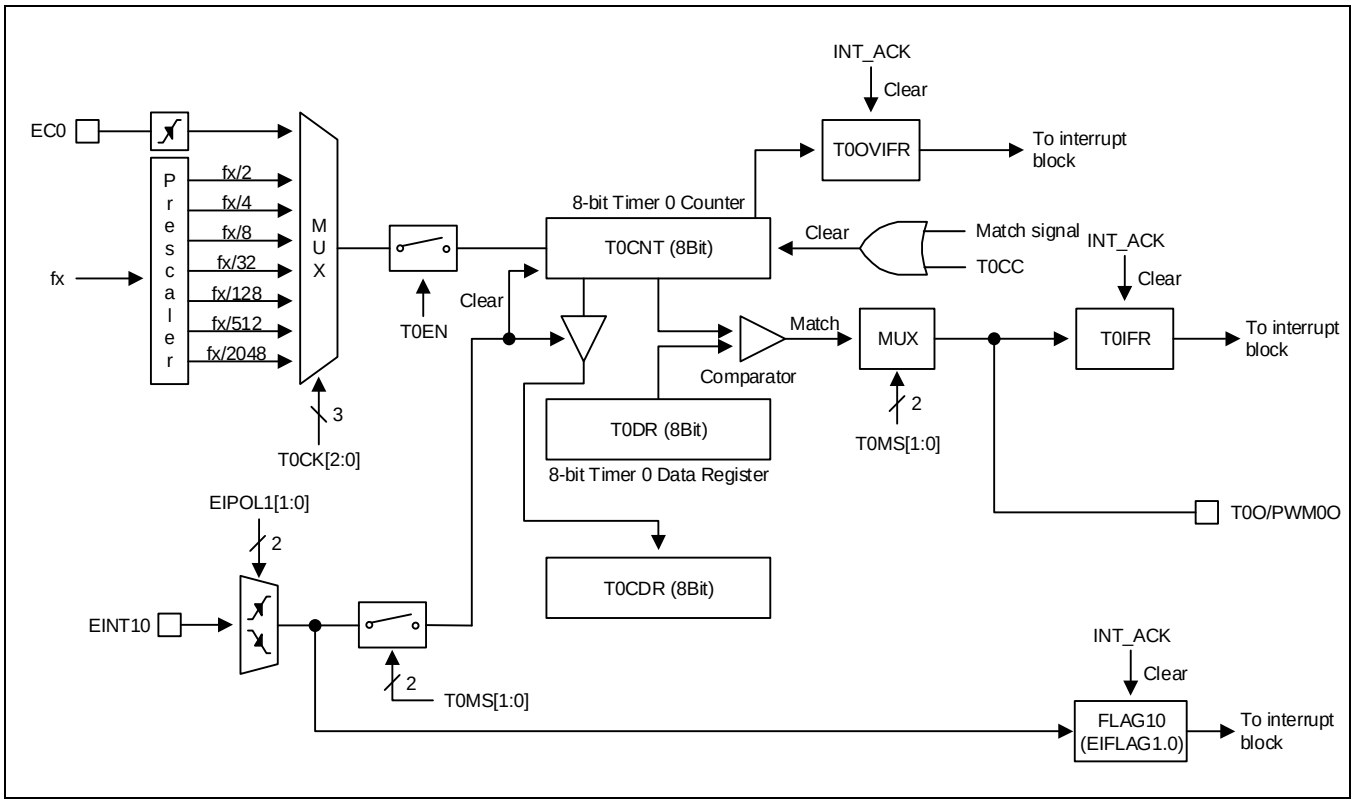


Figure 26. 8-bit Timer 0 Block Diagram

11.2 Timer 1

11.2.1 Overview

The 16-bit timer 1 consists of multiplexer, timer 1 A data register high/low, timer 1 B data register high/low and timer 1 control register high/low (T1ADRH, T1ADRL, T1BDRH, T1BDRL, T1CRH, T1CRL).

It has four operating modes:

16-bit timer/counter mode

16-bit capture mode

16-bit PPG output mode (one-shot mode)

16-bit PPG output mode (repeat mode)

The timer/counter 1 can be clocked by an internal or an external clock source (EC1). The clock source is selected by clock selection logic which is controlled by the clock selection bits (T1CK[2:0]).

TIMER 1 clock source: f_X/1, 2, 4, 8, 64, 512, 2048 and EC1

In the capture mode, by EINT11, the data is captured into input capture data register (T1BDRH/T1BDRL). Timer 1 outputs the comparison result between counter and data register through T1O port in timer/counter mode. Also Timer 1 outputs PWM wave form through PWM1O port in the PPG mode.

Table 11. Timer 1 Operating Modes

T1EN	P1FSRL[1:0]	T1MS[1:0]	T1CK[2:0]	Timer 1
1	11	00	XXX	16-bit Timer/Counter Mode
1	00	01	XXX	16-bit Capture Mode
1	11	10	XXX	16-bit PPG Mode(one-shot mode)
1	11	11	XXX	16-bit PPG Mode(repeat mode)

11.2.2 16-bit Timer/Counter Mode

The 16-bit timer/counter mode is selected by control register as shown in Figure 27.

The 16-bit timer have counter and data register. The counter register is increased by internal or external clock input. Timer 1 can use the input clock with one of 1, 2, 4, 8, 64, 512 and 2048 prescaler division rates (T1CK[2:0]). When the value of T1CNTH, T1CNTL and the value of T1ADRH, T1ADRL are identical in Timer 1 respectively, a match signal is generated and the interrupt of Timer1occurs. The T1CNTH, T1CNTL value is automatically cleared by match signal. It can be also cleared by software (T1CC).

The external clock (EC1) counts up the timer at the rising edge. If the EC1 is selected as a clock source by T1CK[2:0], EC1 port should be set to the input port by P23IO bit.

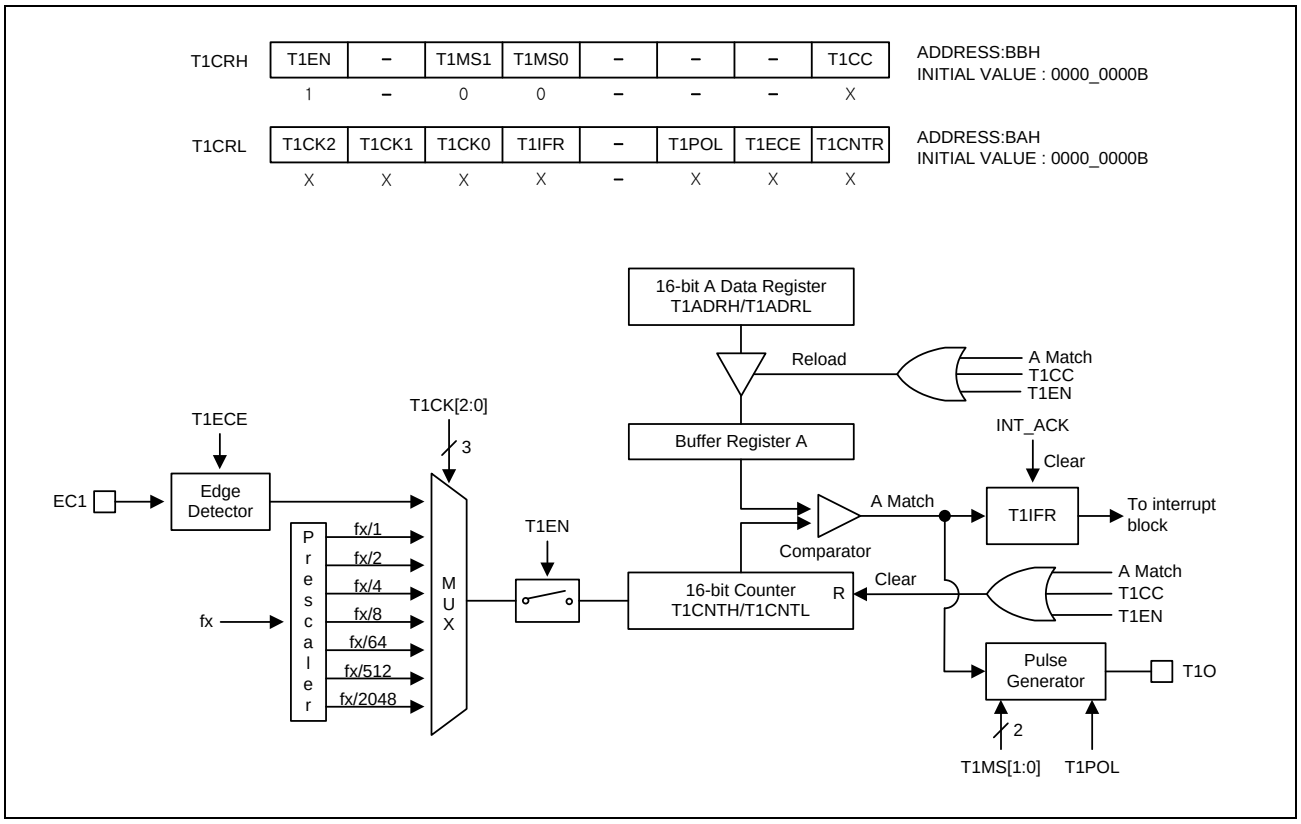


Figure 27. 16-bit Timer/Counter Mode for Timer 1

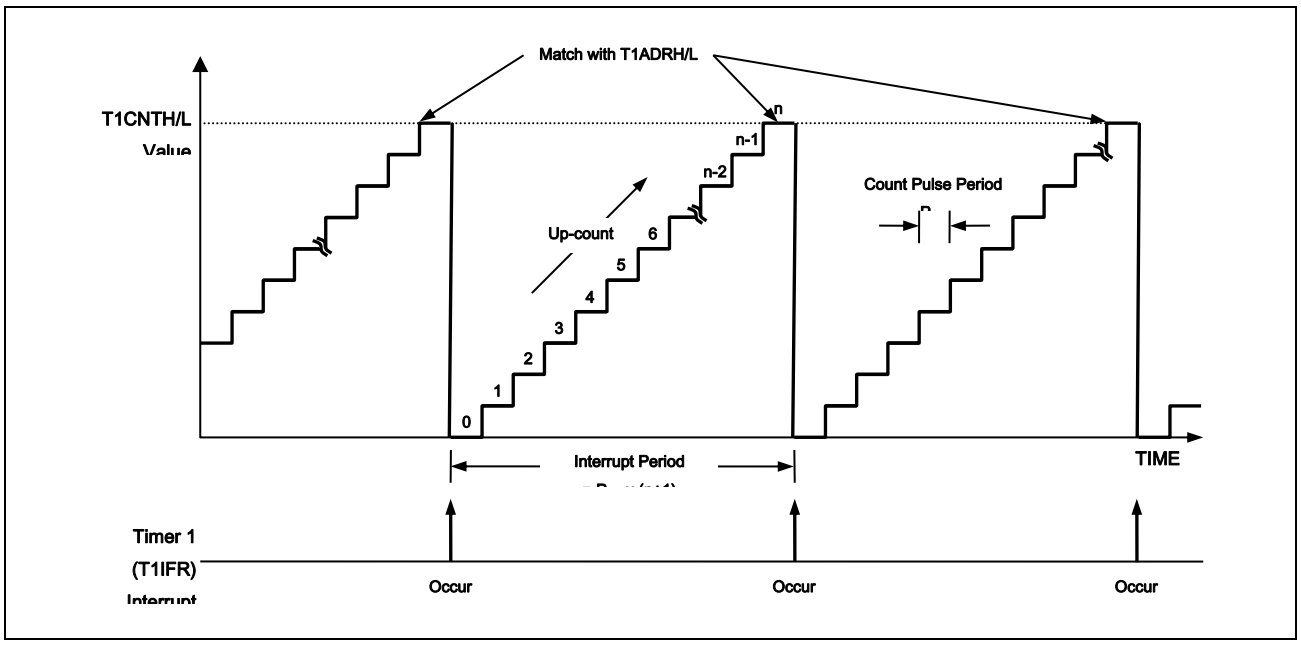


Figure 28. 16-bit Timer/Counter 1 Example

11.2.3 16-bit Capture Mode

The 16-bit timer 1 capture mode is set by T1MS[1:0] as '01'. The clock source can use the internal/external clock. Basically, it has the same function as the 16-bit timer/counter mode and the interrupt occurs when T1CNTH/T1CNTL is equal to T1ADRH/T1ADRL. The T1CNTH, T1CNTL valuesare automatically cleared by match signal. It can be also cleared by software (T1CC).

This timer interrupt in capture mode is very useful when the pulse width of captured signal is wider than the maximum period of timer.

The capture result is loaded into T1BDRH/T1BDRL.

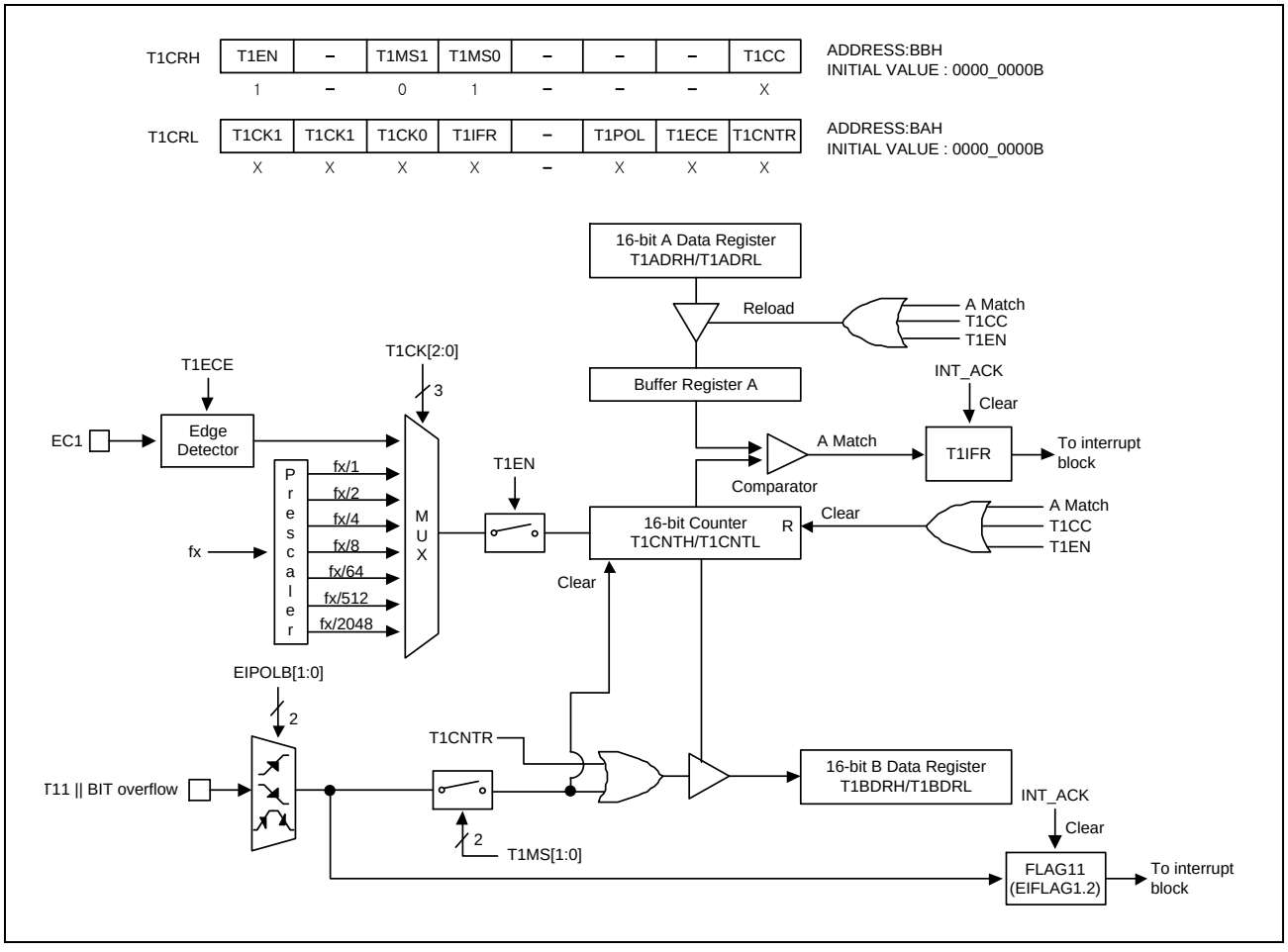


Figure 29. 16-bit Capture Mode for Timer 1

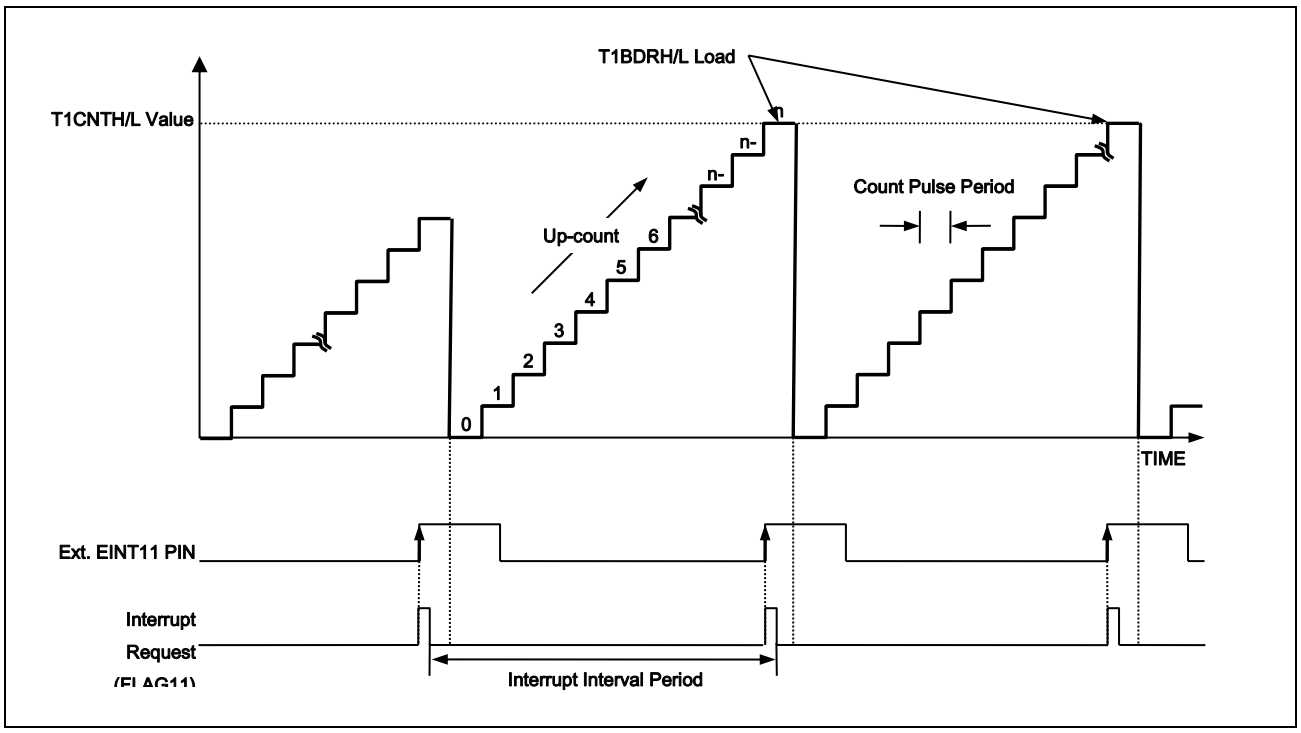


Figure 30. Input Capture Mode Operation for Timer 1

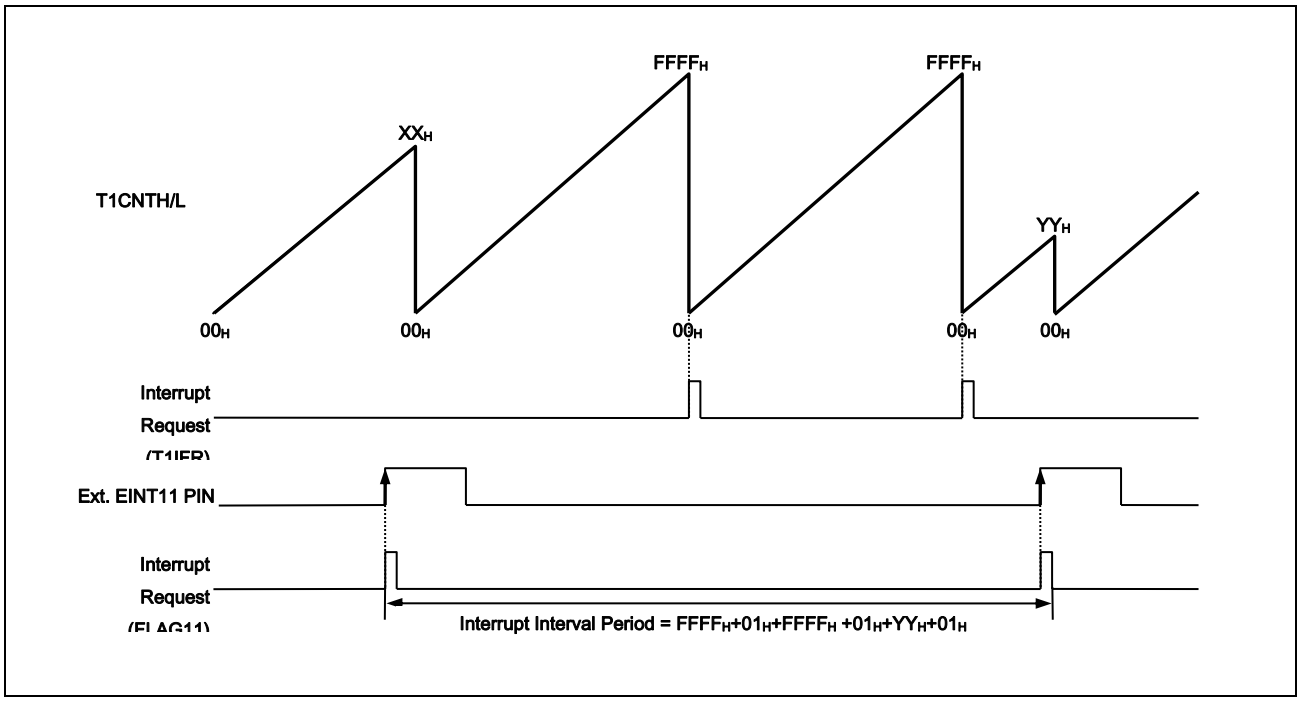
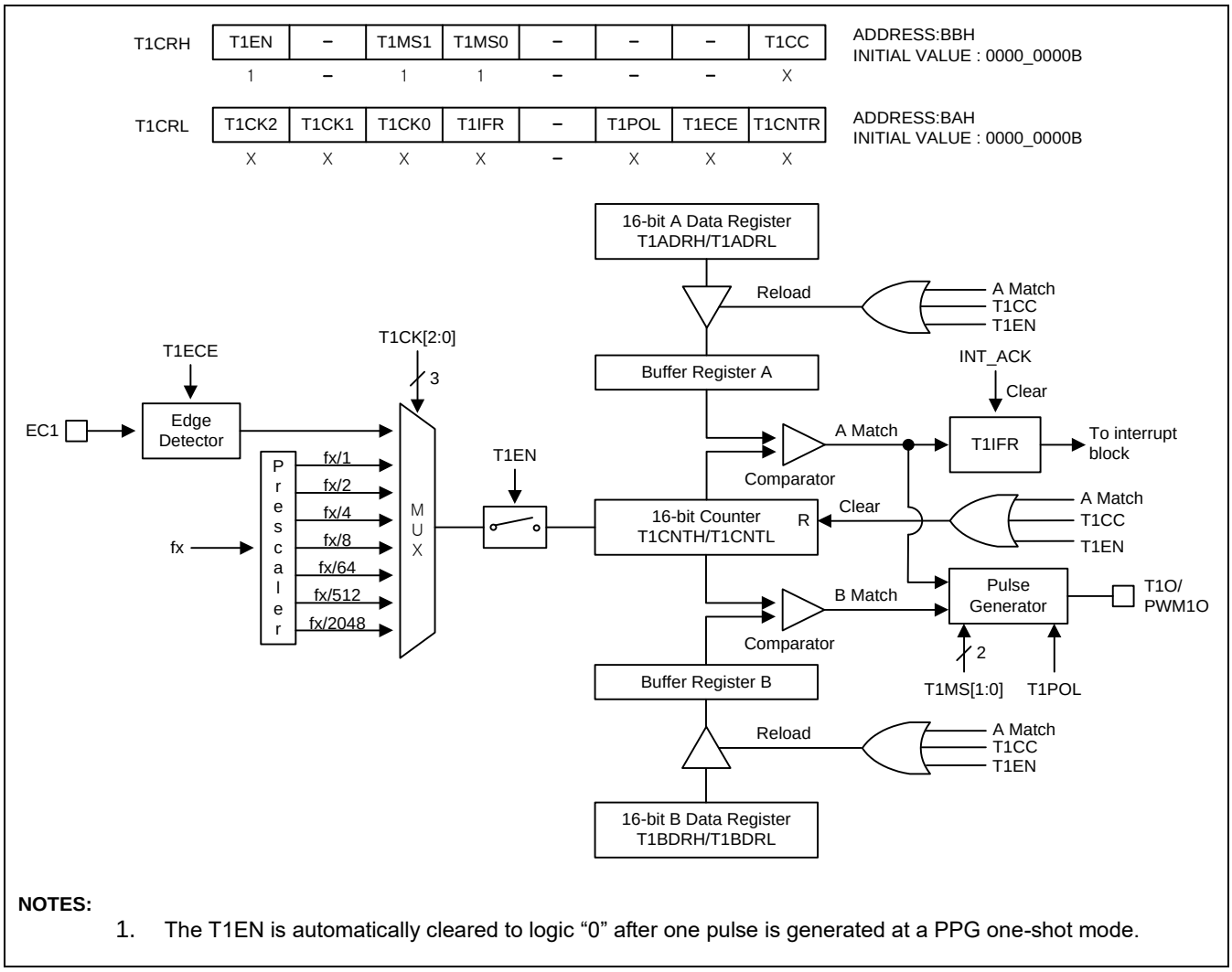


Figure 31. Express Timer Overflow in Capture Mode

11.2.4 16-bit PPG Mode

The timer 1 has a PPG (Programmable Pulse Generation) function. In PPG mode, T1O/PWM1O pin outputs up to 16-bit resolution PWM output. This pin should be configured as a PWM output by setting P1FSRL[3:2] to '11'. The period of the PWM output is determined by the T1ADRH/T1ADRL. And the duty of the PWM output is determined by the T1BDRH/T1BDRL.



NOTES:

1. The T1EN is automatically cleared to logic "0" after one pulse is generated at a PPG one-shot mode.

Figure 32. 16-bit PPG Mode for Timer 1

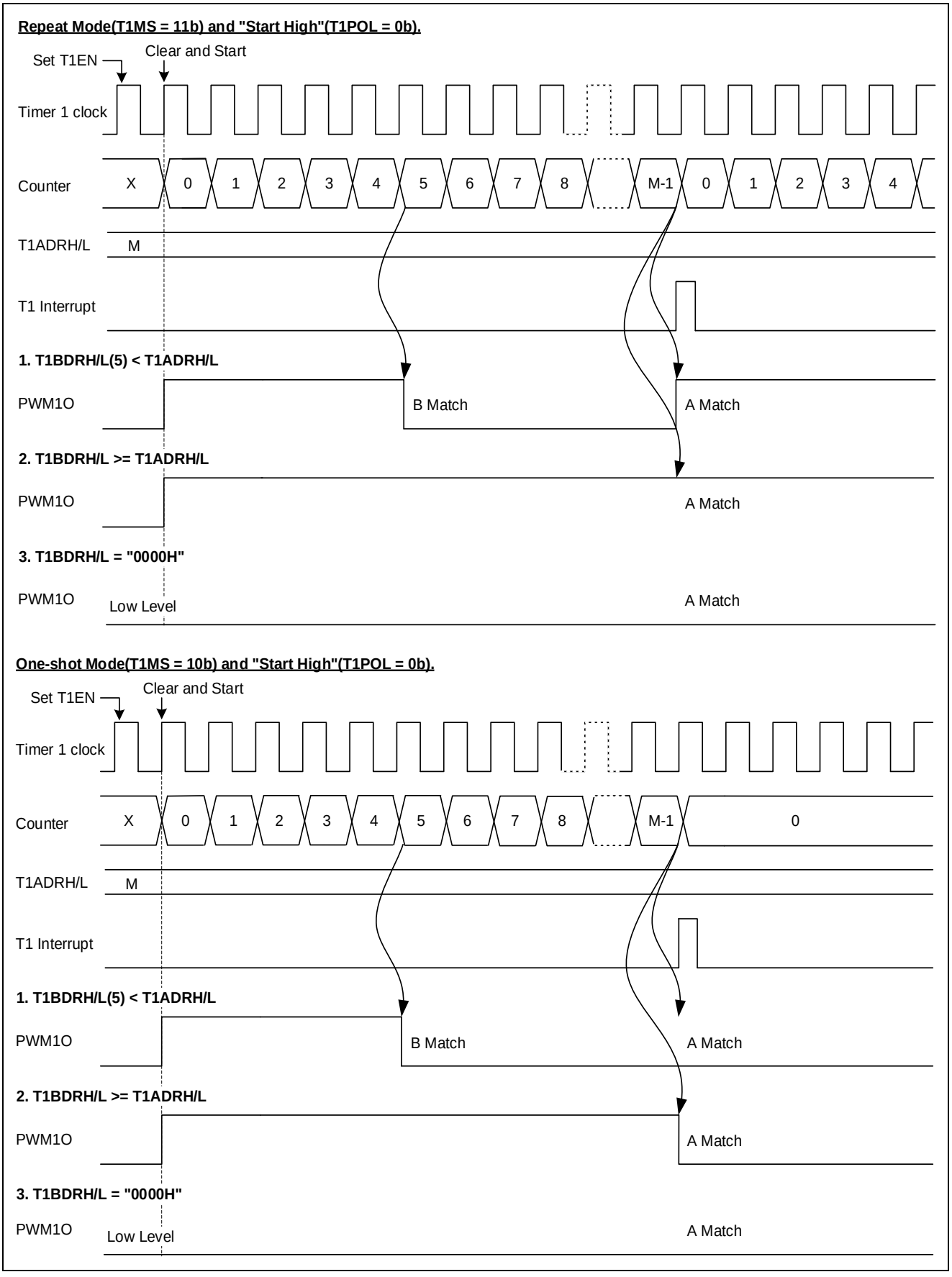


Figure 33. 16-bit PPG Mode Timming chart for Timer 1

11.2.5 Block Diagram

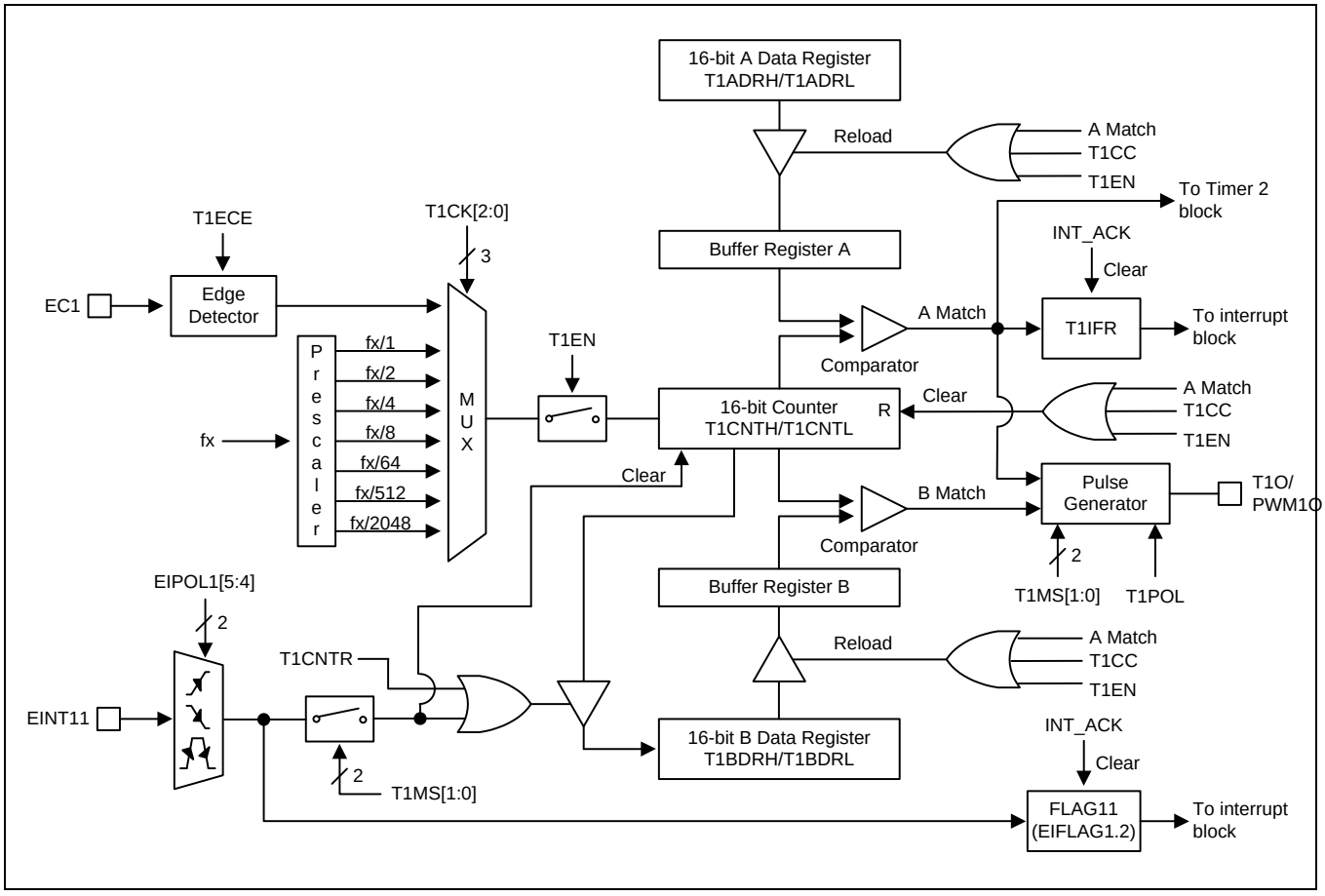


Figure 34. 16-bit Timer 1 Block Diagram

11.3 Timer 2

11.3.1 Overview

The 16-bit timer 2 consists of multiplexer, timer 2 A data high/low register, timer 2 B data high/low register and timer 2 control high/low register (T2ADRH, T2ADRL, T2BDRH, T2BDRL, T2CRH, and T2CRL).

It has four operating modes:

16-bit timer/counter mode

16-bit capture mode

16-bit PPG output mode (one-shot mode)

16-bit PPG output mode (repeat mode)

The timer/counter 2 can be divided clock of the system clock selected from prescaler output and T1 A Match (timer 1 A match signal). The clock source is selected by clock selection logic which is controlled by the clock selection bits (T2CK[2:0]).

TIMER 2 clock source: $f_X/1$, $f_X/2$, $f_X/4$,$f_X/8$,$f_X/32$, $f_X/128$, $f_X/512$ and T1 A Match

In the capture mode, by EINT12, the data is captured into input capture data register (T2BDRH/T2BDRL). In timer/counter mode, whenever counter value is equal to T2ADRH/L, T2O port toggles. Also the timer 2 outputs PWM wave form to PWM2O port in the PPG mode.

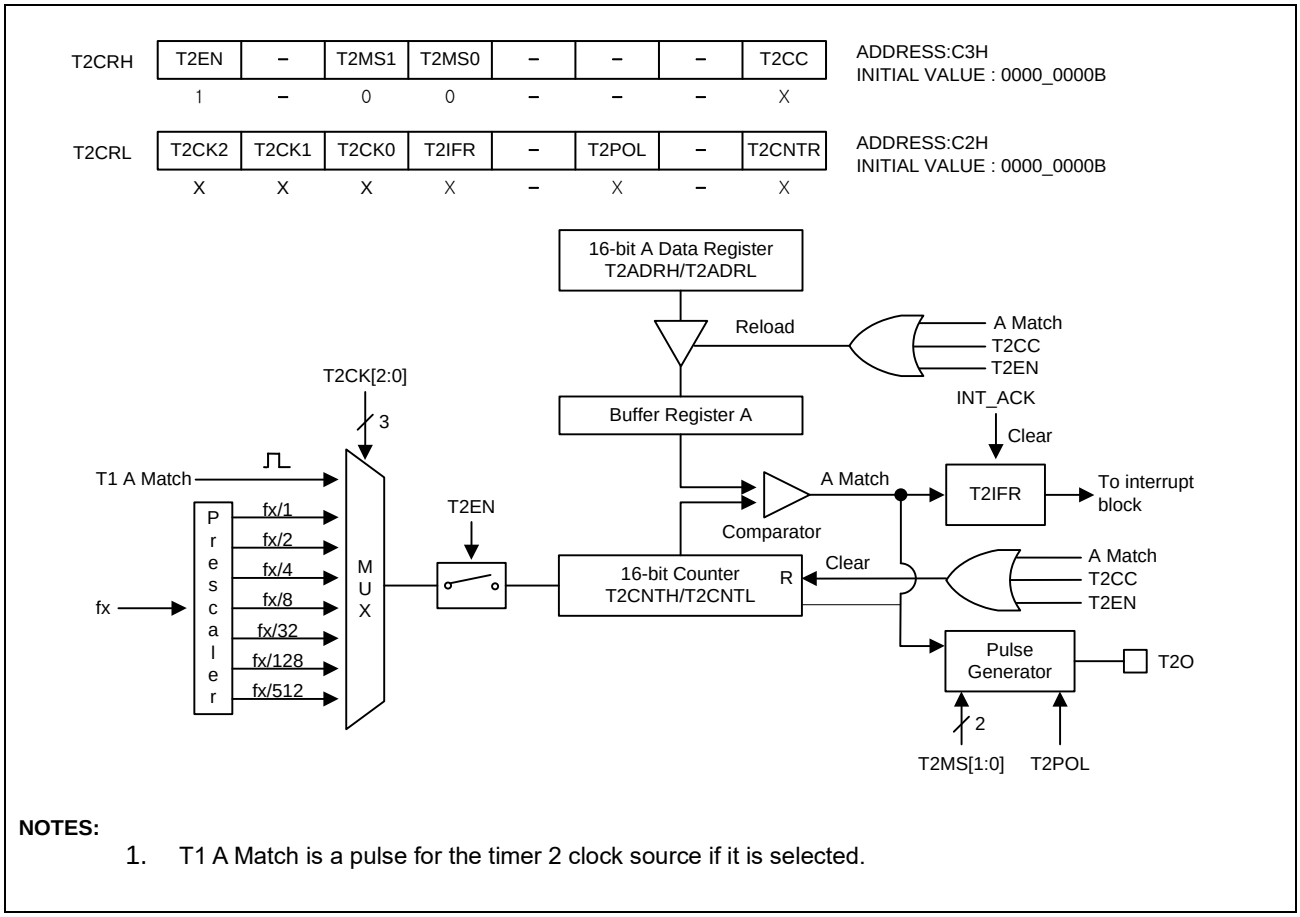
Table 12. Timer 2 Operating Modes

T2EN	P1FSRL[5:4]	T2MS[1:0]	T2CK[2:0]	Timer 2
1	11	00	XXX	16-bit Timer/Counter Mode
1	00	01	XXX	16-bit Capture Mode
1	11	10	XXX	16-bit PPG Mode (one-shot mode)
1	11	11	XXX	16-bit PPG Mode (repeat mode)

11.3.2 16-bit Timer/Counter Mode

The 16-bit timer/counter mode is selected by control register as shown in Figure 35.

The 16-bit timer have counter and data register. The counter register is increased by internal or timer 1 A match clock input. Timer 2 can use the input clock with one of 1, 2, 4, 8, 32, 128, 512 and T1 A Match prescaler division rates (T2CK[2:0]). When the values of T2CNTH/T2CNTL and T2ADRH/T2ADRL are identical in timer 2, a match signal is generated and the interrupt of Timer 2 occurs. The T2CNTH/T2CNTL valuesare automatically cleared by match signal. It can be also cleared by software (T2CC).



NOTES:

1. T1 A Match is a pulse for the timer 2 clock source if it is selected.

Figure 35. 16-bit Timer/Counter Mode for Timer 2

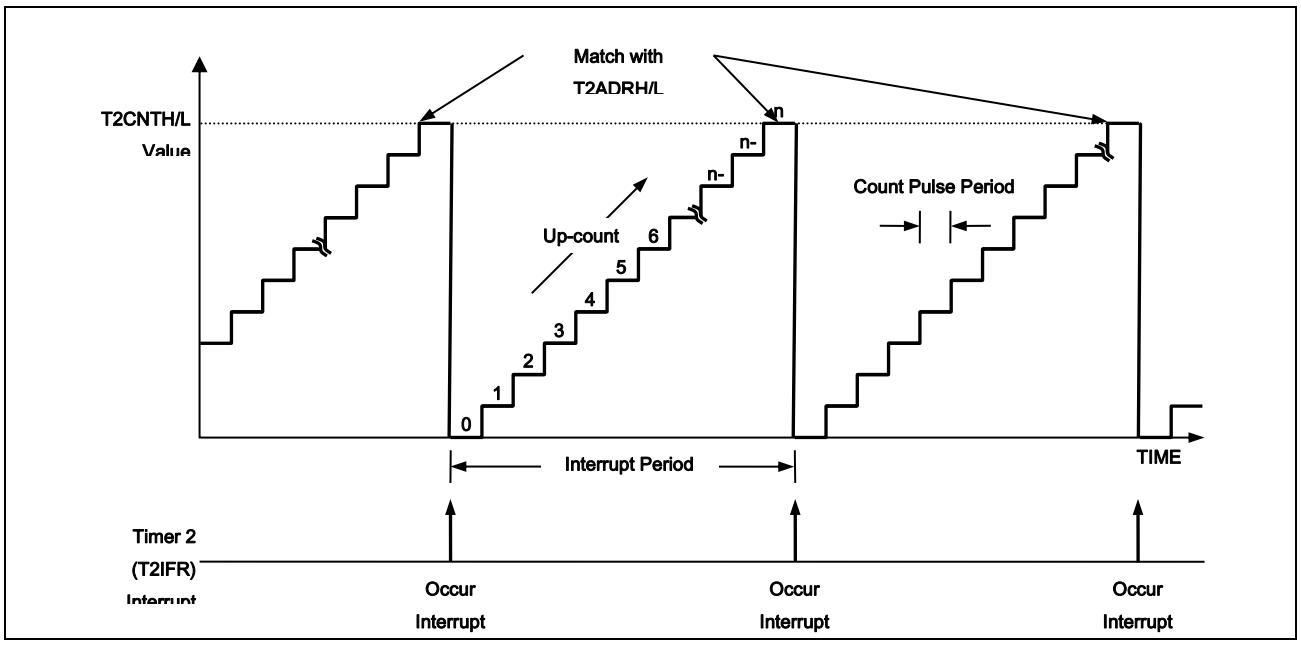


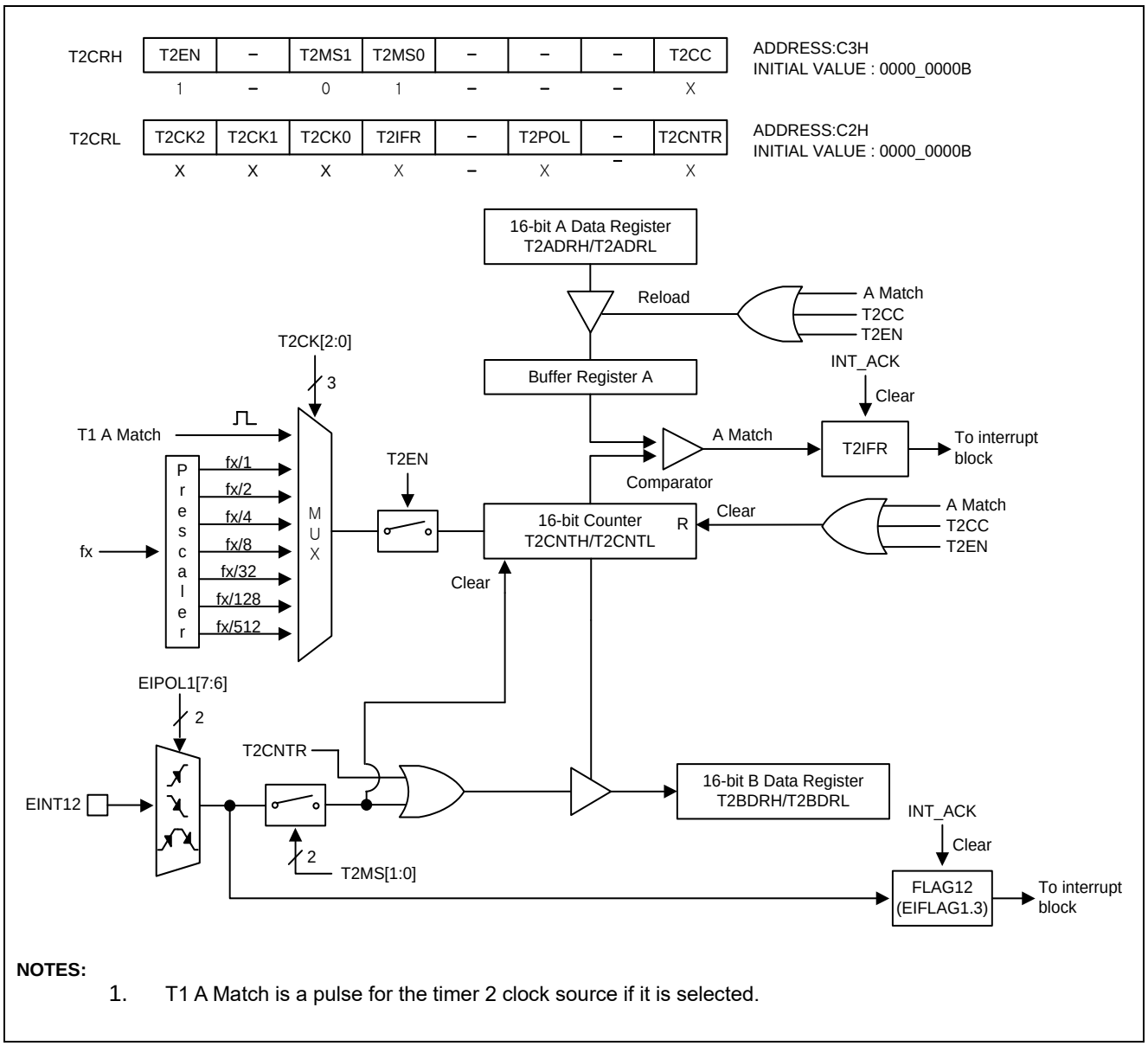
Figure 36. 16-bit Timer/Counter 2 Example

11.3.3 16-bit Capture Mode

The timer 2 capture mode is set by T2MS[1:0] as '01'. The clock source can use the internal clock. Basically, it has the same function as the 16-bit timer/counter mode and the interrupt occurs when T2CNTH/T2CNTL is equal to T2ADRH/T2ADRL. T2CNTH/T2CNTL valuesare automatically cleared by match signal and it can be also cleared by software (T2CC).

This timer interrupt in capture mode is very useful when the pulse width of captured signal is wider than the maximum period of timer.

The capture result is loaded into T2BDRH/T2BDRL. In the timer 2 capture mode, timer 2 output(T2O) waveform is not available.



NOTES:

1. T1 A Match is a pulse for the timer 2 clock source if it is selected.

Figure 37. 16-bit Capture Mode for Timer 2

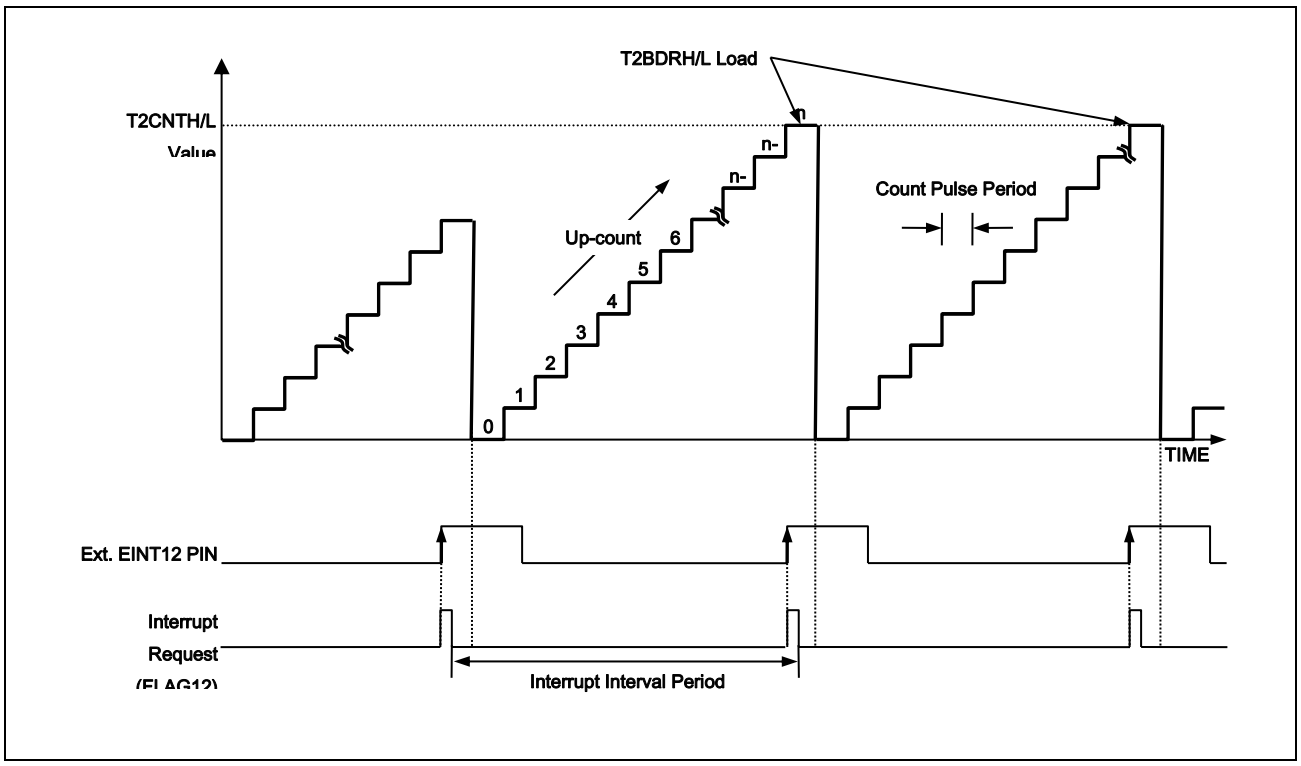


Figure 38. Input Capture Mode Operation for Timer 2

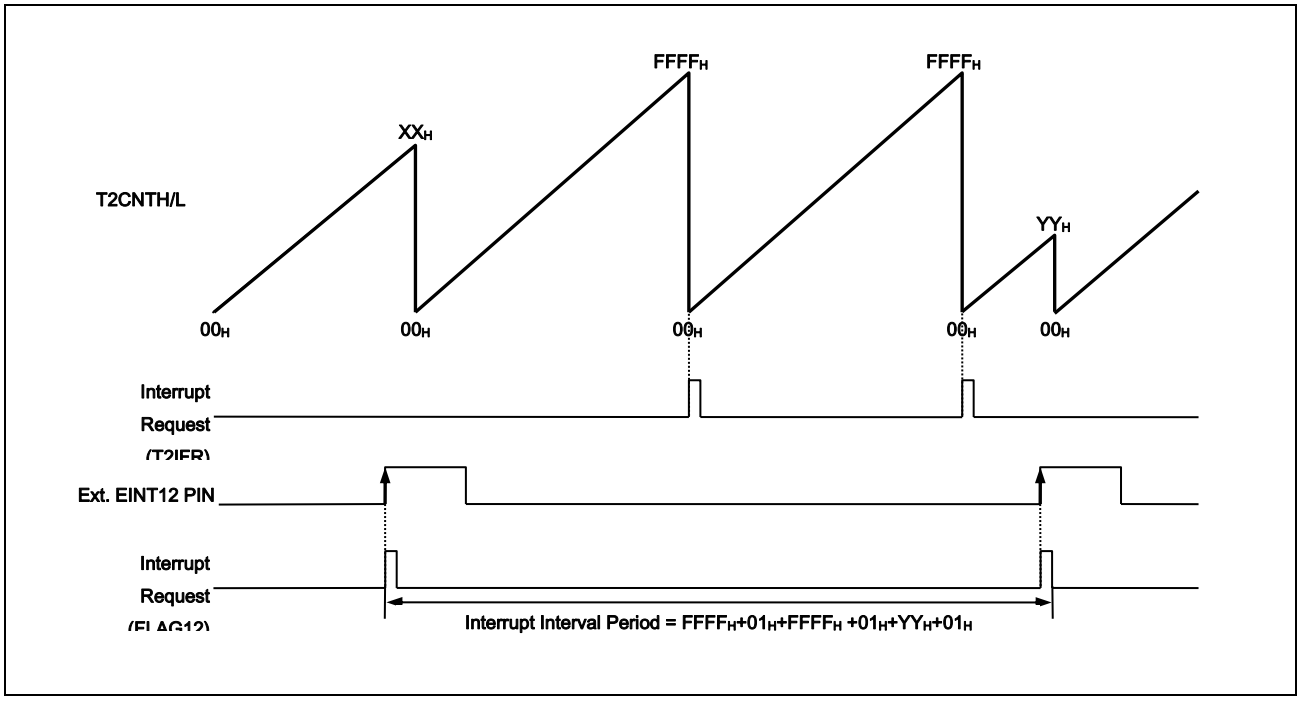
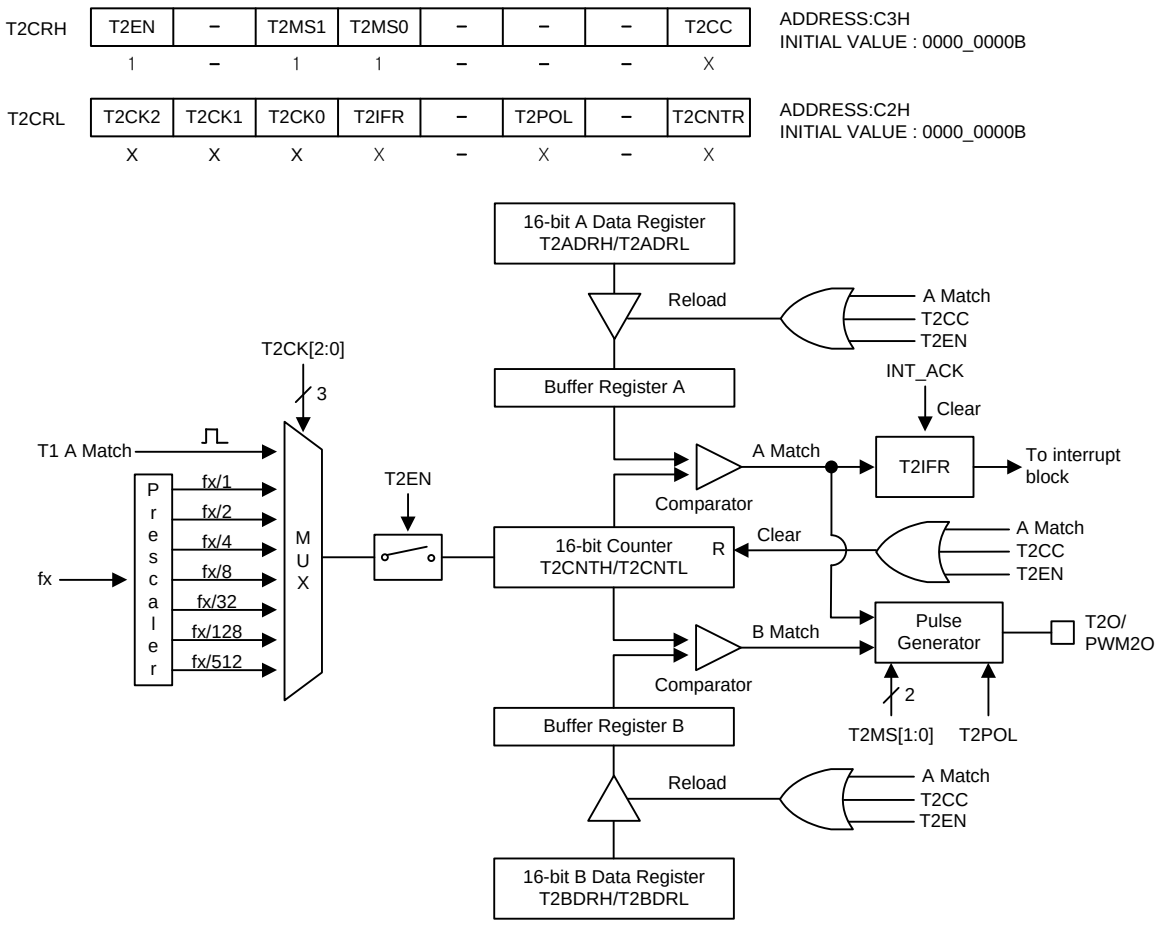


Figure 39. Express Timer Overflow in Capture Mode

11.3.4 16-bit PPG Mode

The timer 2 has a PPG (Programmable Pulse Generation) function. In PPG mode, the T2O/PWM2O pin outputs up to 16-bit resolution PWM output. This pin should be configured as a PWM output by set P1FSRL[5:4] to '11'. The period of the PWM output is determined by the T2ADRH/T2ADRL. And the duty of the PWM output is determined by the T2BDRH/T2BDRL.



NOTES:

1. The T2EN is automatically cleared to logic "0" after one pulse is generated at a PPG one-shot mode.
2. T1 A Match is a pulse for the timer 2 clock source if it is selected.

Figure 40. 16-bit PPG Mode for Timer 2

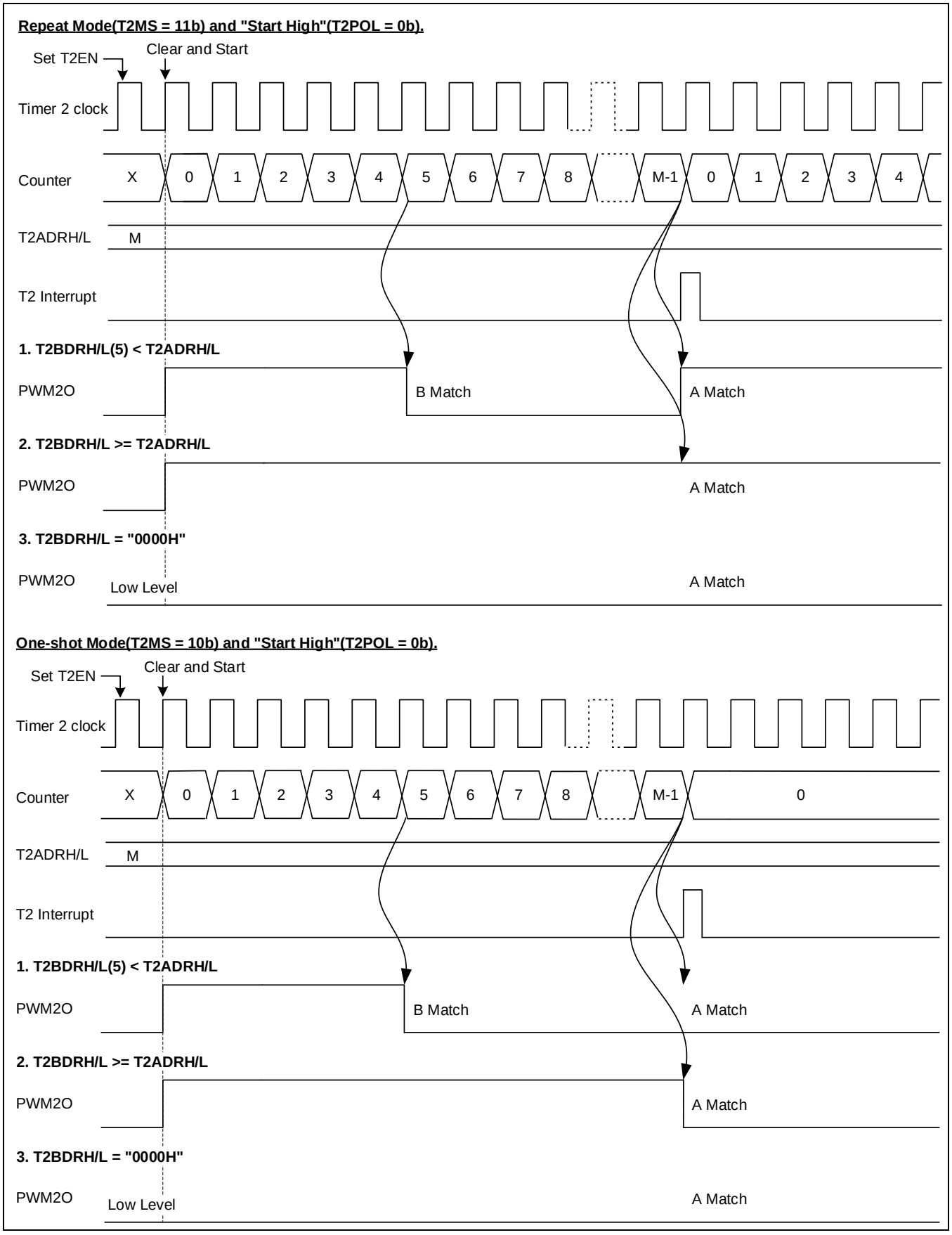
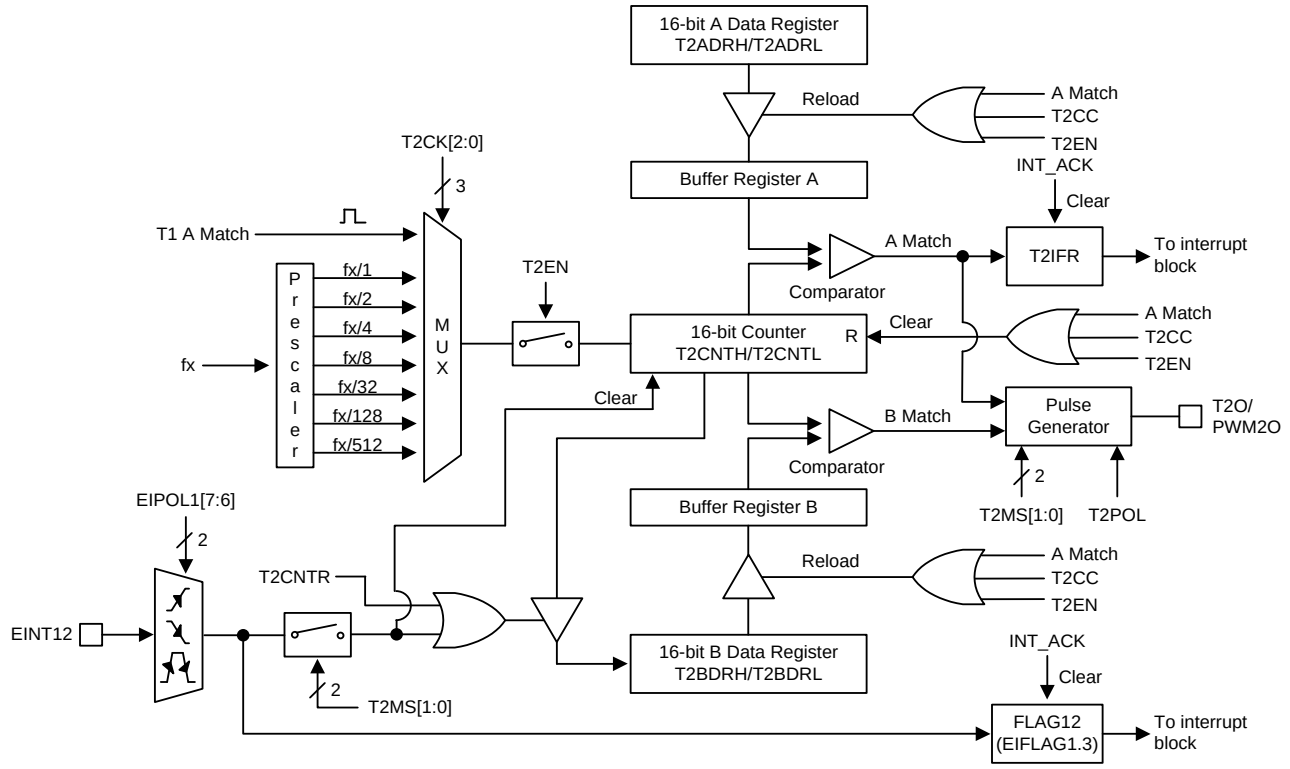


Figure 41. 16-bit PPG Mode Timming chart for Timer 2

11.3.5 Block Diagram



NOTES:

1. T1 A Match is a pulse for the timer 2 clock source if it is selected.

Figure 42. 16-bit Timer 2 Block Diagram

11.4 Timer 3

11.4.1 Overview

The 16-bit timer 3 consists of multiplexer, timer 3 A data register high/low, timer 3 B data register high/low and timer 3 control register high/low (T3ADRH, T3ADRL, T3BDRH, T3BDRL, T3CRH, and T3CRL).

It has four operating modes:

- 16-bit timer/counter mode
- 16-bit capture mode
- 16-bit PPG output mode (one-shot mode)
- 16-bit PPG output mode (repeat mode)

The timer/counter 3 can be clocked by an internal or an external clock source (EC3). The clock source is selected by clock selection logic which is controlled by the clock selection bits (T3CK[2:0]).

TIMER 3 clock source: f_X/1, 2, 4, 8, 64, 512, 2048 and EC3

In the capture mode, by EINT3, the data is captured into input capture data register (T3BDRH/T3BDRL). Timer 3 outputs the comparison result between counter and data register through T3O port in timer/counter mode. Also Timer 3 outputs PWM wave form through PWM3O port in the PPG mode.

Table 13. Timer 3 Operating Modes

T3EN	P0FSRL[3:2]	T3MS[1:0]	T3CK[2:0]	Timer 3
1	11	00	XXX	16-bit Timer/Counter Mode
1	00	01	XXX	16-bit Capture Mode
1	11	10	XXX	16-bit PPG Mode(one-shot mode)
1	11	11	XXX	16-bit PPG Mode(repeat mode)

11.4.2 16-bit Timer/Counter Mode

The 16-bit timer/counter mode is selected by control register as shown in Figure 43.

The 16-bit timer have counter and data register. The counter register is increased by internal or external clock input. Timer 3 can use the input clock with one of 1, 2, 4, 8, 64, 512 and 2048 prescaler division rates (T3CK[2:0]). When the value of T3CNTH, T3CNTL and the value of T3ADRH, T3ADRL are identical in Timer 3 respectively, a match signal is generated and the interrupt of Timer 3 occurs. The T3CNTH, T3CNTL value is automatically cleared by match signal.

It can be also cleared by software (T3CC).

The external clock (EC3) counts up the timer at the rising edge. If the EC3 is selected as a clock source by T3CK[2:0], EC3 port should be set to the input port by P00IO bit.

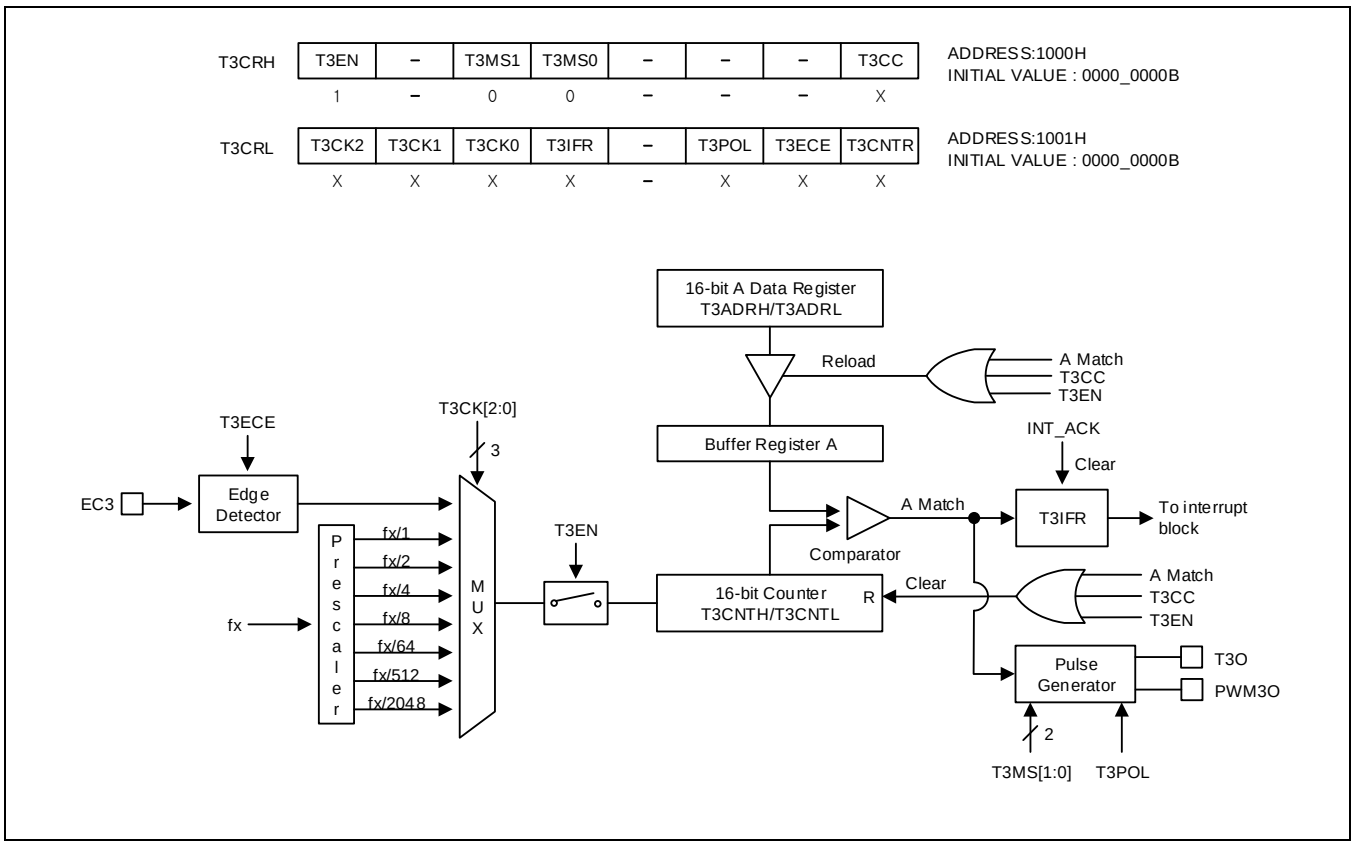


Figure 43. 16-bit Timer/Counter Mode for Timer 3

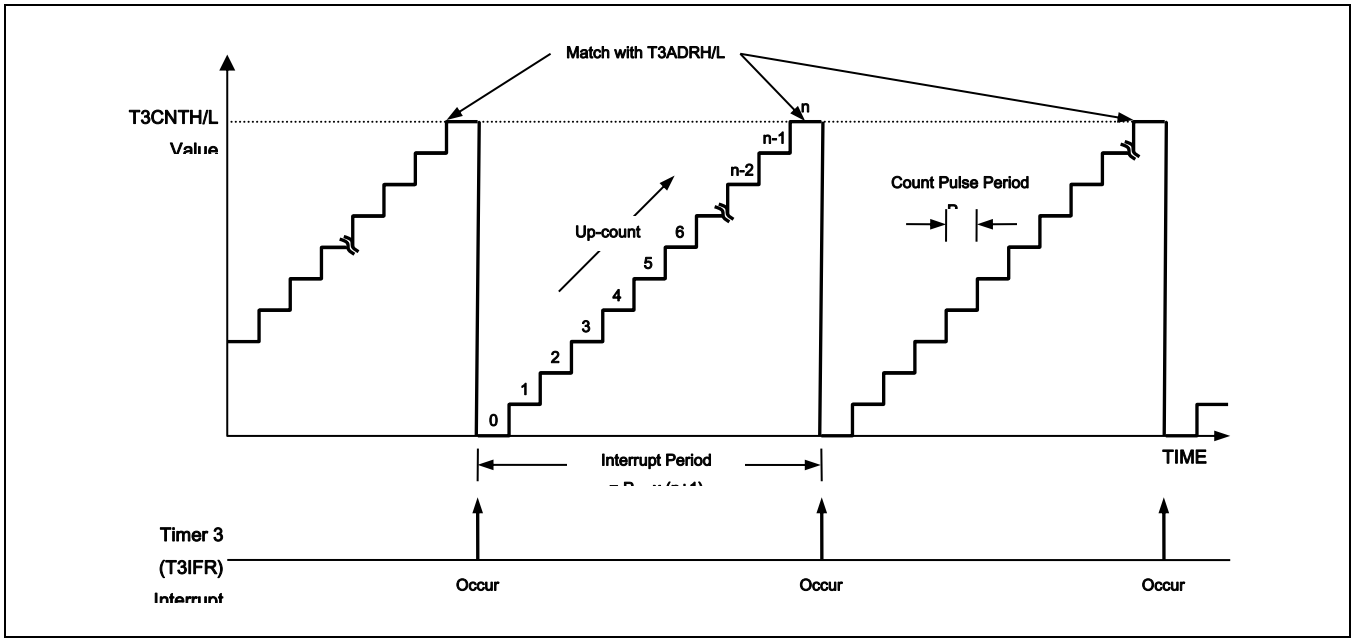


Figure 44. 16-bit Timer/Counter 3 Example

11.4.3 16-bit Capture Mode

The 16-bit timer 3 capture mode is set by T3MS[1:0] as '01'. The clock source can use the internal/external clock. Basically, it has the same function as the 16-bit timer/counter mode and the interrupt occurs when T3CNTH/T3CNTL is equal to T3ADRH/T3ADRL. The T3CNTH, T3CNTL values are automatically cleared by match signal. It can be also cleared by software (T3CC).

This timer interrupt in capture mode is very useful when the pulse width of captured signal is wider than the maximum period of timer.

The capture result is loaded into T3BDRH/T3BDRL.

According to EIPOL0 registers setting, the external interrupt EINT3 function is chosen. Of course, the EINT3 pin must be set as an input port.

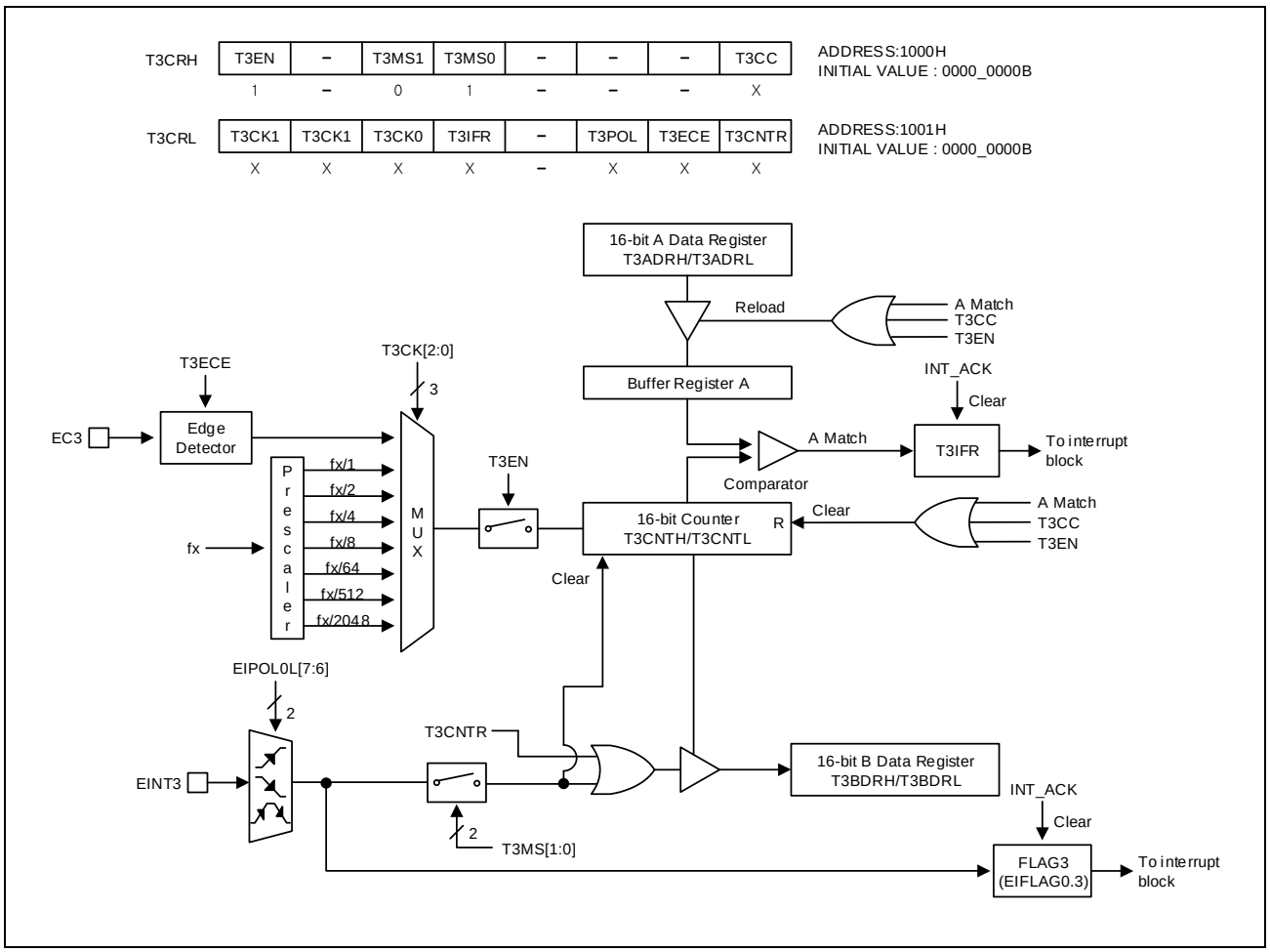


Figure 45. 16-bit Capture Mode for Timer 3

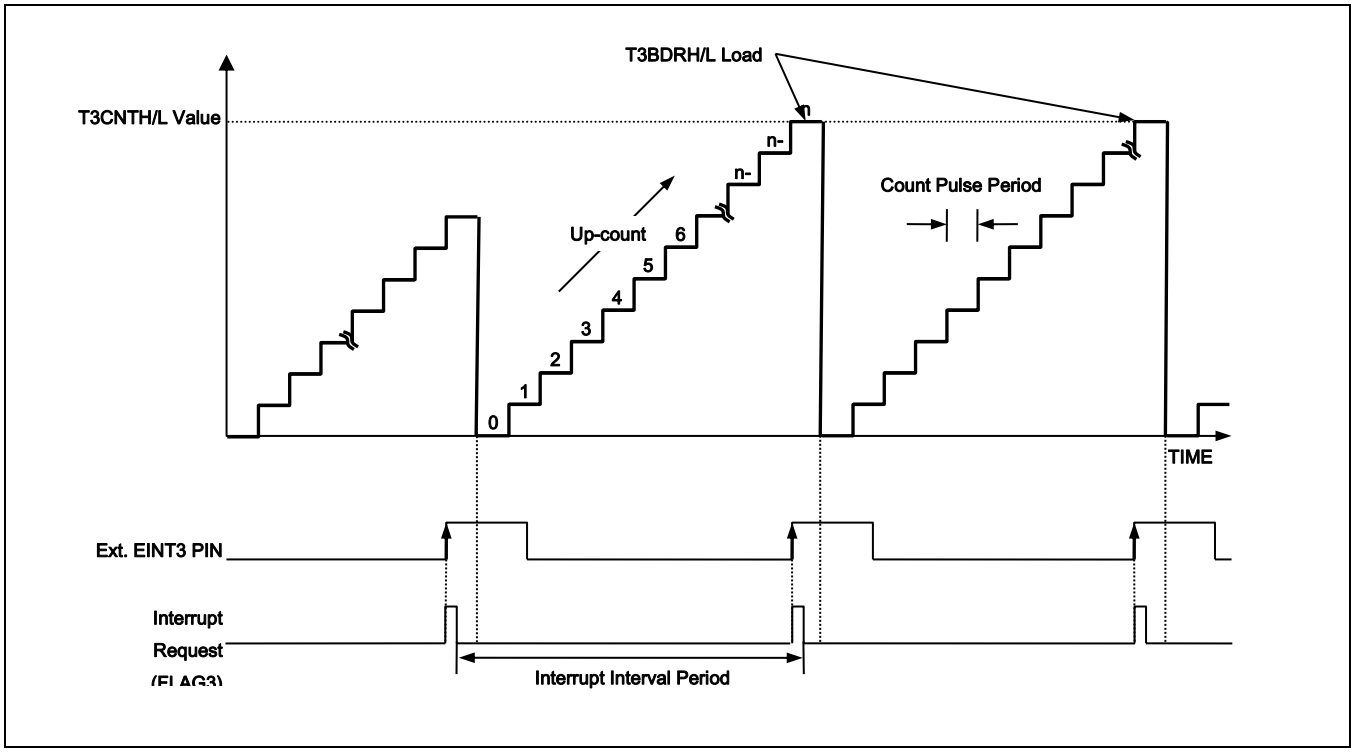


Figure 46. Input Capture Mode Operation for Timer 3

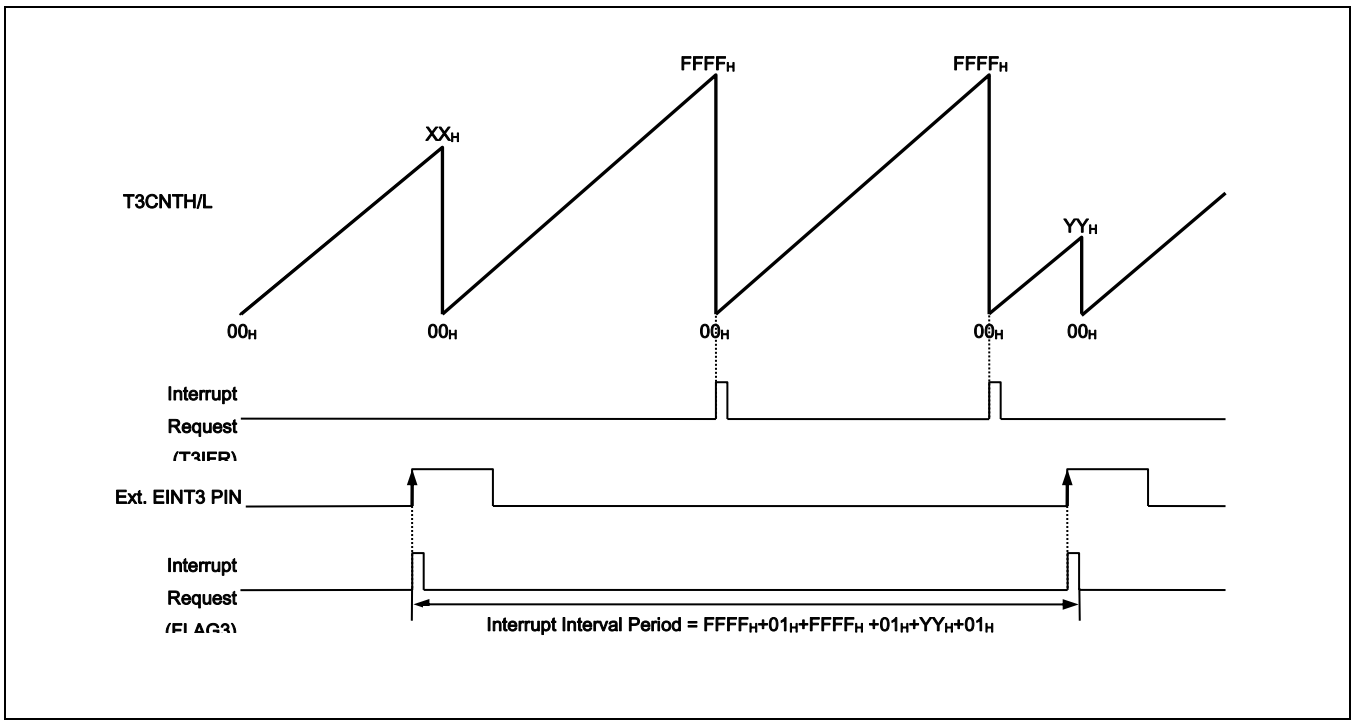
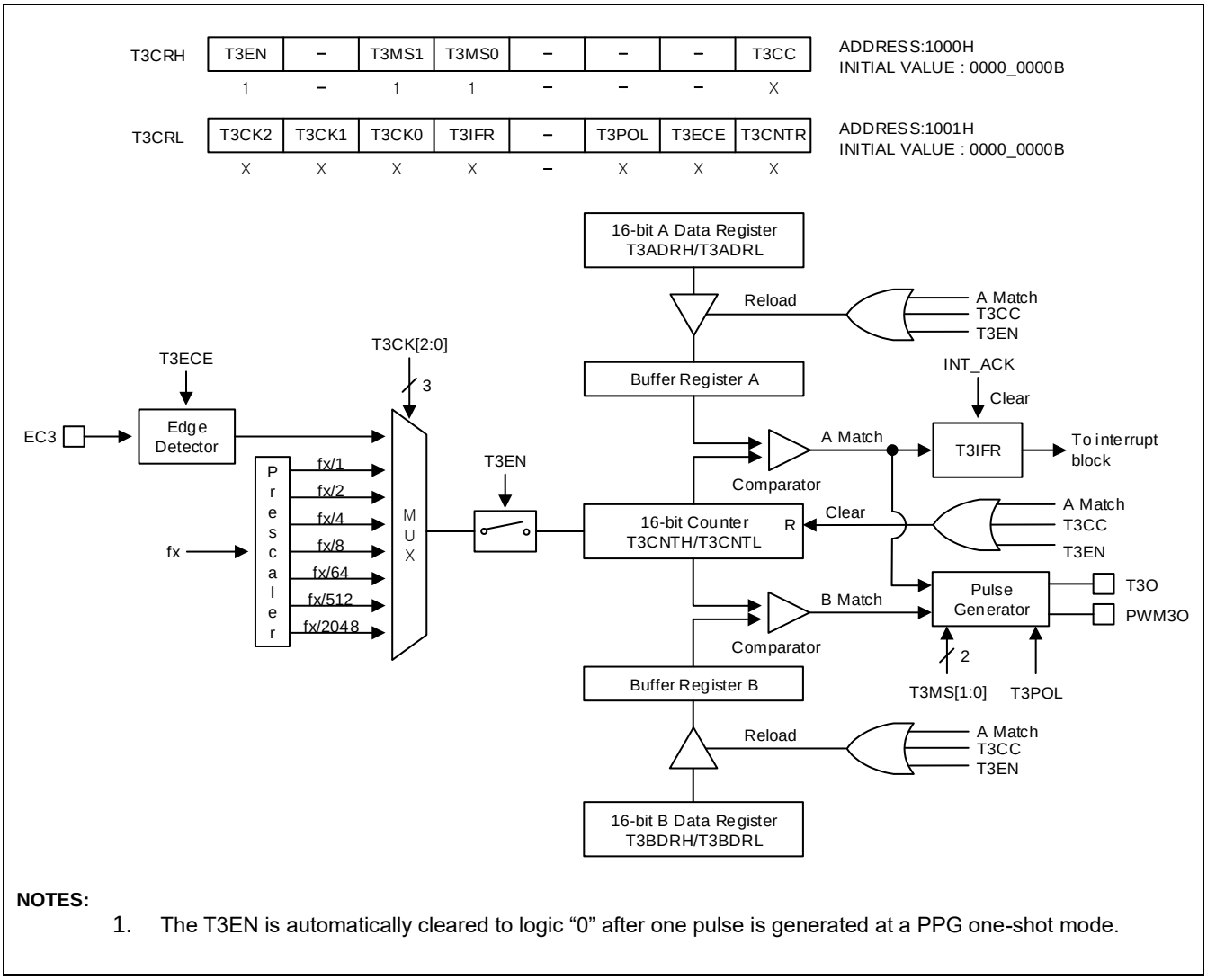


Figure 47. Express Timer Overflow in Capture Mode

11.4.4 16-bit PPG Mode

The timer 3 has a PPG (Programmable Pulse Generation) function. In PPG mode, T3O/PWM3O pin outputs up to 16-bit resolution PWM output. This pin should be configured as a PWM output by setting P0FSRH[3:2] to '11'. The period of the PWM output is determined by the T3ADRH/T3ADRL. And the duty of the PWM output is determined by the T3BDRH/T3BDRL.



NOTES:

1. The T3EN is automatically cleared to logic "0" after one pulse is generated at a PPG one-shot mode.

Figure 48. 16-bit PPG Mode for Timer 3

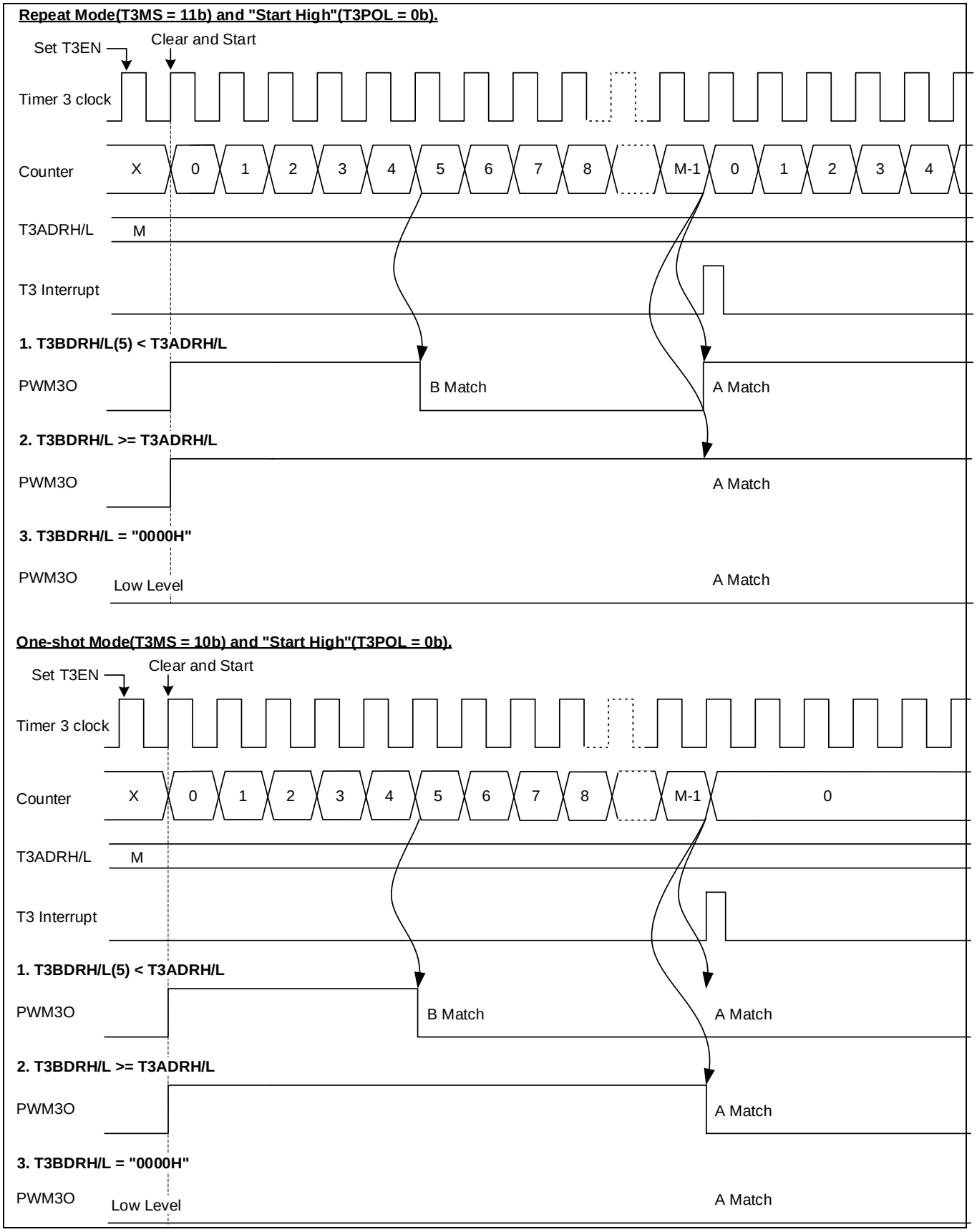


Figure 49. 16-bit PPG Mode Timming chart for Timer 3

11.4.5 Block Diagram

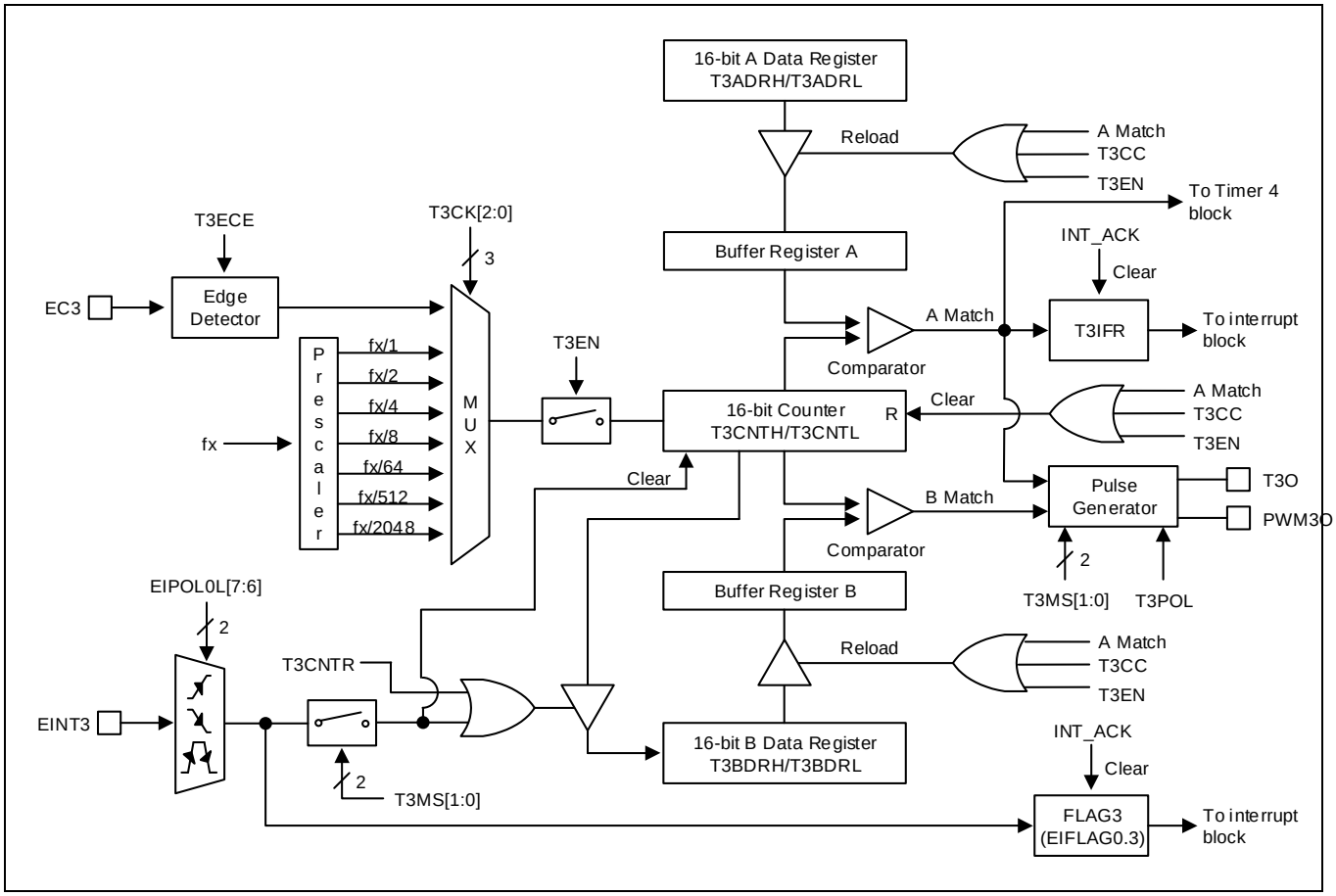


Figure 50. 16-Bit Timer 3 Block Diagram

11.5 Timer 4

11.5.1 Overview

The 16-bit TIMER 4 consists of multiplexer, timer 4 A data high/low register, timer 4 B data high/low register and timer 4 control high/low register (T4ADRH, T4ADRL, T4BDRH, T4BDRL, T4CRH, and T4CRL).

It has four operating modes:

- 16-bit timer/counter mode
- 16-bit capture mode
- 16-bit PPG output mode (one-shot mode)
- 16-bit PPG output mode (repeat mode)

The timer/counter 4 can be divided clock of the system clock selected from prescaler output and T3 A Match (timer 3 A match signal). The clock source is selected by clock selection logic which is controlled by the clock selection bits (T4CK[2:0]).

TIMER 4 clock source: $f_X/1$, $f_X/2$, $f_X/4$,$f_X/8$,$f_X/32$, $f_X/128$, $f_X/512$ and T3 A Match

In the capture mode, by EINT4, the data is captured into input capture data register (T4BDRH/T4BDRL). In timer/counter mode, whenever counter value is equal to T4ADRH/L, T4O port toggles. Also the TIMER 4 outputs PWM wave form to PWM4O port in the PPG mode.

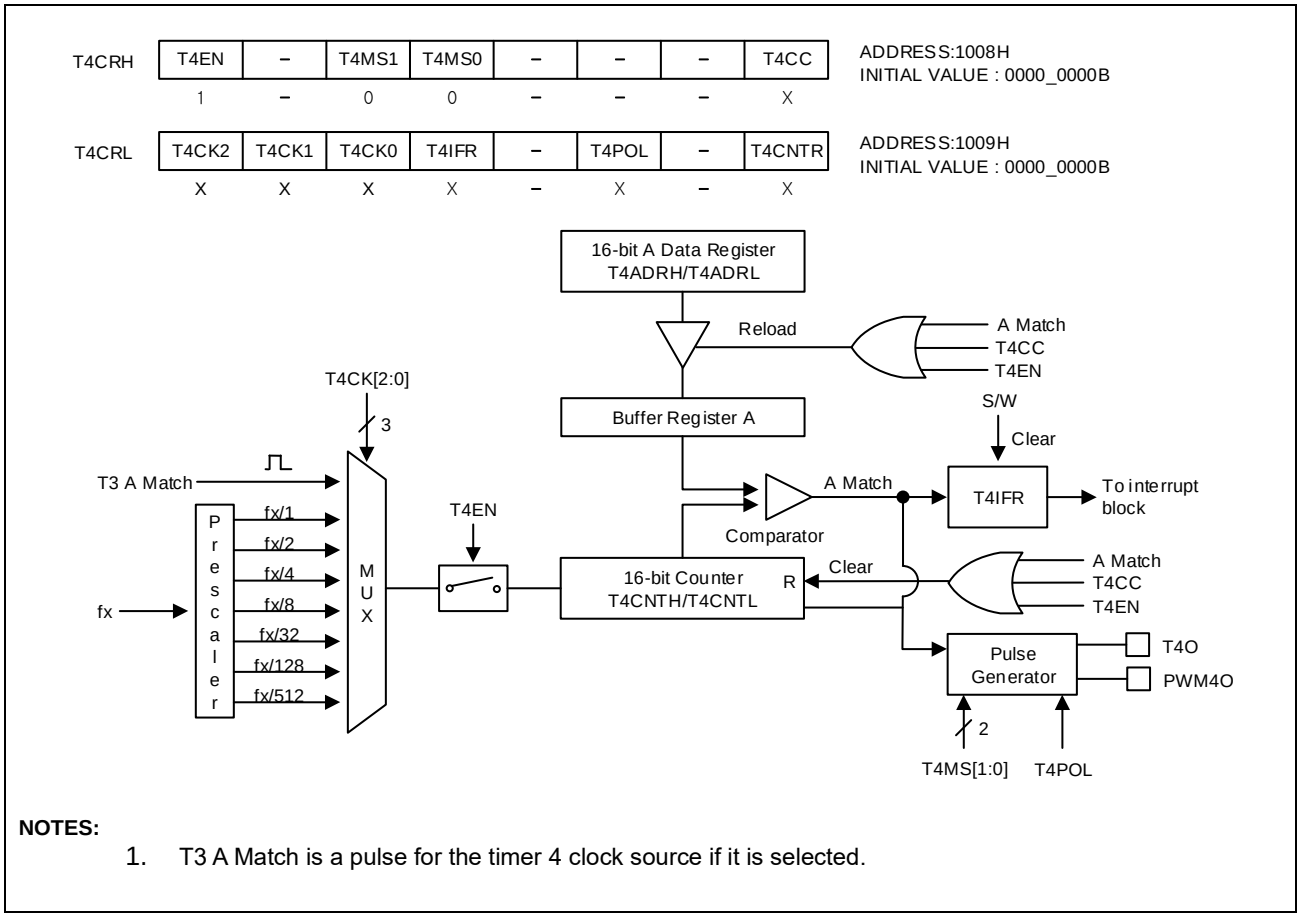
Table 14. TIMER 4 Operating Modes

T4EN	P0FSRH[5:4]	T4MS[1:0]	T4CK[2:0]	TIMER 4
1	11	00	XXX	16-bit Timer/Counter Mode
1	00	01	XXX	16-bit Capture Mode
1	11	10	XXX	16-bit PPG Mode (one-shot mode)
1	11	11	XXX	16-bit PPG Mode (repeat mode)

11.5.2 16-bit Timer/Counter Mode

The 16-bit timer/counter mode is selected by control register as shown in Figure 51.

The 16-bit timer have counter and data register. The counter register is increased by internal or timer 3 A match clock input. Timer 4 can use the input clock with one of 1, 2, 4, 8, 32, 128, 512 and T3 A Match prescaler division rates (T4CK[2:0]). When the values of T4CNTH/T4CNTL and T4ADRH/T4ADRL are identical in timer 4, a match signal is generated and the interrupt of Timer 4 occurs.The T4CNTH/T4CNTL values are automatically cleared by match signal. It can be also cleared by software (T4CC).



NOTES:

1. T3 A Match is a pulse for the timer 4 clock source if it is selected.

Figure 51. 16-bit Timer/Counter Mode for Timer 4

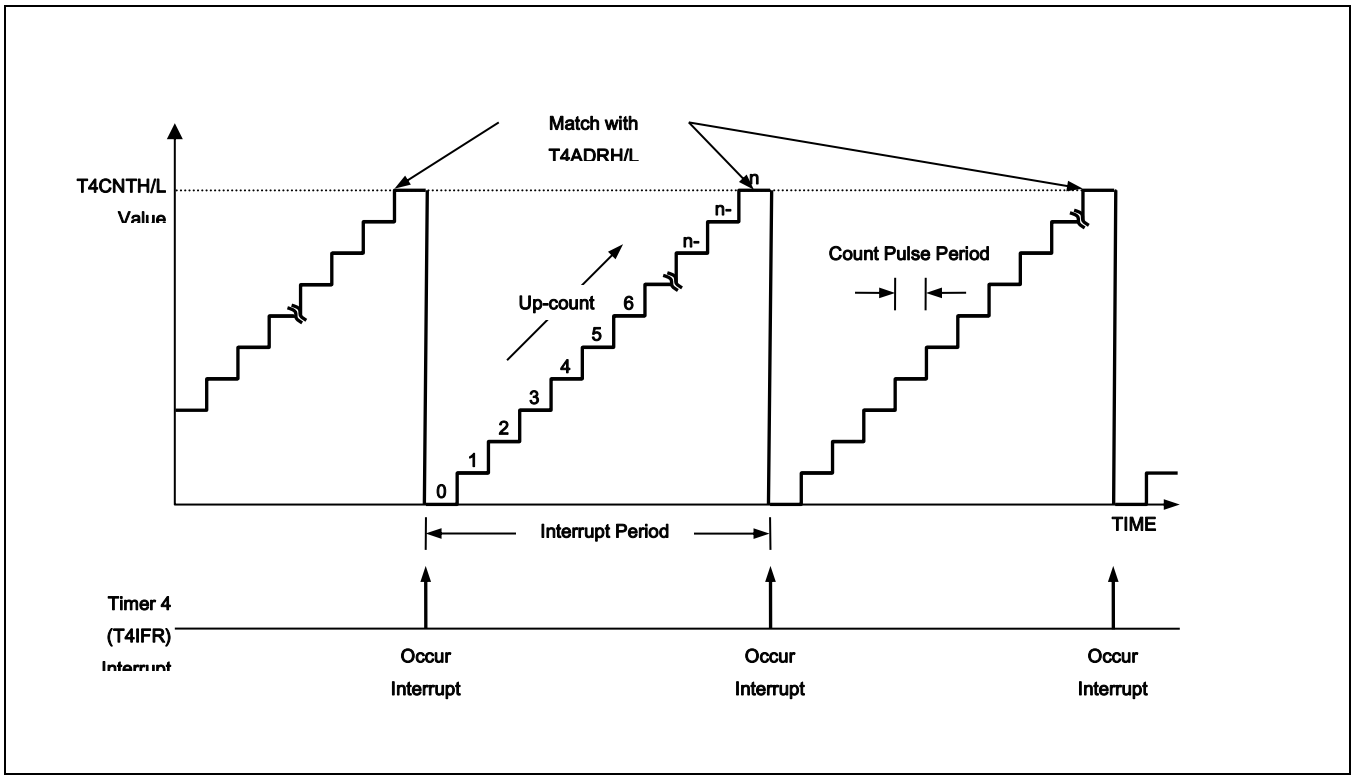


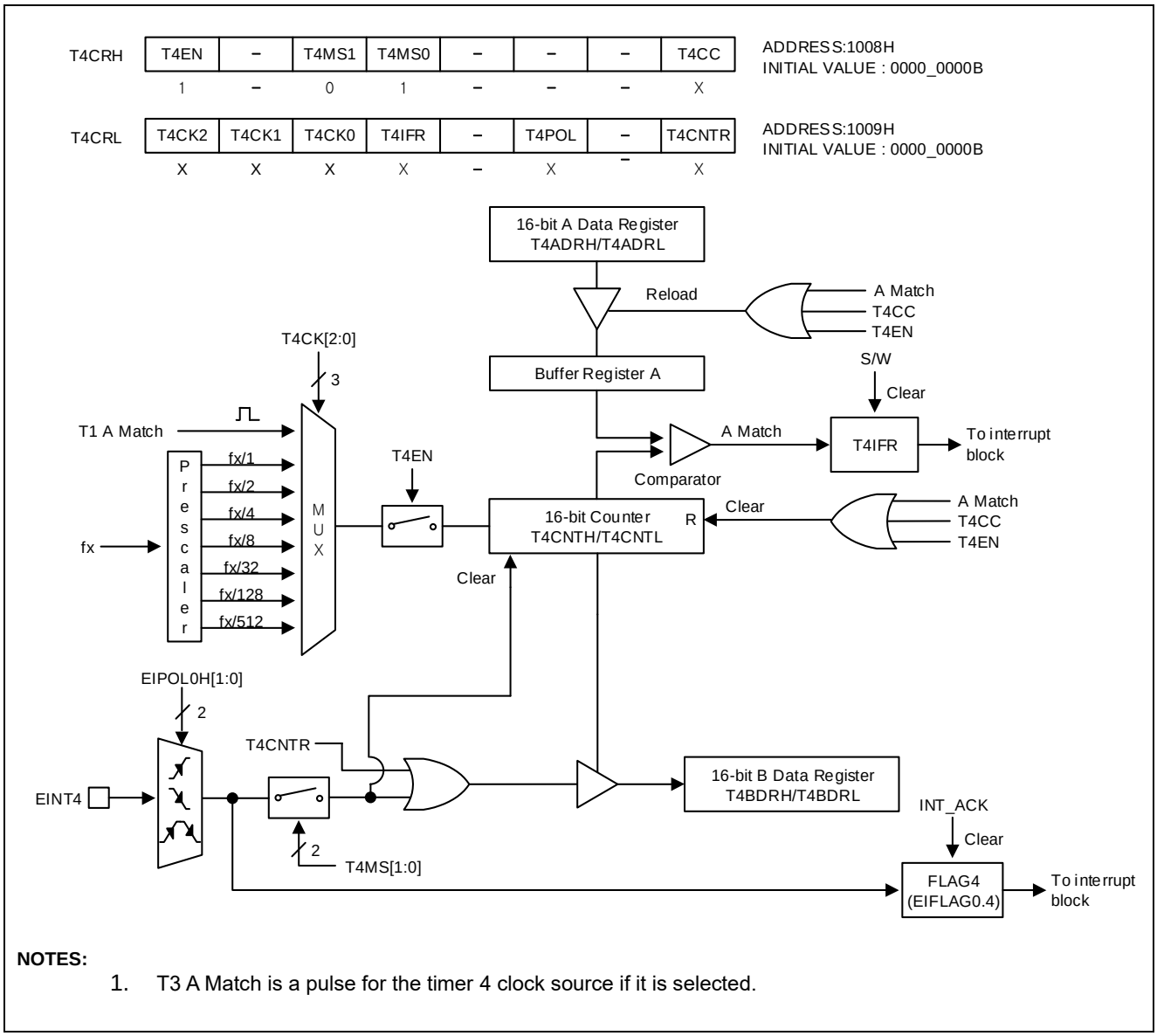
Figure 52. 16-bit Timer/Counter 4 Example

11.5.3 16-bit Capture Mode

The timer 4 capture mode is set by T4MS[1:0] as '01'. The clock source can use the internal clock. Basically, it has the same function as the 16-bit timer/counter mode and the interrupt occurs when T4CNTH/T4CNTL is equal to T4ADRH/T4ADRL. T4CNTH/T4CNTL values are automatically cleared by match signal and it can be also cleared by software (T4CC).

This timer interrupt in capture mode is very useful when the pulse width of captured signal is wider than the maximum period of timer.

The capture result is loaded into T4BDRH/T4BDRL. In the timer 4 capture mode, timer 4 output (T4O) waveform is not available.



NOTES:

1. T3 A Match is a pulse for the timer 4 clock source if it is selected.

Figure 53. 16-bit Capture Mode for Timer 4

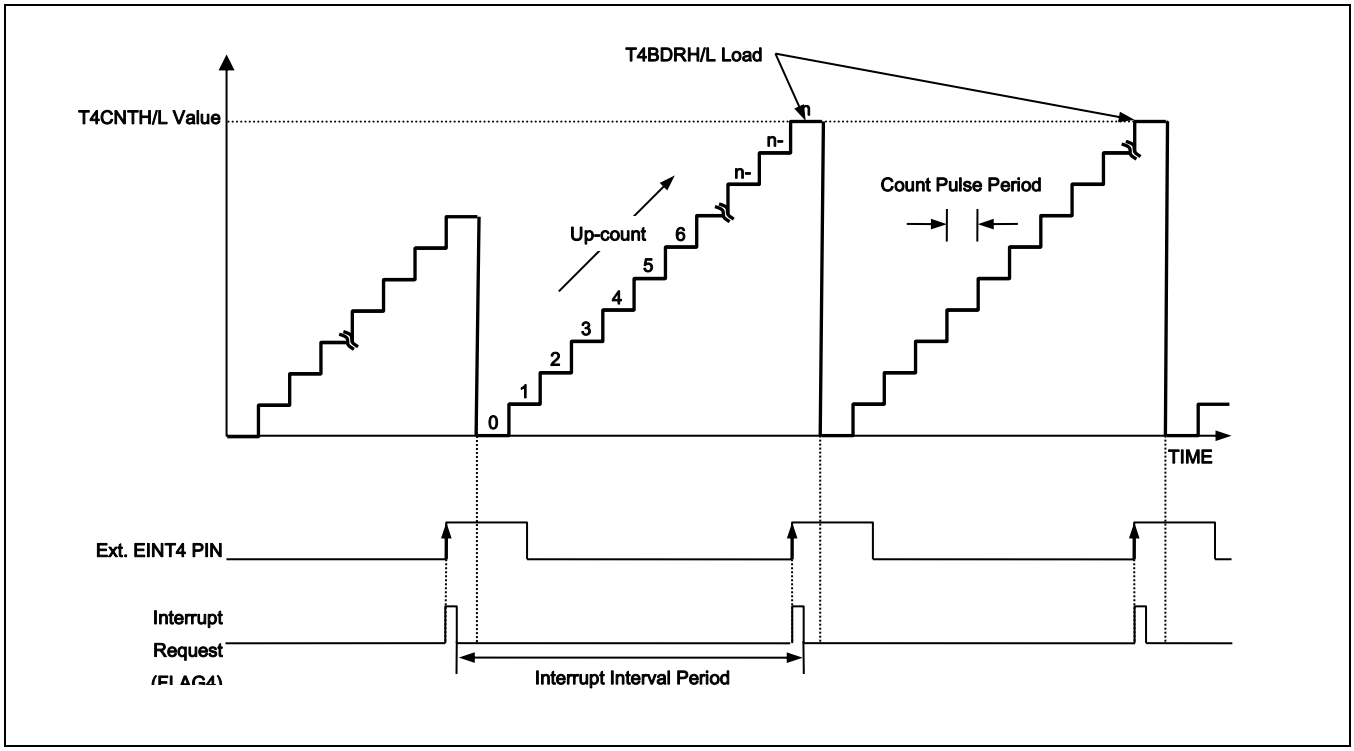


Figure 54. Input Capture Mode Operation for Timer 4

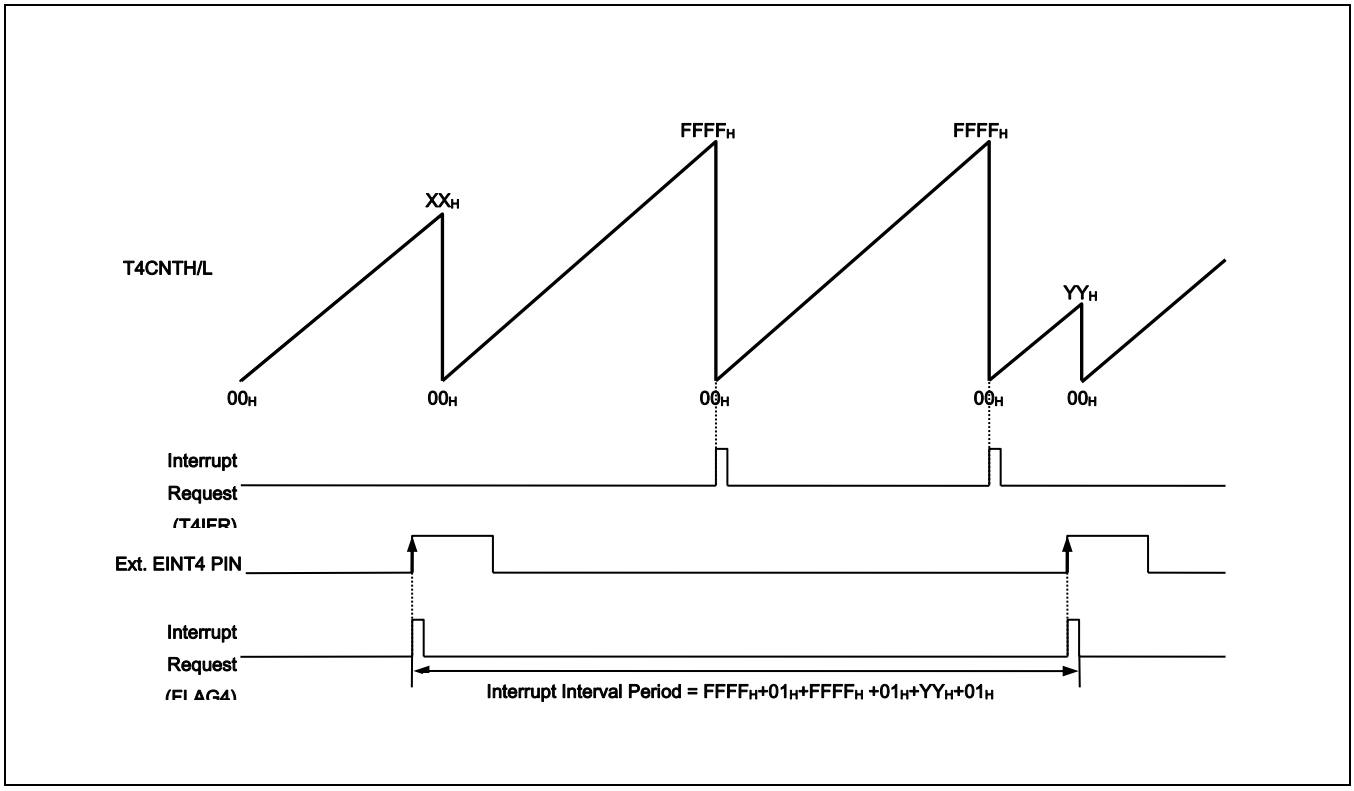
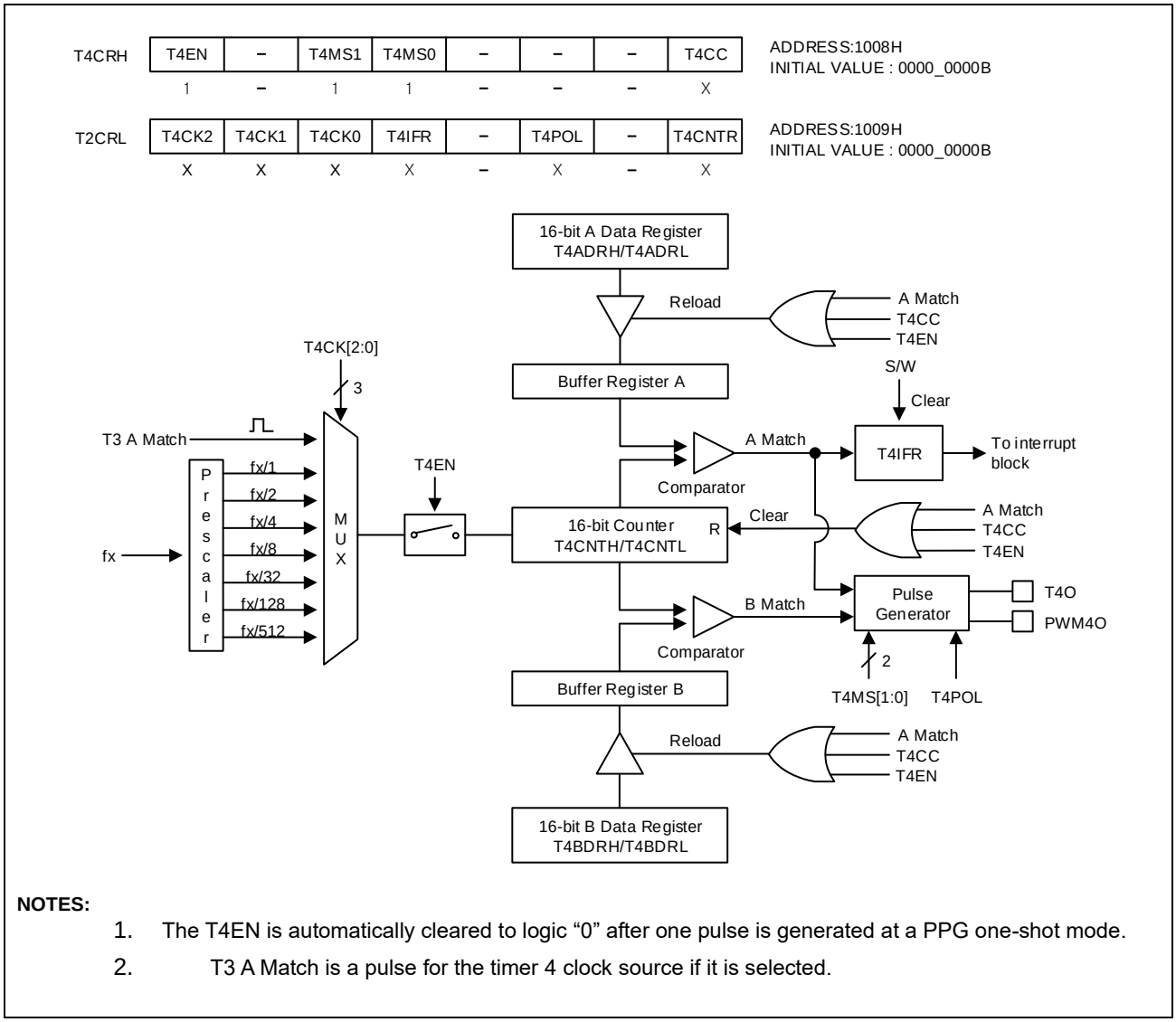


Figure 55. Express Timer Overflow in Capture Mode

11.5.4 16-bit PPG Mode

The timer 4 has a PPG (Programmable Pulse Generation) function. In PPG mode, the T4O/PWM4O pin outputs up to 16-bit resolution PWM output. This pin should be configured as a PWM output by set P0FSRH[5:4] to '11'. The period of the PWM output is determined by the T4ADRH/T4ADRL. And the duty of the PWM output is determined by the T4BDRH/T4BDRL.



NOTES:

1. The T4EN is automatically cleared to logic "0" after one pulse is generated at a PPG one-shot mode.
2. T3 A Match is a pulse for the timer 4 clock source if it is selected.

Figure 56. 16-bit PPG Mode for Timer 4

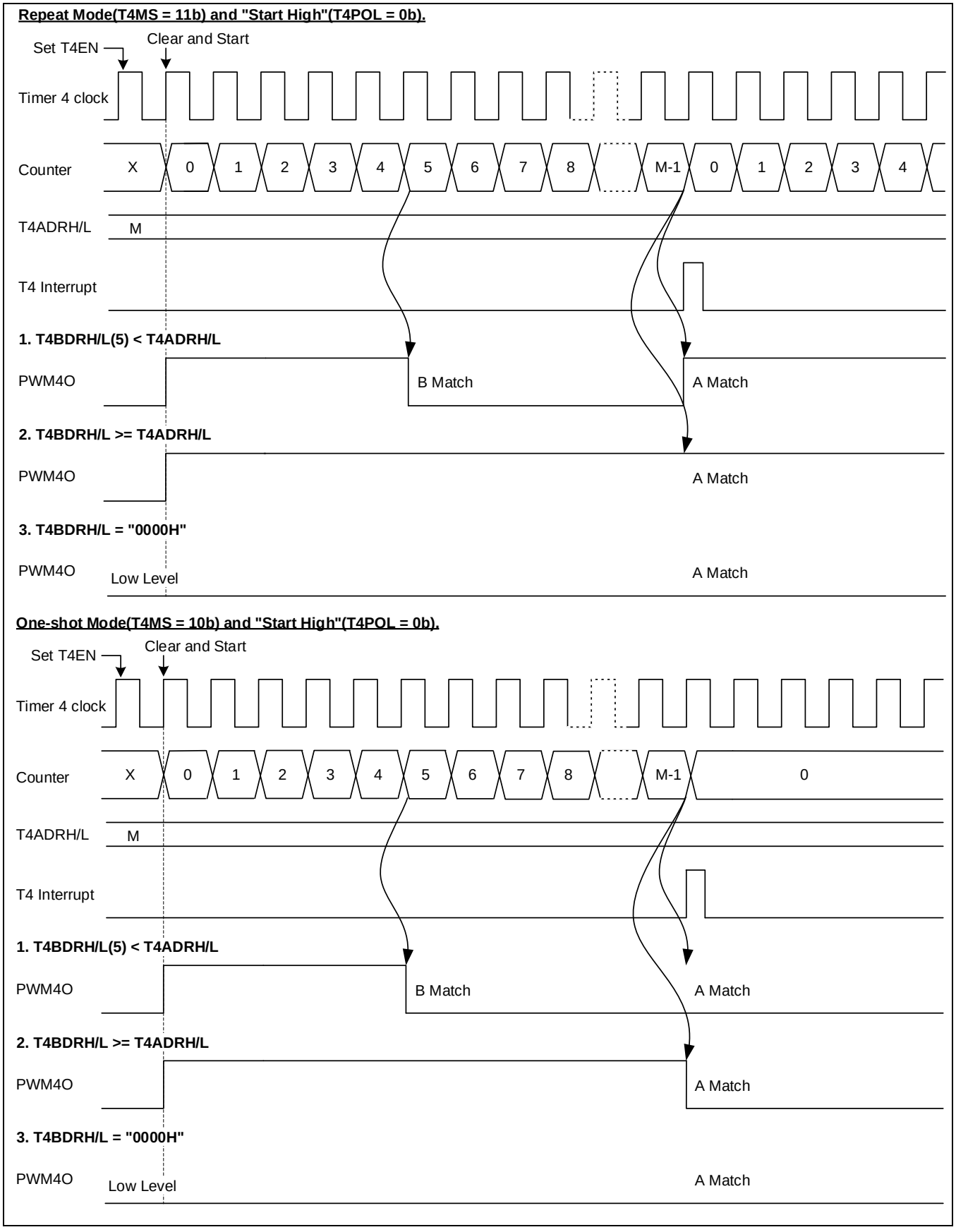
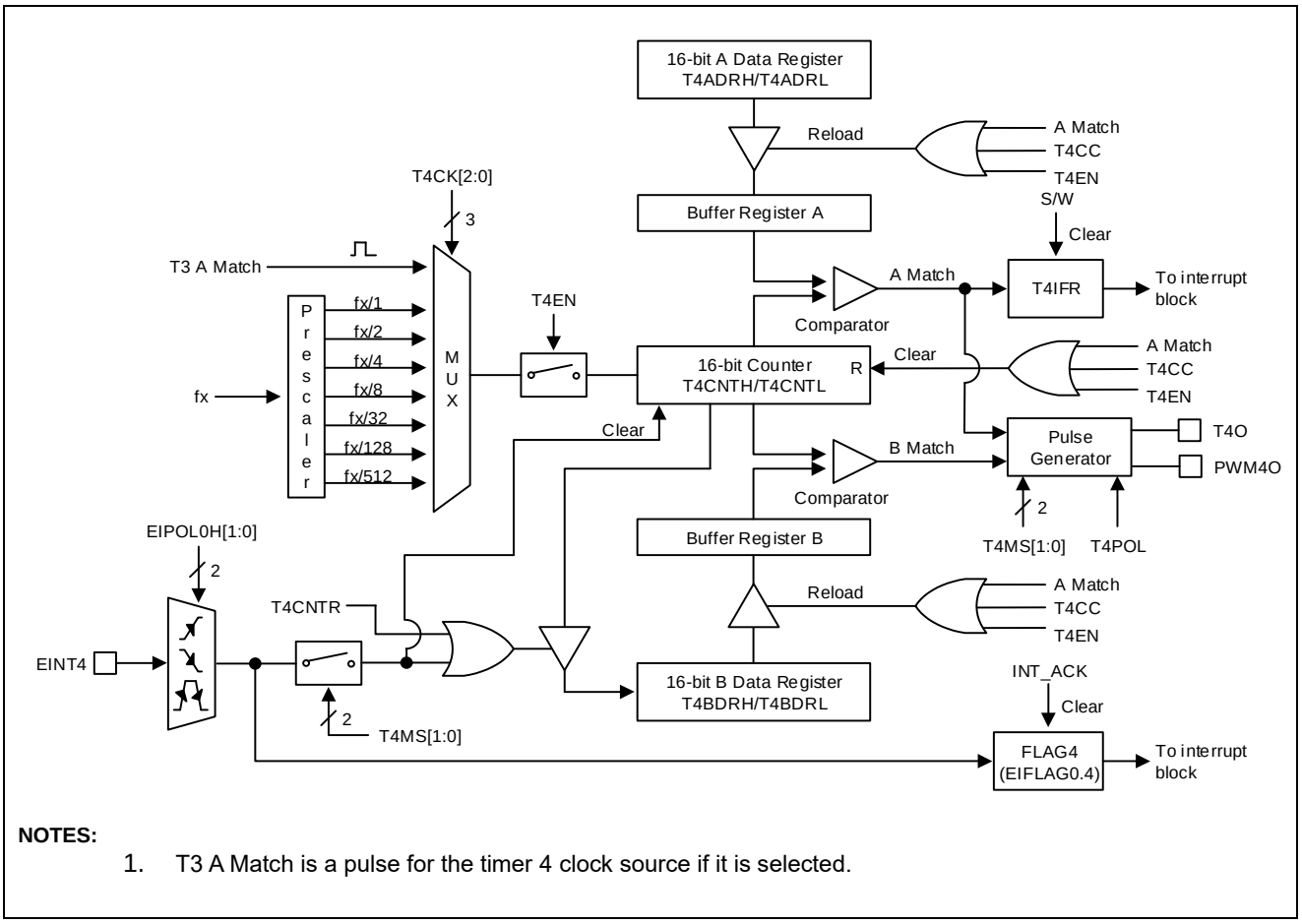


Figure 57. 16-bit PPG Mode Timming chart for Timer 4

11.5.5 Block Diagram



NOTES:

1. T3 A Match is a pulse for the timer 4 clock source if it is selected.

Figure 58. 16-bit Timer 4 Block Diagram

11.6 Timer 5

11.6.1 Overview

The 16-bit TIMER 5 consists of multiplexer, timer 5 A data high/low register, timer 5 B data high/low register and timer 5 control high/low register (T5ADRH, T5ADRL, T5BDRH, T5BDRL, T5CRH, and T5CRL).

It has four operating modes:

- 16-bit timer/counter mode
- 16-bit capture mode
- 16-bit PPG output mode (one-shot mode)
- 16-bit PPG output mode (repeat mode)

The timer/counter 5 can be divided clock of the system clock selected from prescaler output.

The clock source is selected by clock selection logic which is controlled by the clock selection bits (T5CK[2:0]).

TIMER 5 clock source: $f_X/1$, $f_X/2$, $f_X/4$,$f_X/8$,$f_X/32$, $f_X/128$, $f_X/512$ and HSIRC

In the capture mode, by EINT5, the data is captured into input capture data register (T5BDRH/T5BDRL). In timer/counter mode, whenever counter value is equal to T5ADRH/L, T5O port toggles. Also the TIMER 5 outputs PWM wave form to PWM5O port in the PPG mode.

Table 15. TIMER 5 Operating Modes

T5EN	P0FSRH[5:4]	T5MS[1:0]	T5CK[2:0]	TIMER 5
1	11	00	XXX	16-bit Timer/Counter Mode
1	00	01	XXX	16-bit Capture Mode
1	11	10	XXX	16-bit PPG Mode (one-shot mode)
1	11	11	XXX	16-bit PPG Mode (repeat mode)

11.6.2 16-bit Timer/Counter Mode

The 16-bit timer/counter mode is selected by control register as shown in Figure 62.

The 16-bit timer have counter and data register. The counter register is increased by internal clock input. Timer 5 can use the input clock with one of 1, 2, 4, 8, 32, 128, 512 and High Frequency Internal Oscillator (HSIRC) prescaler division rates (T5CK[2:0]). When the values of T5CNTH/T5CNTL and T5ADRH/T5ADRL are identical in timer 5, a match signal is generated and the interrupt of Timer 5 occurs. The T5CNTH/T5CNTL values are automatically cleared by match signal. It can be also cleared by software (T5CC).

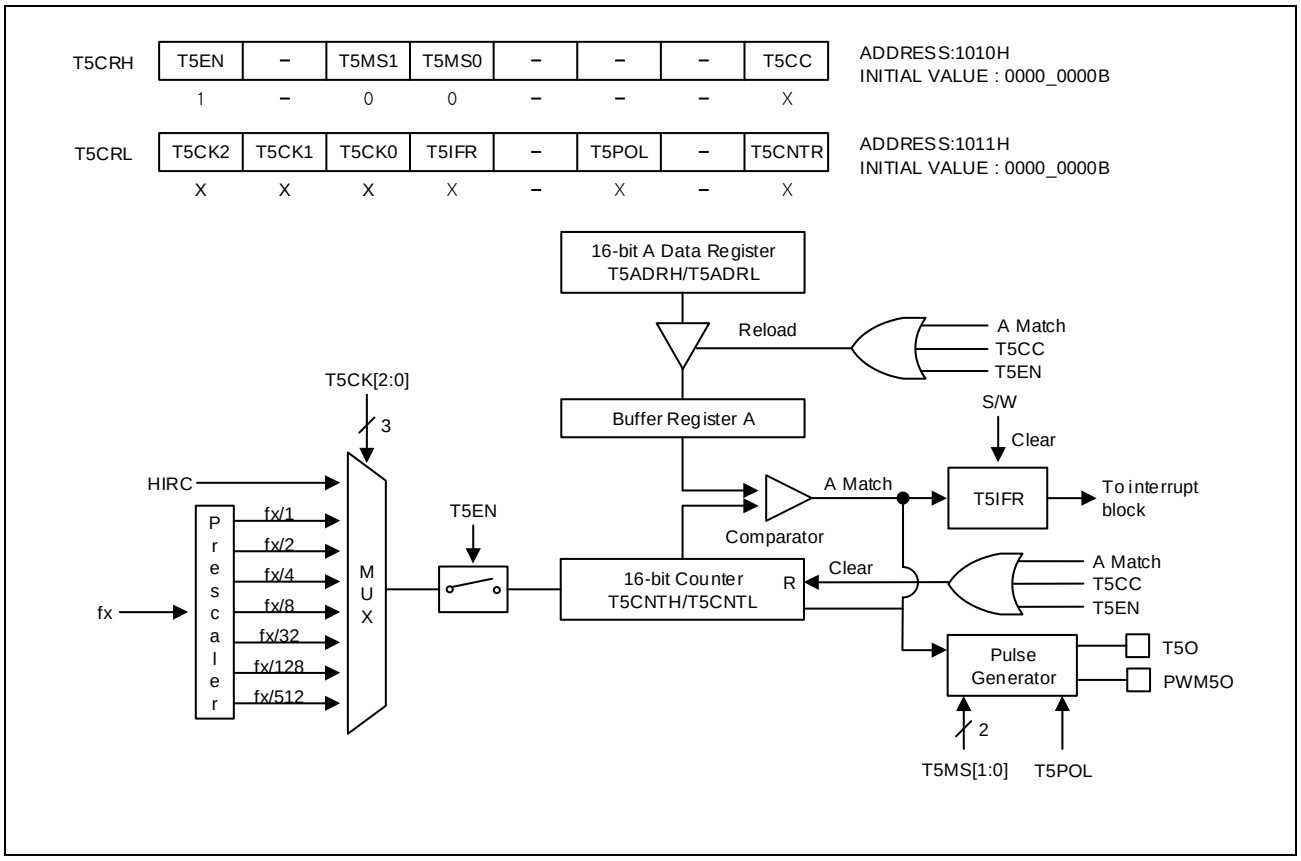


Figure 59. 16-bit Timer/Counter Mode for Timer 5

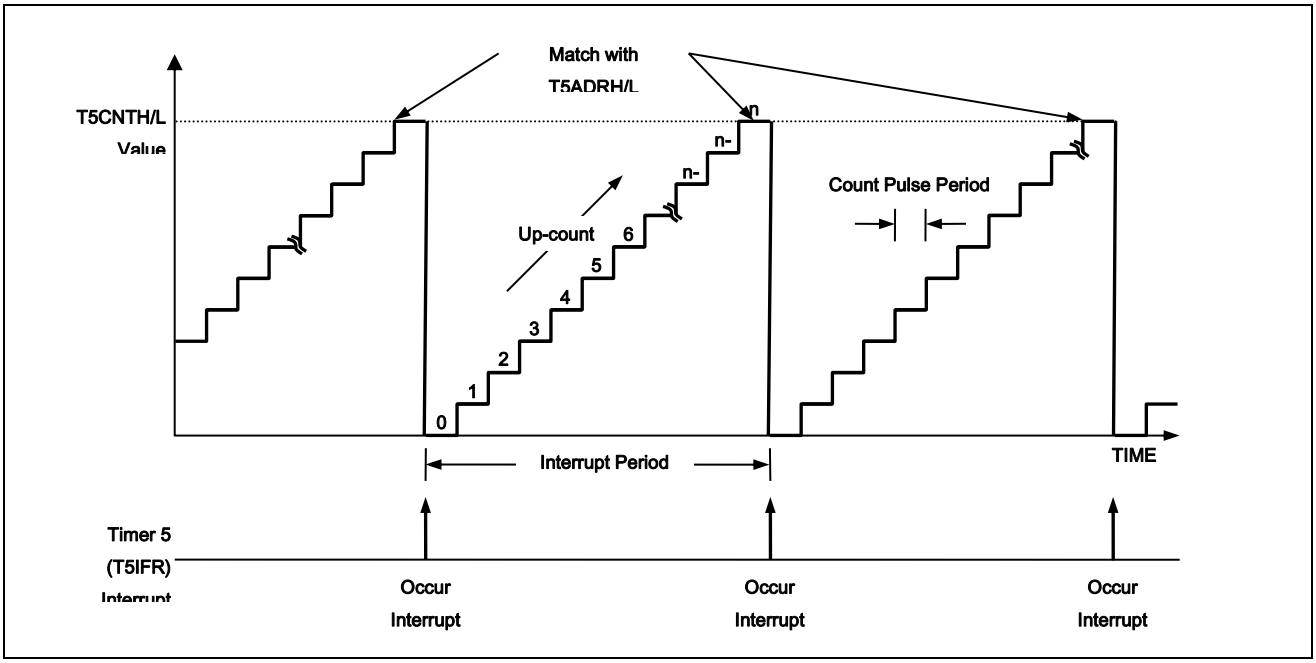


Figure 60. 16-bit Timer/Counter 4 Example

11.6.3 16-bit Capture Mode

The timer 5 capture mode is set by T5MS[1:0] as '01'. The clock source can use the internal clock. Basically, it has the same function as the 16-bit timer/counter mode and the interrupt occurs when T5CNTH/T5CNTL is equal to T5ADRH/T5ADRL. T5CNTH/T5CNTL values are automatically cleared by match signal and it can be also cleared by software (T5CC).

This timer interrupt in capture mode is very useful when the pulse width of captured signal is wider than the maximum period of timer.

The capture result is loaded into T5BDRH/T5BDRL. In the timer 5 capture mode, timer 5 output (T5O) waveform is not available.

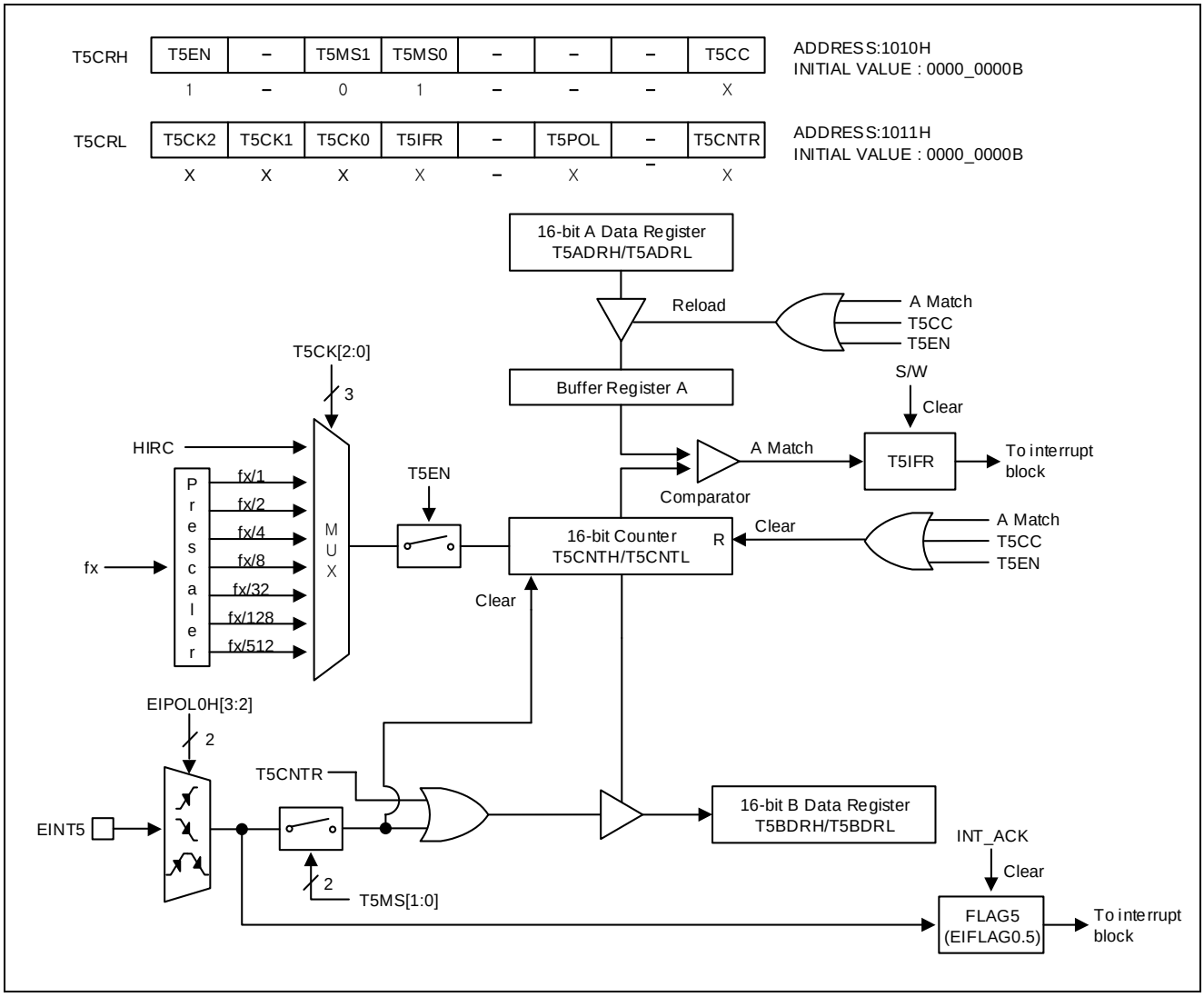


Figure 61. 16-bit Capture Mode for Timer 5

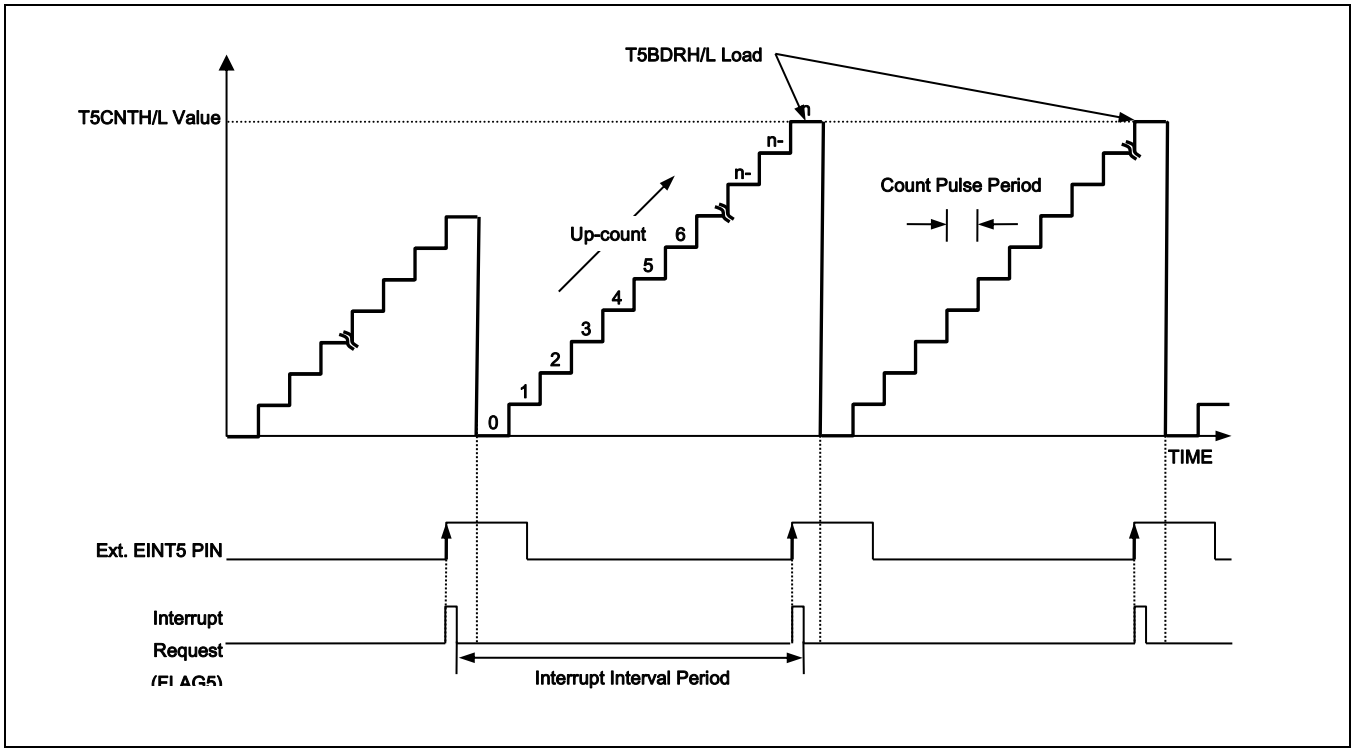


Figure 62. Input Capture Mode Operation for Timer 5

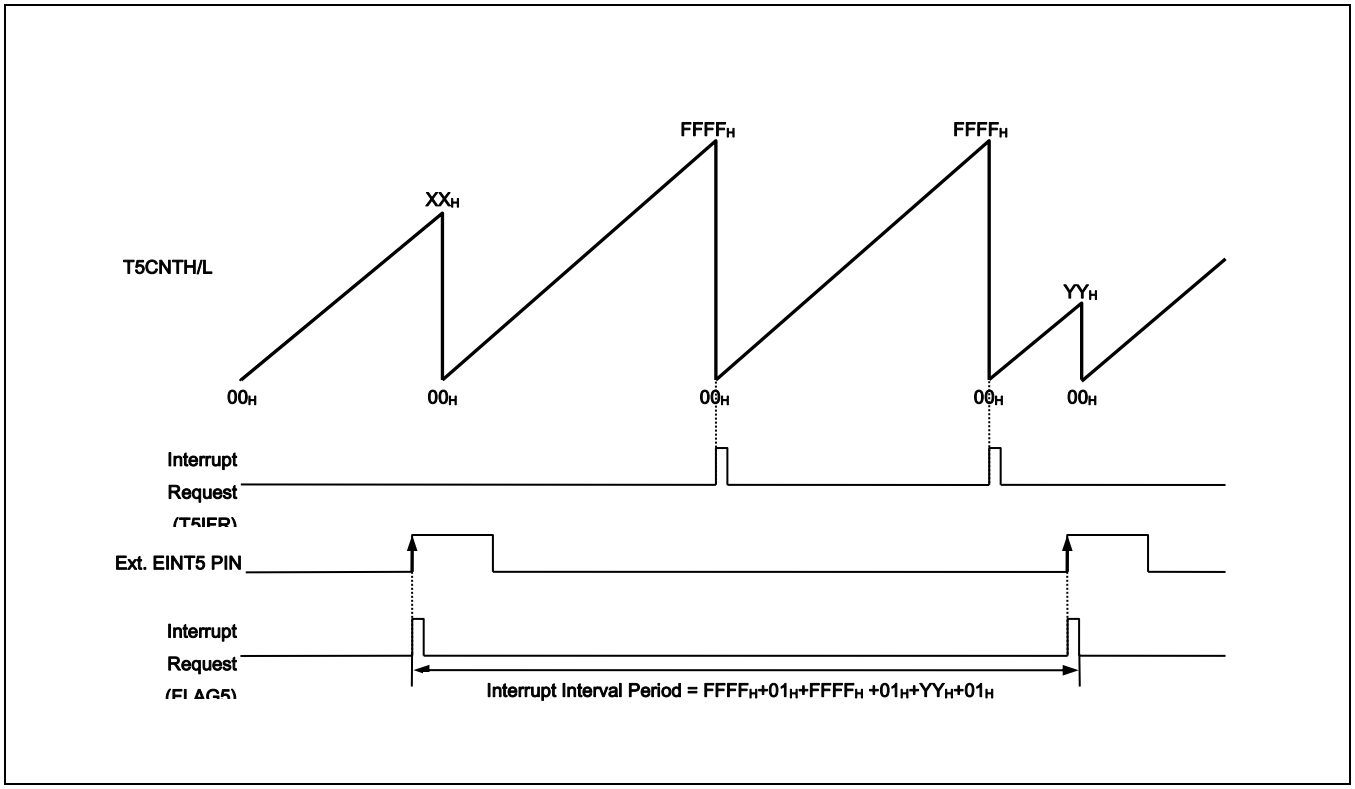
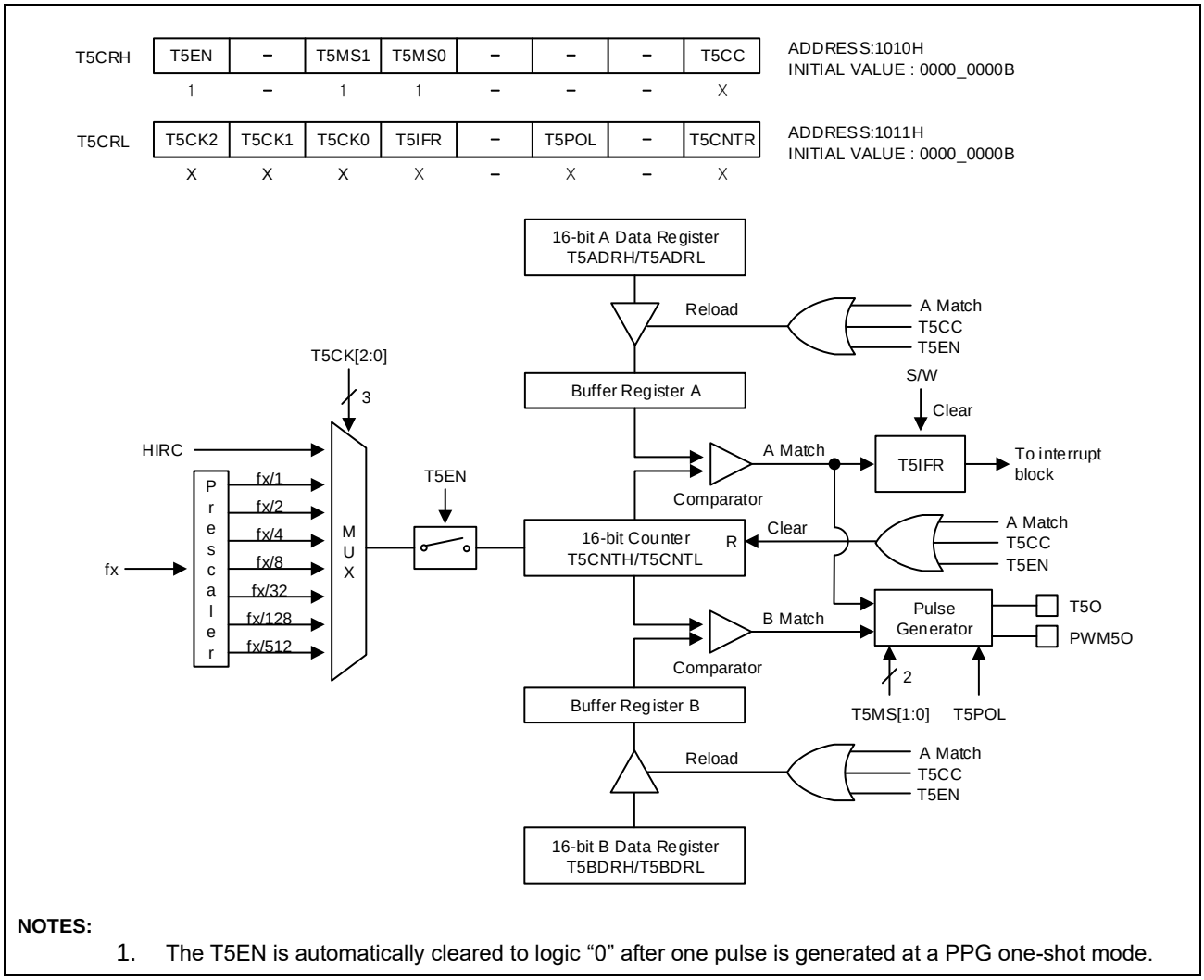


Figure 63. Express Timer Overflow in Capture Mode

11.6.4 16-bit PPG Mode

The timer 5 has a PPG (Programmable Pulse Generation) function. In PPG mode, the T5O/PWM5O pin outputs up to 16-bit resolution PWM output. This pin should be configured as a PWM output by set P0FSRH[7:6] to '11'. The period of the PWM output is determined by the T5ADRH/T5ADRL. And the duty of the PWM output is determined by the T5BDRH/T5BDRL.



NOTES:

1. The T5EN is automatically cleared to logic "0" after one pulse is generated at a PPG one-shot mode.

Figure 64. 16-bit PPG Mode for Timer 5

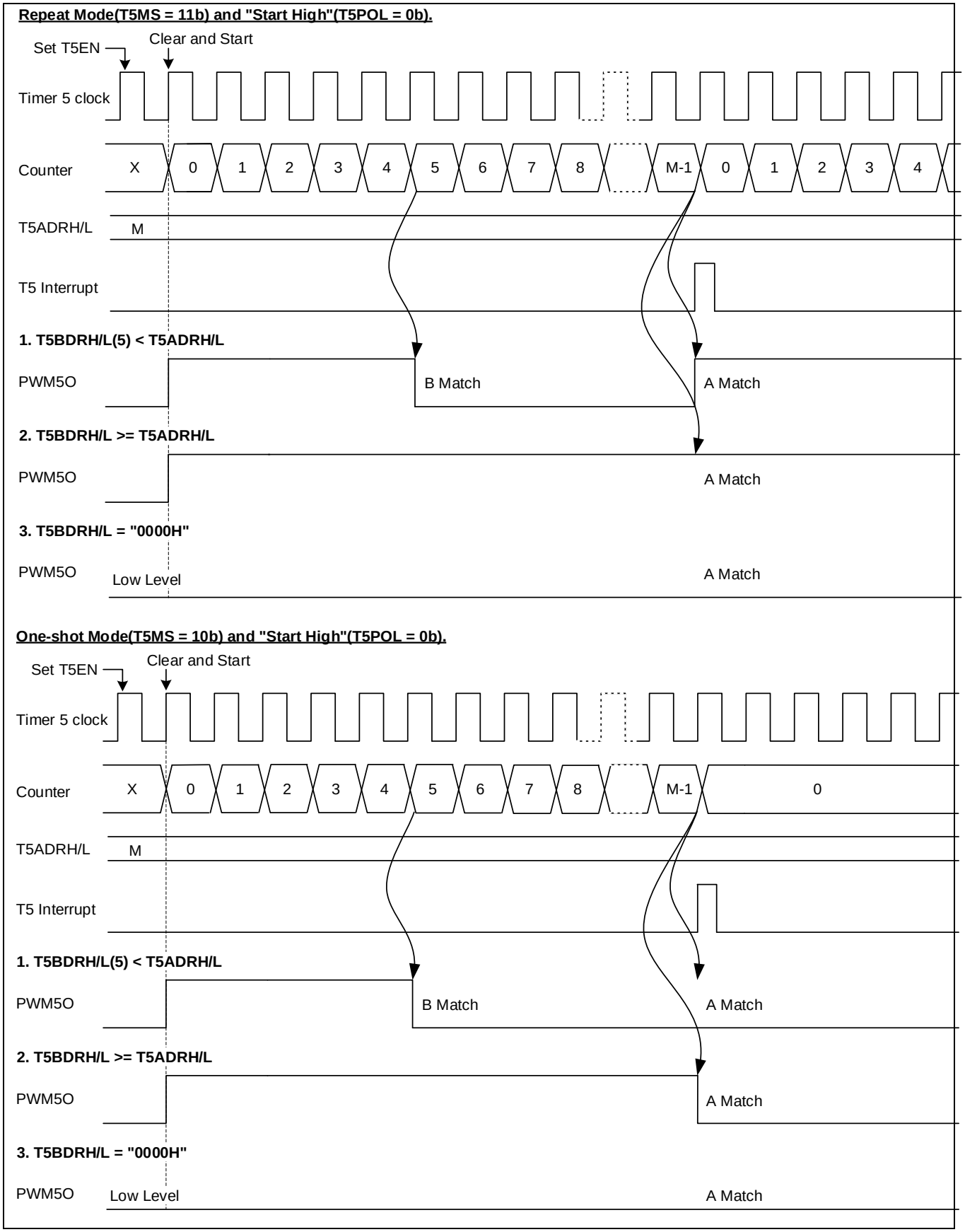


Figure 65. 16-bit PPG Mode Timming chart for Timer 5

11.6.5 Block Diagram

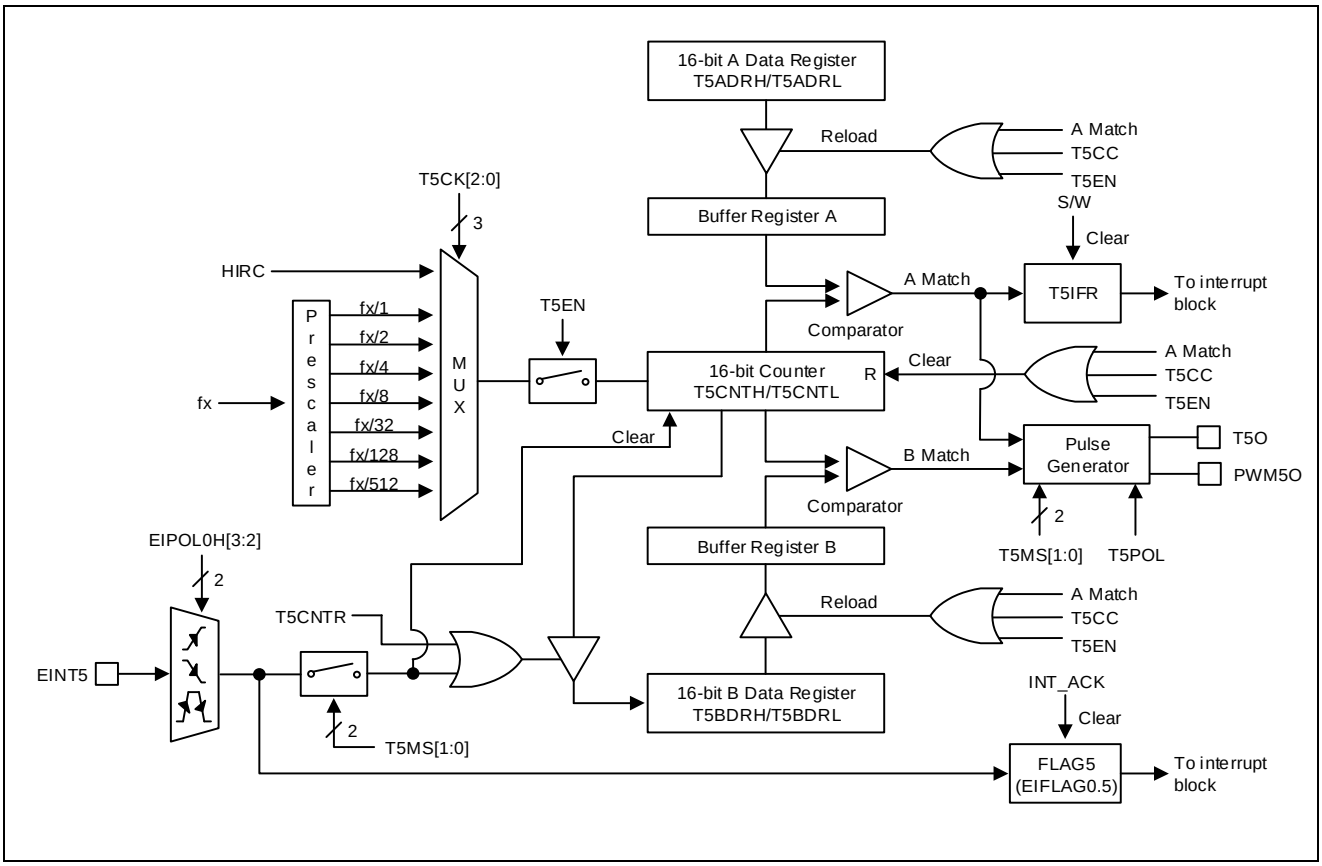


Figure 66. 16-bit Timer 5 Block Diagram

12 Buzzer Driver

12.1 Overview

The Buzzer consists of 8bit counter, buzzer data register (BUZDR), and buzzer control register (BUZCR). The Square Wave (61.035Hz~125.0kHz @8MHz) is outputted through P03/AN1/EINT1BUZ0 pin. The buzzer data register (BUZDR) controls the buzzer frequency (look at the following expression). In buzzer control register (BUZCR), BUCK[1:0] selects source clock divided by prescaler.

$$f_{BUZ}\,(Hz) = \frac{\text{Oscillator Frequency}}{2 \times \text{Prescaler Ratio} \times (\text{BUZDR} + 1)}$$

Table 16. Buzzer Frequency at 8 MHz

BUZDR[7:0]	Buzzer Frequency (kHz)			
	BUZCR[2:1]=00	BUZCR[2:1]=01	BUZCR[2:1]=10	BUZCR[2:1]=11
0000_0000	125kHz	62.5kHz	31.25kHz	15.625kHz
0000_0001	62.5kHz	31.25kHz	15.625kHz	7.812kHz
…	…	…	…	…
1111_1101	492.126Hz	246.063Hz	123.031Hz	61.515Hz
1111_1110	490.196Hz	245.098Hz	122.549Hz	61.274Hz
1111_1111	488.281Hz	244.141Hz	122.07Hz	61.035Hz

12.2 Block Diagram

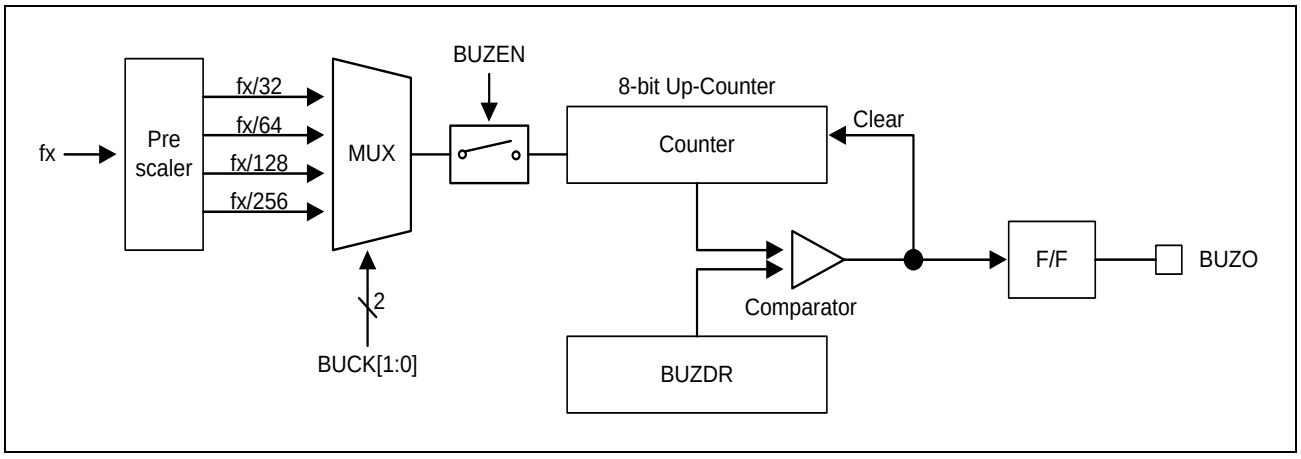


Figure 67. Buzzer Driver Block Diagram

13 USI (USART + SPI + I2C)

13.1 Overview

The USI is an acronym of USART, SPI and I2C, A96T418 has two USI function blocks. Each USI consists of USI control register1/2/3/4, USI status register 1/2, USI baud-rate generation register, USI data register, USI SDA hold time register, USI SCL high period register, USI SCL low period register, and USI slave address register (USInCR1, USInCR2, USInCR3, USInCR4, USInST1, USInST2, USInBD, USInDR, where n is 0, and USInSDHR, USInSCHR, USInSCLR, USInSAR where n is only 0).

The operation mode is selected by the operation mode of USIn selection bits (USInMS[1:0]).

It has four operating modes:

- Asynchronous mode (UART)
- Synchronous mode (USART)
- SPI mode
- I2C mode

13.2 USIn UART Mode

The universal synchronous and asynchronous serial receiver and transmitter (USART) is a highly flexible serial communication device. The main features are listed below.

- Full Duplex Operation (Independent Serial Receive and Transmit Registers)
- Asynchronous or Synchronous Operation
- Baud Rate Generator
- Supports Serial Frames with 5,6,7,8, or 9 Data bits and 1 or 2 Stop bits
- Odd or Even Parity Generation and Parity Check are Supported by Hardware
- Data OverRun Detection
- Framing Error Detection
- Three Separate Interrupts on TX Completion, TX Data Register Empty and RX Completion
- Double Speed Asynchronous communication mode

The USIn comprises clock generator, transmitter and receiver. The clock generation logic consists of synchronization logic for external clock input used by synchronizing or SPI slave operation, and the baud rate generator for asynchronous or master (synchronous or SPI) operation.

The Transmitter consists of a single write buffer, a serial shift register, parity generator and control logic for handling different serial frame formats. The write buffer allows continuous transfer of data without any delay between frames. The receiver is the most complex part of the UART module due to its clock and data recovery units. The recovery unit is used for asynchronous data reception. In addition to the recovery unit, the receiver includes a parity checker, a shift register, a two-level receive FIFO (USInDR) and control logic. The receiver supports the same frame formats as the transmitter and can detect frame error, data overrun and parity errors.

13.3 USIn SPI Mode

The USIn can be set to operate in industrial standard SPI compliant mode. The SPI mode has the following features.

- Full Duplex, Three-wire synchronous data transfer
- Mater and Slave Operation
- Supports all four SPIn modes of operation (mode 0, 1, 2, and 3)
- Selectable LSB first or MSB first data transfer
- Double buffered transmit and receive
- Programmable transmit bit rate

When SPI mode is enabled (USInMS[1:0]=”11”), the slave select (SSn) pin becomes active LOW input in slave mode operation, or can be output in master mode operation if USInSSEN bit is set to ‘0’.

Note that during SPI mode of operation, the pin RXDn is renamed as MISOn and TXDn is renamed as MOSIn for compatibility to other SPI devices.

13.4 USIn I2C Mode

The USIn can be set to operate in industrial standard serial communication protocols mode. The I2C mode uses 2 bus lines serial data line (SDAn) and serial clock line (SCLn) to exchange data. Because both SDAn and SCLn lines are open-drain output, each line needs pull-up resistor. A96T418 supports only one I2C, so n=0. The features are as shown below.

- Compatible with I2C bus standard
- Multi-master operation
- Up to 400kHz data transfer read speed
- 7 bit address
- Both master and slave operation
- Bus busy detection
- I2C Slave mode does not support repeated START bit mode.

14 USART1

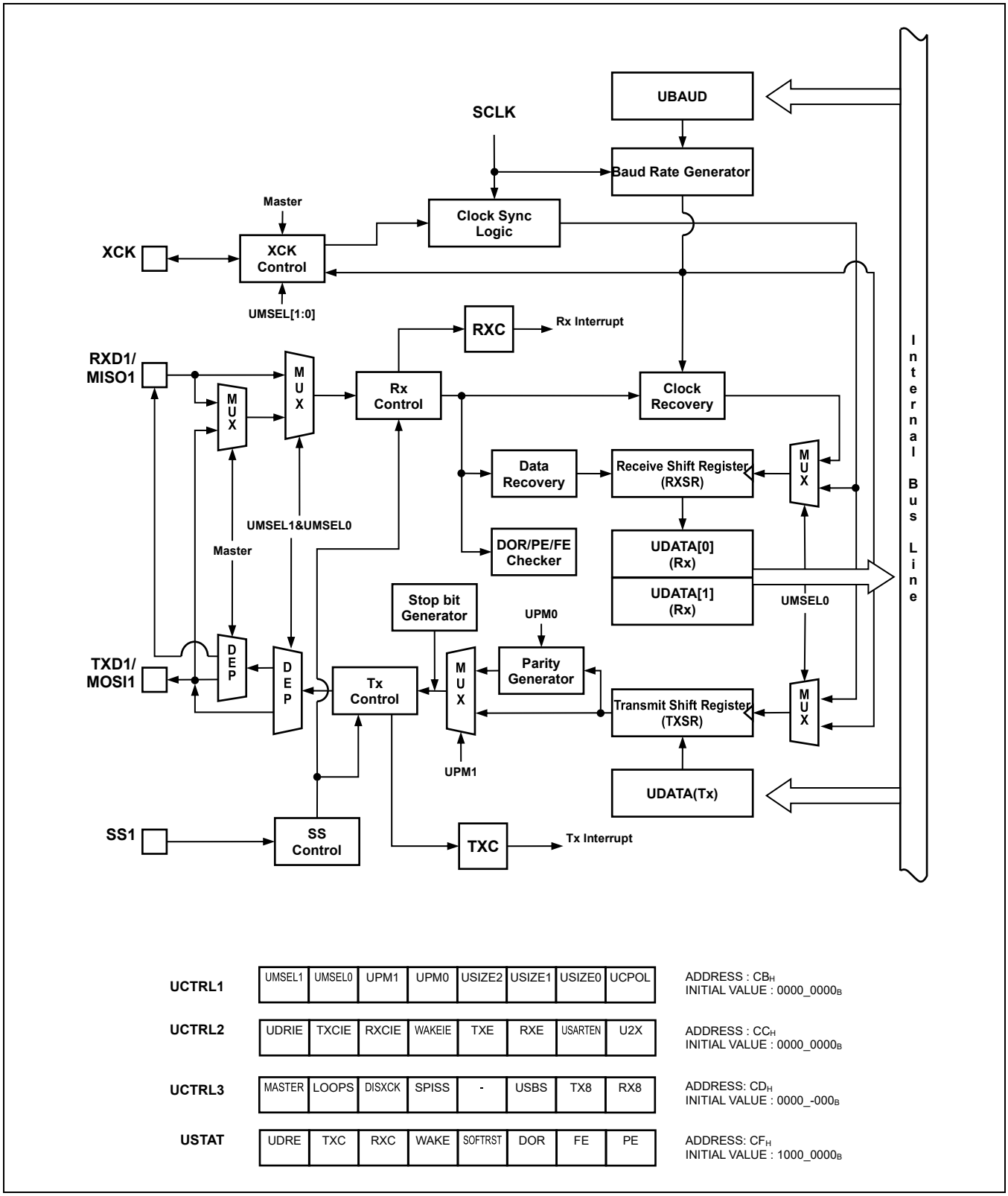
14.1 Overview

The Universal Synchronous and Asynchronous serial Receiver and Transmitter (USART1) is a highly flexible serial communication device. The main features are listed below.

- Full Duplex Operation (Independent Serial Receive and Transmit Registers)
- Asynchronous or Synchronous Operation
- Master or Slave Clocked Synchronous and SPI Operation
- Supports all four SPI Modes of Operation (Mode 0, 1, 2, 3)
- LSB First or MSB First Data Transfer @SPI mode
- High Resolution Baud Rate Generator
- Supports Serial Frames with 5,6,7,8, or 9 Data bits and 1 or 2 Stop bits
- Odd or Even Parity Generation and Parity Check Supported by Hardware
- Data OverRun Detection
- Framing Error Detection
- Digital Low Pass Filter
- Three Separate Interrupts on TX Complete, TX Data Register Empty and RX Complete
- Double Speed Asynchronous Communication Mode

USART1 has three main parts of Clock Generator, Transmitter and Receiver. The Clock Generation logic consists of synchronization logic for external clock input used by synchronous or SPI slave operation, and the baud rate generator for asynchronous or master (synchronous or SPI) operation. The Transmitter consists of a single write buffer, a serial shift register, parity generator and control logic for handling different serial frame formats. The write buffer allows a continuous transfer of data without any delay between frames. The receiver is the most complex part of the USART1 module due to its clock and data recovery units. The recovery unit is used for asynchronous data reception. In addition to the recovery unit, the Receiver includes a parity checker, a shift register, a two level receive FIFO (UDATA) and control logic. The Receiver supports the same frame formats as the Transmitter and can detect Frame Error, Data OverRun and Parity Errors.

14.2 Block Diagram



UCTRL1	UMSEL1	UMSEL0	UPM1	UPM0	USIZE2	USIZE1	USIZE0	UCPOL	ADDRESS : CB_H INITIAL VALUE : 0000_0000_B
UCTRL2	UDRIE	TXCIE	RXCIE	WAKEIE	TXE	RXE	USARTEN	U2X	ADDRESS : CC_H INITIAL VALUE : 0000_0000_B
UCTRL3	MASTER	LOOPS	DISXCK	SPISS	-	USBS	TX8	RX8	ADDRESS: CD_H INITIAL VALUE : 0000_-000_B
USTAT	UDRE	TXC	RXC	WAKE	SOFTRST	DOR	FE	PE	ADDRESS: CF_H INITIAL VALUE : 1000_0000_B

Figure 68. USART1 Block Diagram

15 LED Driver

15.1 Overview

LED drive contains 8 COM / 16 SEG output pins. They are also shared with Touch sensing pins. By setting LED CONTROL REGISTER 1 (LEDCON1), there are 5 modes that can be shared(or not shared) with touch sensing function. The controller consists of display data RAM memory, COM and SEG generator. COM0-COM7 are shared with SEG0-SEG7. It is selected by CSER register. SEG8~SEG15 is dedicated only SEG function in LED function. COM and SEG pin can also be used as I / O pins. COMOE, and SEGOE1,SEGOE2 registers are used to select SEG0-SEG14, COM0- COM7.

During the power-on reset, reset pin, BOD reset or watchdog reset, LED are turned off.

15.2 Block Diagram

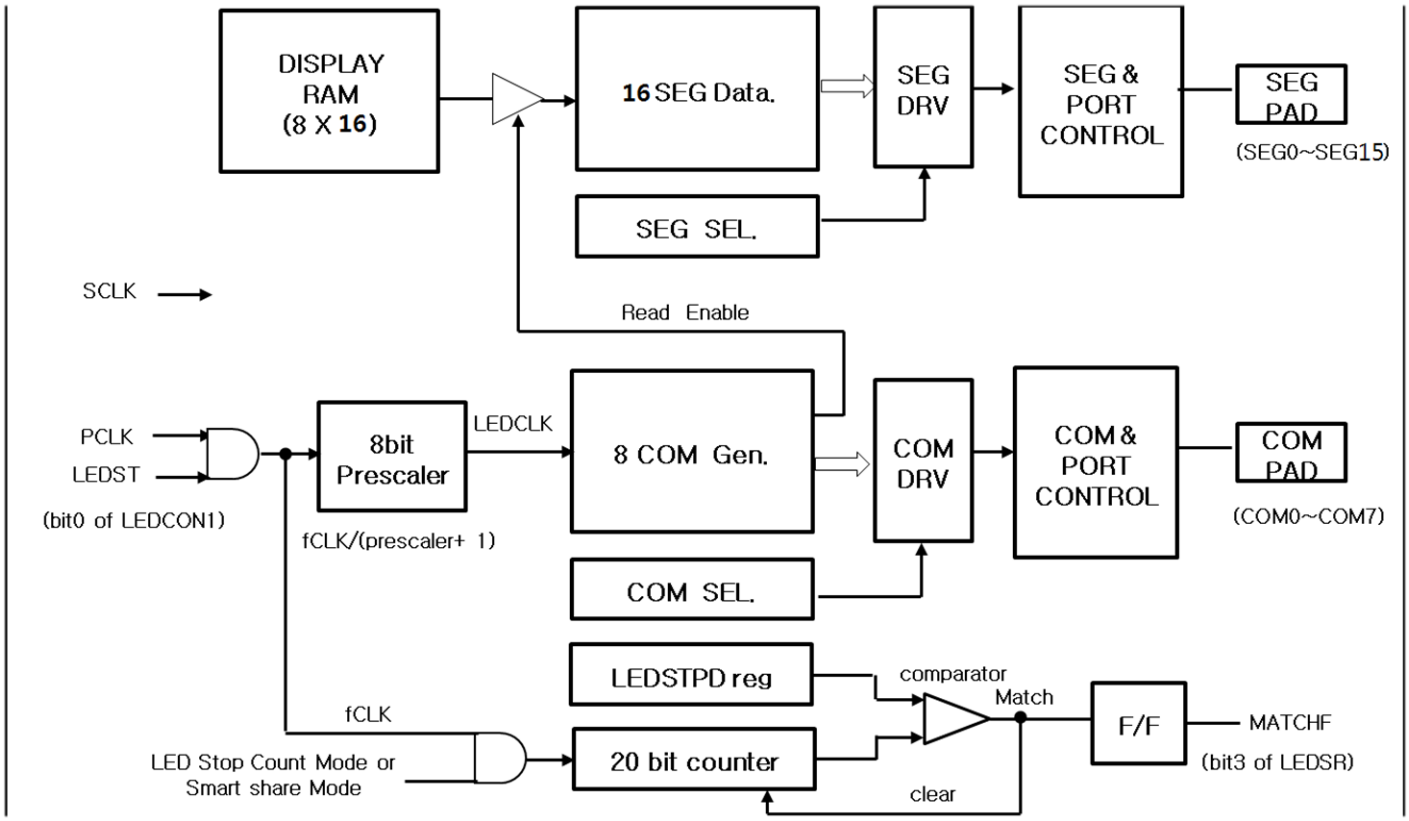


Figure 69. LED Driver Block Diagram

16 20-Channel Touch Switch

16.1 Features

- 10V Conducted Susceptibility (CS) Immunity
- Self-Capacitive Touch Key Sensor.
- Total 20-channel Touch Key Support.
- 16-bits Sensing Resolutions.
- Fast Initial Self Calibration.
- Key Detection Mode : Single/Multi-Mode.
- Clock Frequency during Sensing Operation : 16MHz.
- The Improvement of the SNR by Bias-Calibration in Analog Sensing Block.
- VDD Operating Voltage : 2.7V ~ 5.5V.
- Current Consumption : T.B.D.
- Current Consumption@STOPmode :< 1uA.
- Operation Temperature : -40℃ ~ 85℃.

16.2 Block Diagram

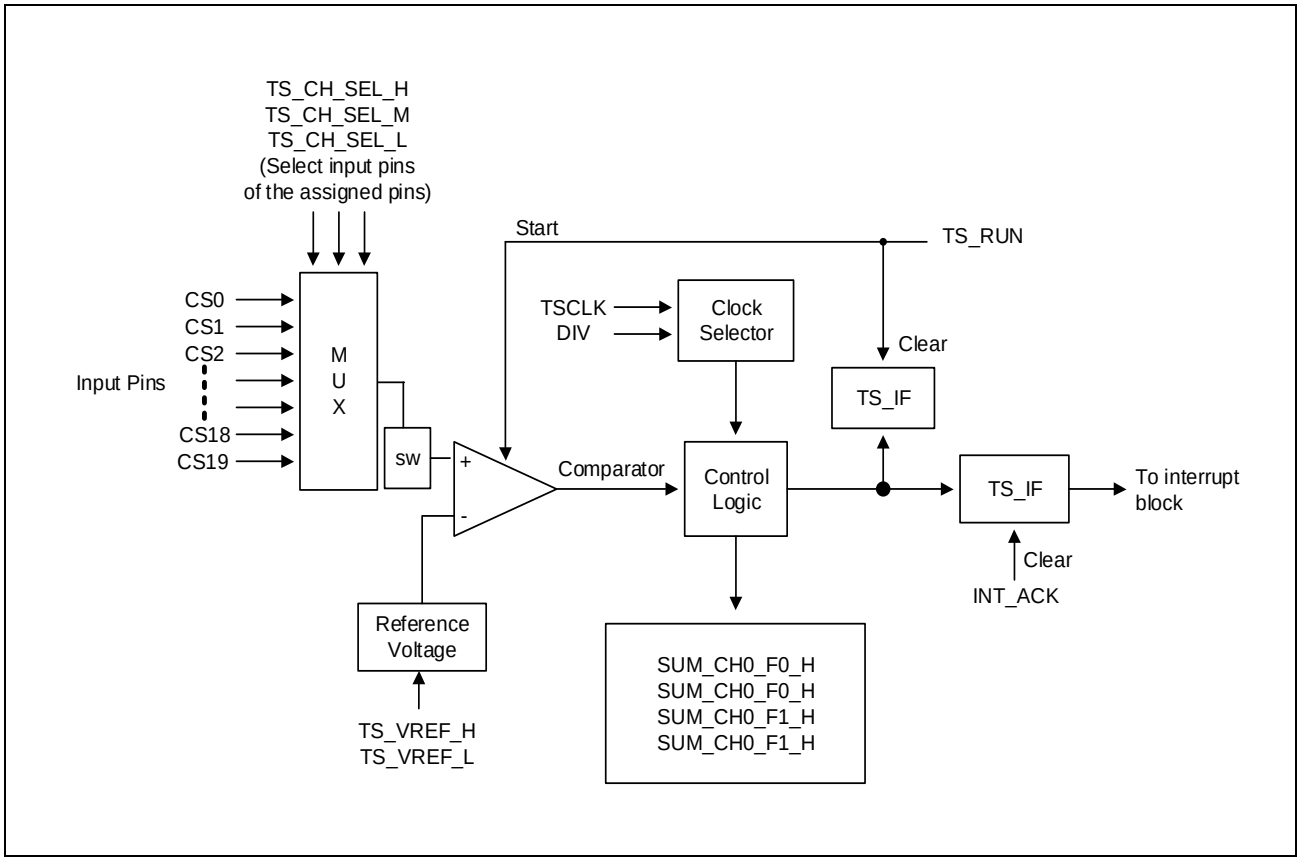


Figure 70. 16-bit Touch Block Diagram

16.3 CAPN Port

Connect the negative terminal of the reference capacitor Cs to CAPN port, and the positive terminal of the Cs capacitor to VDD. Cs capacitors must use 5% precision polyester plug-in capacitors, 10% high precision NPO or X7R chip capacitors. C0G type or Mylar Capacitors recommended for applications with severe temperature changes.

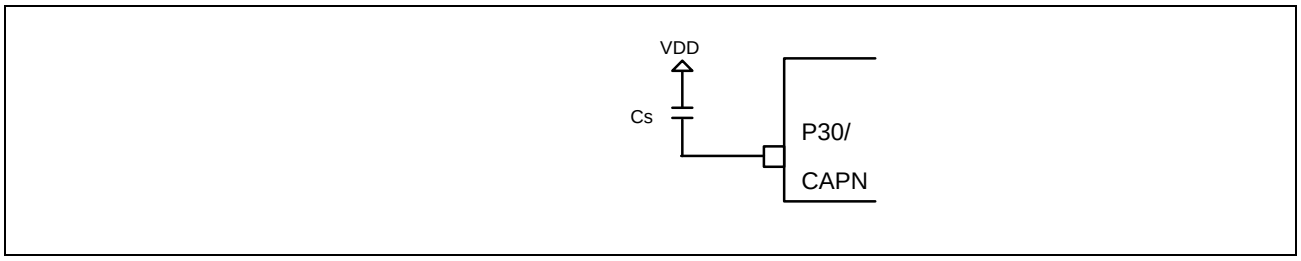


Figure 71. CAPN Pin with Cs Capacitor

17 12-bit A/D Converter

17.1 Overview

The analog-to-digital converter (A/D) allows conversion of an analog input signal to corresponding 12-bit digital value. The A/D module has eight analog inputs. The output of the multiplexeris the input into the converter which generates the result through successive approximation. The A/D module has four registers which are the A/D converter control high register (ADCCRH), A/D converter control low register (ADCCRL), A/D converter data high register (ADCDRH), and A/D converter data low register (ADCDRL). The channels to be converted are selected by setting ADSEL[2:0]. To execute A/D conversion, TRIG[2:0] bits should be set to 'xxx'. The register ADCDRH and ADCDRL contains the results of the A/D conversion. When the conversion is completed, the result is loaded into the ADCDRH and ADCDRL, the A/D conversion status bit AFLAG is set to '1', and the A/D interrupt is set. During A/D conversion, AFLAG bit is read as '0'.

17.2 Conversion Timing

The A/D conversion process requires 4 steps (4 clock edges) to convert each bit and 12 clocks to set up A/D conversion. Therefore, total of 48 clocks are required to complete a 12-bit conversion: When fxx/8 is selected for conversion clock with a 12MHz fxx clock frequency, one clock cycle is 0.66 μs. Each bit conversion requires 4 clocks, the conversion rate is calculated as follows:

4 clocks/bit × 12 bits + set-up time = 60 clocks

ADC Conversion Time = ADCLK * 60 cycles

NOTES:

1. The A/D converter needs at least 7.5us for conversion time. So you must set the conversion time more than 7.5us.

17.3 Block Diagram

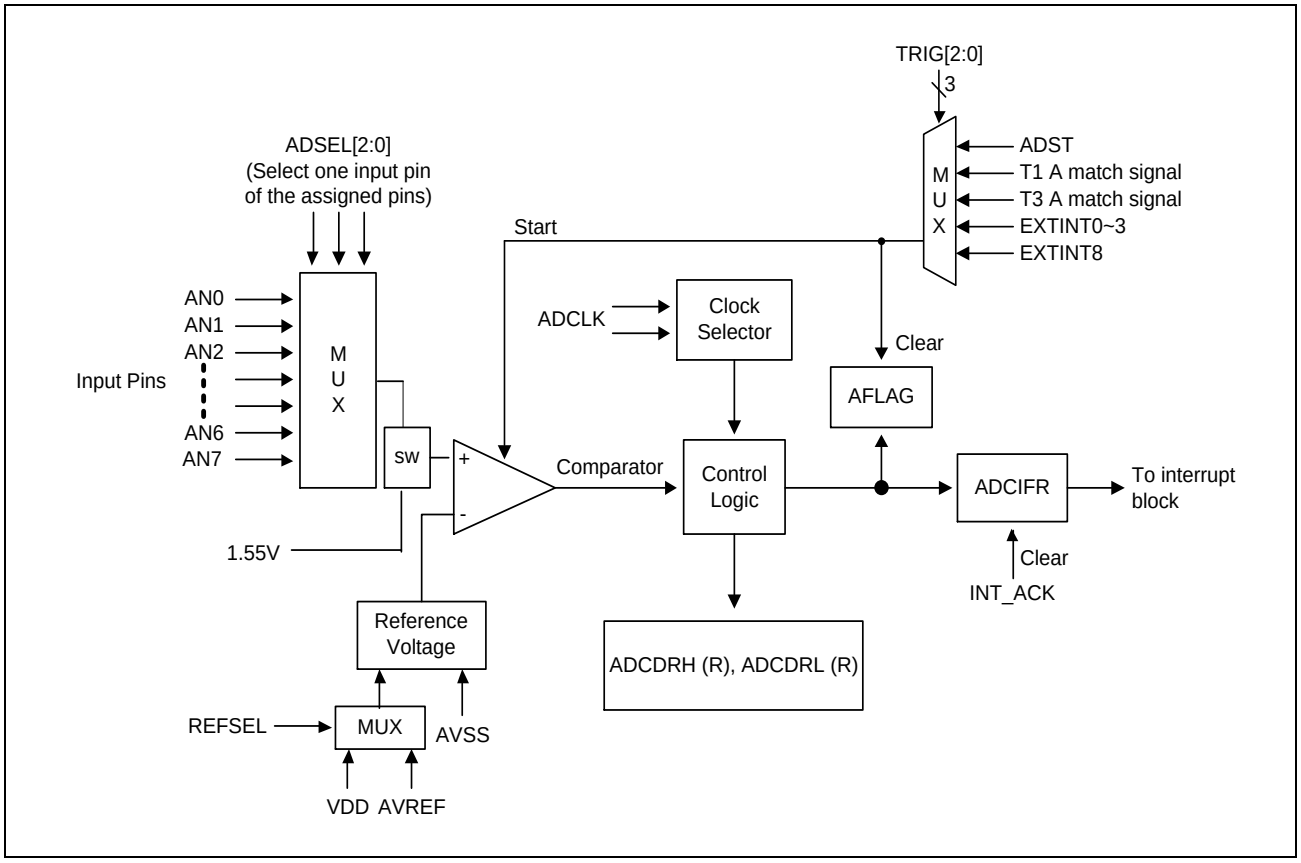


Figure 72. 12-bit ADC Block Diagram

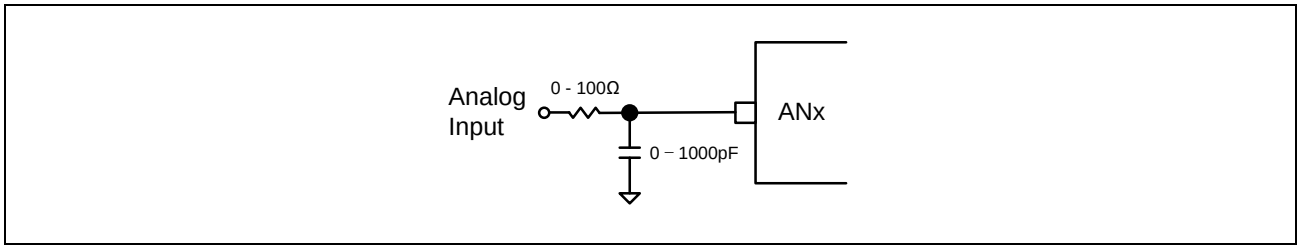


Figure 73. A/D Analog Input Pin with Capacitor

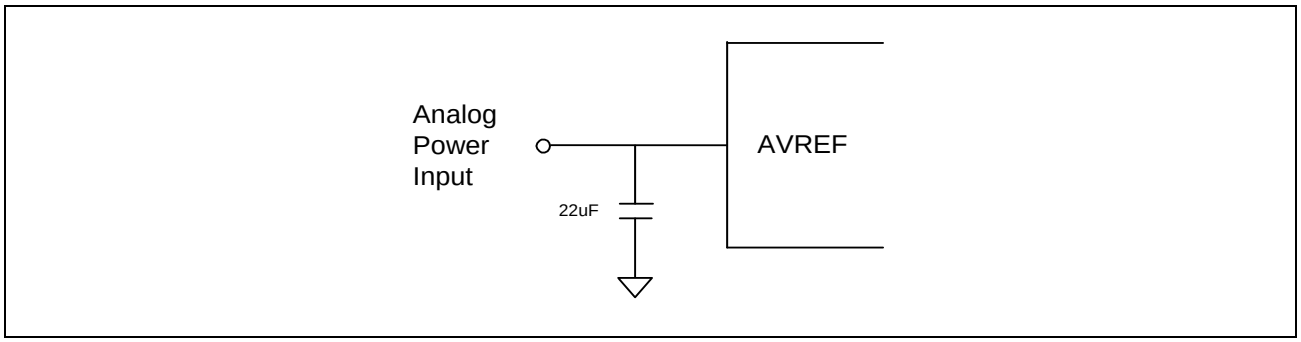


Figure 74. A/D Power (AVREF) Pin with Capacitor

18 Power Down Operation

18.1 Overview

The A96T418 has two power-down modes to minimize the power consumption of the device. In power down mode, power consumption is reduced considerably. The device provides three kinds of power saving functions, Main-IDLE, Sub-IDLE and STOP mode. In three modes, program is stopped.

18.2 Peripheral Operation in IDLE/STOP Mode

Table 17. Peripheral Operation during Power Down Mode

Peripheral	IDLE Mode	STOP Mode
CPU	ALL CPU Operation are Disable	ALL CPU Operation are Disable
RAM	Retain	Retain
Basic Interval Timer	Operates Continuously	Stop (Can be operated with WDTRC OSC)
Watch Dog Timer	Operates Continuously	Stop (Can be operated with WDTRC OSC)
Watch Timer	Operates Continuously	Stop (Can be operated with sub clock)
Timer0~4	Operates Continuously	Halted (Only when the Event Counter Mode is Enabled, Timer operates Normally)
ADC	Operates Continuously	Stop
BUZ	Operates Continuously	Stop
USI0/1	Operates Continuously	Only operate with external clock
Internal OSC (16MHz)	Oscillation	Stop when the system clock (fx) is fHSIRC
WDTRC OSC (128kHz)	Can be operated with setting value	Can be operated programmable
Sub OSC (32.768kHz)	Oscillation	Can be operated programmable
Touch OSC (16MHz)	Oscillation	Stop when the system clock (fx) is fHSIRC
I/O Port	Retain	Retain
Control Register	Retain	Retain
Address Data Bus	Retain	Retain
Release Method	By RESET, all Interrupts	By RESET, Timer Interrupt (EC0, EC1, EC3), External Interrupt, USART by RX, WT (sub clock), WDT USI0/1 by RX, I2C (Slave mode)

19 RESET

19.1 Overview

The following is the hardware setting value.

Table 18. Reset State

On Chip Hardware	Initial Value
Program Counter (PC)	0000h
Accumulator	00h
Stack Pointer (SP)	07h
Peripheral Clock	On
Control Register	Refer to the Peripheral Registers

19.2 Reset Source

The A96T418 has five types of reset sources. The following is the reset sources.

- External RESETB
- Power ON RESET (POR)
- WDT Overflow Reset (In the case of WDTEN = ’1’)
- Low Voltage Reset (In the case of LVREN = ’0’)
- OCD Reset

19.3 RESET Block Diagram

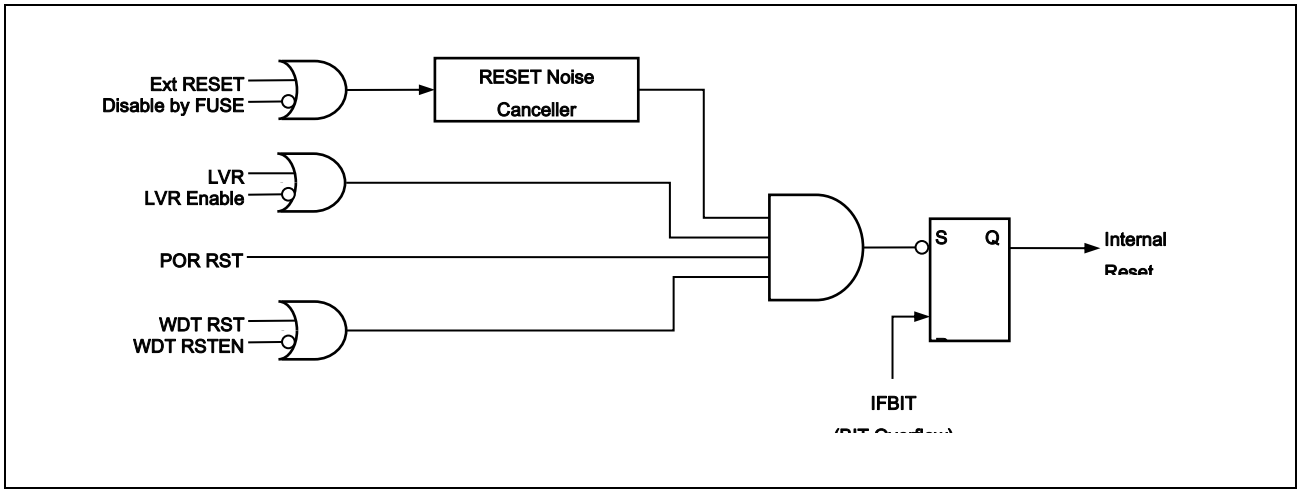


Figure 75. RESET Block Diagram

20 Memory Programming

A96T418 has flash memory to which a program can be written, erased, and overwritten while mounted on the board. Serial ISP mode is supported.

Flash of A96T418 features the followings:

- Flash Size : 32Kbytes
- Single power supply program and erase
- Command interface for fast program and erase operation
- Up to 10,000 program/erase cycles at typical voltage and temperature for flash memory
- Security feature

20.1 Flash Control and Status Register

Registers to control Flash and Data EEPROM are Mode Register (FEMR), Control Register (FECR), Status Register (FESR), Time Control Register (FETCR), Address Low Register x (FEARLx), Address Middle Register x (FEARMx), address High Register (FEARH). They are mapped to SFR area and can be accessed only in programming mode.

20.2 Memory Map

20.2.1 Flash Memory Map

Program memory uses 32KBytes of Flash memory. It is read by byte and written by byte or page. One page is 64-bytes.

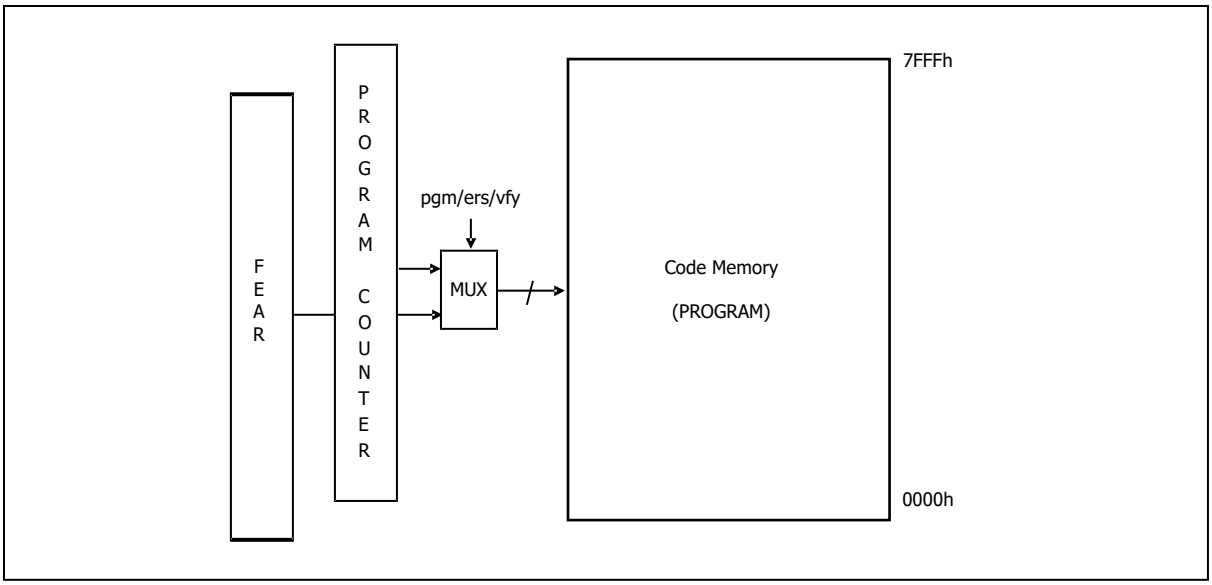


Figure 76. Flash Memory Map

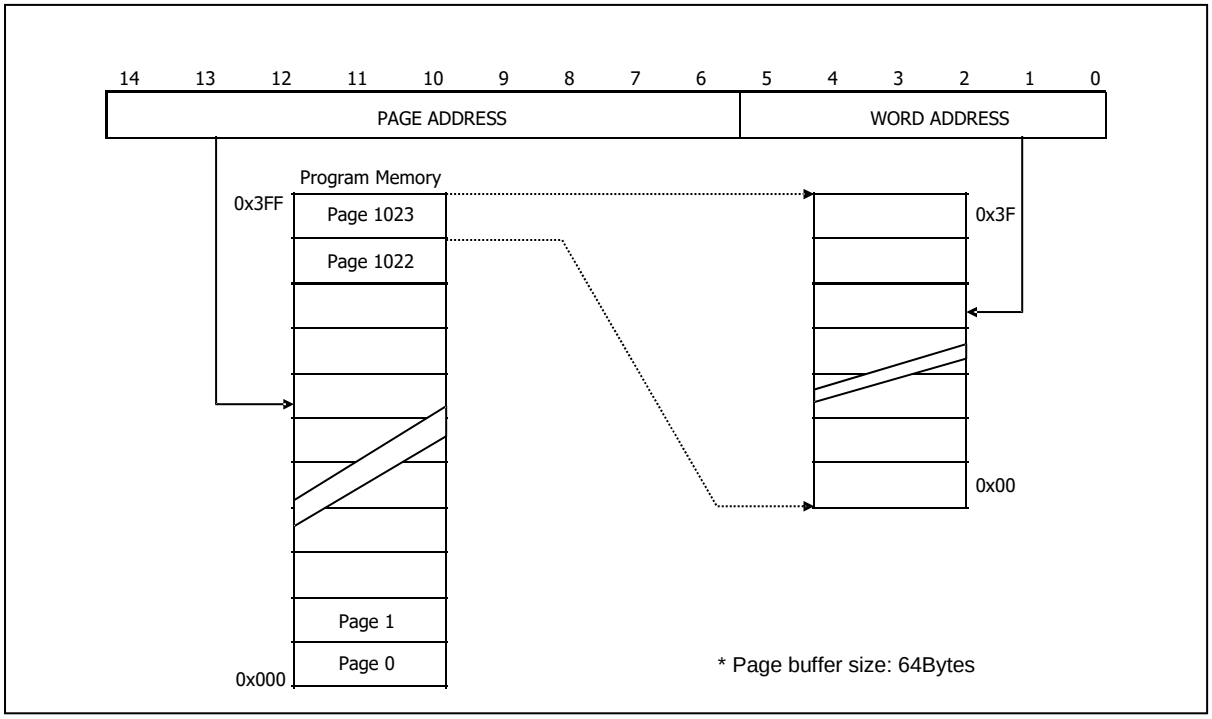


Figure 77. Address Configuration of Flash Memory

21 Electrical Characteristics

21.1 Absolute Maximum Ratings

Table 19. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Note
Supply Voltage	VDD	-0.3~+6.5	V	–
Normal Voltage Pin	V_I	-0.3~VDD+0.3	V	Voltage on any pin with respect to VSS
	V_O	-0.3~VDD+0.3	V	
	I_{OH}	42.5	mA	Maximum current output sourced by (I_{OH} per I/O pin)
	$\sum I_{OH}$	112	mA	Maximum current ($\sum I_{OH}$)
	I_{OL1}	50	mA	Maximum current (I_{OL1} per I/O pin)
	$\sum I_{OL1}$	101	mA	Maximum current ($\sum I_{OL1}$)
	I_{OL2}	160	mA	Maximum current sunk by (I_{OL2} per I/O pin)
	$\sum I_{OL2}$	160	mA	Maximum current by LED Drive ($\sum I_{OL2}$)
Total Power Dissipation	P_T	600	mW	–
Storage Temperature	T_{STG}	-65~+150	°C	–

NOTES:

1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

21.2 Recommended Operating Conditions

Table 20. Recommended Operating Conditions

(T_A=-40°C ~ 85°C)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Operating Voltage	VDD	f_X= 16MHz HSIRC	2.0	–	5.5	V
		f_X= 128kHz LSIRC	2.0	–	5.5	
		f_X= 32 ~ 38kHz Ext. Sub Crystal	2.0	–	5.5	
		Touch, ADC, LED Driver	2.7	–	5.5	
Operating Temperature	T_{OPR}	VDD=2.0~5.5V	-40	–	85	°C

21.3 Touch Sensing Characteristics

Table 21. Touch Switch Characteristics

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Load Capacitance	Cload	-	-	50	100	pF
Operating Frequency	Fop	Cload=50pF(@typ.) Cload=100pF(@min.)	2	4	4	MHz
High-Sense Voltage	VHS	VDD=5V	2.6	3.5	5	V
COMP Reference Voltage	VCOM	VDD=5V	2.5	3	3.5	V

21.4 A/D Converter Characteristics

Table 22. A/D Converter Characteristics

(T_A=-40°C ~ +85°C, VDD=2.7V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Resolution	–	–		–-	12	–	bit
Integral Linear Error	ILE	AVREF= 2.7V – 5.5V fx= 8MHz		–	–	±6	LSB
Differential Linearity Error	DLE			–	–	±1	
Zero Offset Error	ZOE			–	–	±5	
Full Scale Error	FSE			–	–	±5	
Conversion Time	t_{CON}	12-bit resolution, 8MHz		8	–	–	us
Analog Input Voltage	V_{AN}	–		VSS	–	AVREF	V
Analog Reference Voltage	AVREF	*Note 3		2.7	–	VDD	
Analog Input Leakage Current	I_{AN}	AVREF=5.12V		–	–	2	uA
ADC Operating Current	I_{ADC}	Enable	VDD=5.12V	–	1	2	mA
		Disable		–	–	0.1	uA

NOTES:

1. Zero offset error is the difference between 000000000000 and the converted output for zero input voltage (VSS).
2. Full scale error is the difference between 111111111111 and the converted output for full-scale input voltage (AVREF).
3. When AVREF is lower than 2.7V, the ADC resolution is worse.

21.5 Power-On Reset Characteristics

Table 23. Power-on Reset Characteristics

(T_A=-40°C ~ +85°C, VDD=2.0V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
RESET Release Level	V_{POR}	–	–	1.2	–	V
VDD Voltage Rising Time	t_R	–	0.05	–	50.0	V/ms
Minimum Pulse Width	t_{LW}	–	100			us
POR Current	I_{POR}	–	–	0.2	–	uA

21.6 Low Voltage Reset and Low Voltage Indicator Characteristics

Table 24. LVR and LVI Characteristics

(T_A=-40°C ~ +85°C, VDD=2.0V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Detection Level	V_{LVR} V_{LVI}	The LVR can select all levels but LVI can select other levels except 1.61/1.77/1.88/2.00/2.13V. (Falling level)		-	1.61	1.75	V
				1.63	1.77	1.91	
				1.73	1.88	2.03	
				1.84	2.00	2.16	
				1.96	2.13	2.30	
				2.10	2.28	2.46	
				2.26	2.46	2.66	
				2.47	2.68	2.89	
				2.59	2.81	3.03	
				2.82	3.06	3.30	
				2.95	3.21	3.47	
				3.28	3.56	3.84	
				3.43	3.73	4.03	
				3.60	3.91	4.22	
				3.91	4.25	4.59	
Hysteresis	$\triangle V$	–		–	30	180	mV
Minimum Pulse Width	t_{LW}	–		100	–	–	us
LVR and LVI Current	I_{BL}	Enable (Both)	VDD= 3V, RUN Mode	–	14.0	24.0	uA
		Enable (One of two)		–	10.0	18.0	
		Disable (Both)	VDD= 3V	–	–	0.1	

NOTES:

1. Guaranteed by design

21.7 High Speed Internal RC Oscillator Characteristics

Table 25. High Internal RC Oscillator Characteristics

(T_A=-40°C ~ +85°C, VDD=2.0V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Frequency	f_{HSIRC}	V_{DD} = 2.0 – 5.5V		–	16	–	MHz
Tolerance	–	T_A = -10°C to +70°C	With 0.1uF Bypass capacitor	–	–	±1.5	%
		T_A = -10°C to +70°C		–	–	±2.0	
		T_A = -40°C to +85°C		–	–	±2.5	
Clock Duty Ratio	TOD	–		40	50	60	%
Stabilization Time	T_{HFS}	–		–	–	100	us
HSIRC Current	I_{HSIRC}	Enable		–	0.2	–	mA
		Disable		–	–	-0.1	uA

NOTES:

1. A 0.1uF bypass capacitor should be connected to VDD and VSS.

21.8 Low Speed Internal RC Oscillator Characteristics

Table 26. Internal WDTRC Oscillator Characteristics

(T_A=-40°C ~ +85°C, VDD=2.0V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Frequency	f_{LSIRC}	T_A=-40°C ~ +85°C	102	128	154	kHz
Stabilization Time	T_{LSIRC}	–	–	–	1	ms
LSIRC Current	I_{LSIRC}	Enable	–	1	–	uA
		Disable	–	–	0.1	

21.9 DC Characteristics

Table 27. DC Characteristics

(T_A= -40°C ~ +85°C, VDD= 2.0V ~ 5.5V, VSS= 0V, f_{SCLK}= 16MHz)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Input High Voltage	V_{IH}	All input pins	0.7VDD	–	VDD	V
Input Low Voltage	V_{IL}	All input pins except V_{IL1}	–	–	0.3VDD	V
Output High Voltage	V_{OH1}	VDD=4.5V, I_{OH}=-8.57mA, All output ports;	VDD-1.0	–	–	V
	V_{OH2}	VDD=4.5V, I_{OH}= -19 mA, All output ports;	VDD-2.0	–	–	V
SEG Output High Voltage	V_{OH30}	VDD=5.0V, I_{OH}= -8.66 mA, T_A= 25°C	-	VDD-0.5	–	V
	V_{OH31}	VDD=5.0V, I_{OH}= -13.22 mA, T_A= 25°C	-	VDD-0.5	–	V
	V_{OH32}	VDD=5.0V, I_{OH}= -19.49 mA, T_A= 25°C	-	VDD-0.5	–	V
	V_{OH33}	VDD=5.0V, I_{OH}= -22.06 mA, T_A= 25°C	-	VDD-0.5	–	V
SEG Current Matching	ITOSEG	VDD=5.0V, VOH=4.5V TA= 25°C, Voh31	-5		5	%
Output Low Voltage	V_{OL1}	VDD=4.5V, I_{OL}= 10mA; All output ports except V_{OL2}	–	–	1.0	V
	V_{OL2}	VDD=5V, I_{OL}= 250mA, T_A= 25°C; P2x LED High sink current output	–	1.5	-	V
Input High Leakage Current	I_{IH}	All input ports	–	–	1	uA
Input Low Leakage Current	I_{IL}	All input ports	-1	–	–	uA
Pull-Up Resistor	R_{PU}	VDD=5.0V, VI=0V, T_A= 25°C, All Input ports	25	50	100	kΩ
OSC feedback resistor	R_X	SXIN=VDD, SXOUT=VSS T_A= 25°C, VDD=5V	6.25	13.53	36.98	MΩ
Power Supply Current	I_{DD1} (RUN)	f_{HSIRC}= 16MHz, VDD= 5V±10%	0.7	-	4.0	mA
	I_{DD2} (IDLE)	f_{HSIRC}= 16MHz, VDD= 5V±10%	0.5	-	3.0	mA
	$I_{DD3(STOP1)}$	STOP @ WDT on, VDD= 5.5V±10%, T_A= 25°C	–	-	22.0	uA
	$I_{DD4(STOP2)}$	STOP @ WDT off & LVR off, VDD= 5.5V±10%,T_A= 25°C	–	-	7.0	

NOTES:

1. Where f_{SUB} is an external sub oscillator, the f_{HSIRC} and f_{LSIRC} are an internal RC oscillator, and the f_{SCLK} is the selected system clock.
2. All supply current items don't include the current of an internal Watch-dog timer RC (WDTRC) oscillator and a peripheral block.
3. All supply current items include the current of the power-on reset (POR) block.
4. SEG Current Matching represents (ISEG-ISEGAVR) / ISEGAVR)

21.10 AC Characteristics

Table 28. AC Characteristics

(T_A= -40°C ~ +85°C, VDD= 2.0V ~ 5.5V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
RESETB input low width	t_{RSL}	Input, VDD= 5V	10	–	–	us
Interrupt input high, low width	t_{INTH}, t_{INTL}	All interrupt, VDD= 5V	200	–	–	ns
External Counter Input High, Low Pulse Width	tECWH, tECWL	ECn, VDD = 5V (n= 0, 1, 3)	200	–	–	
External Counter Transition Time	tREC, tFEC	ECn, VDD = 5V (n= 0, 1, 3)	20	–	–	

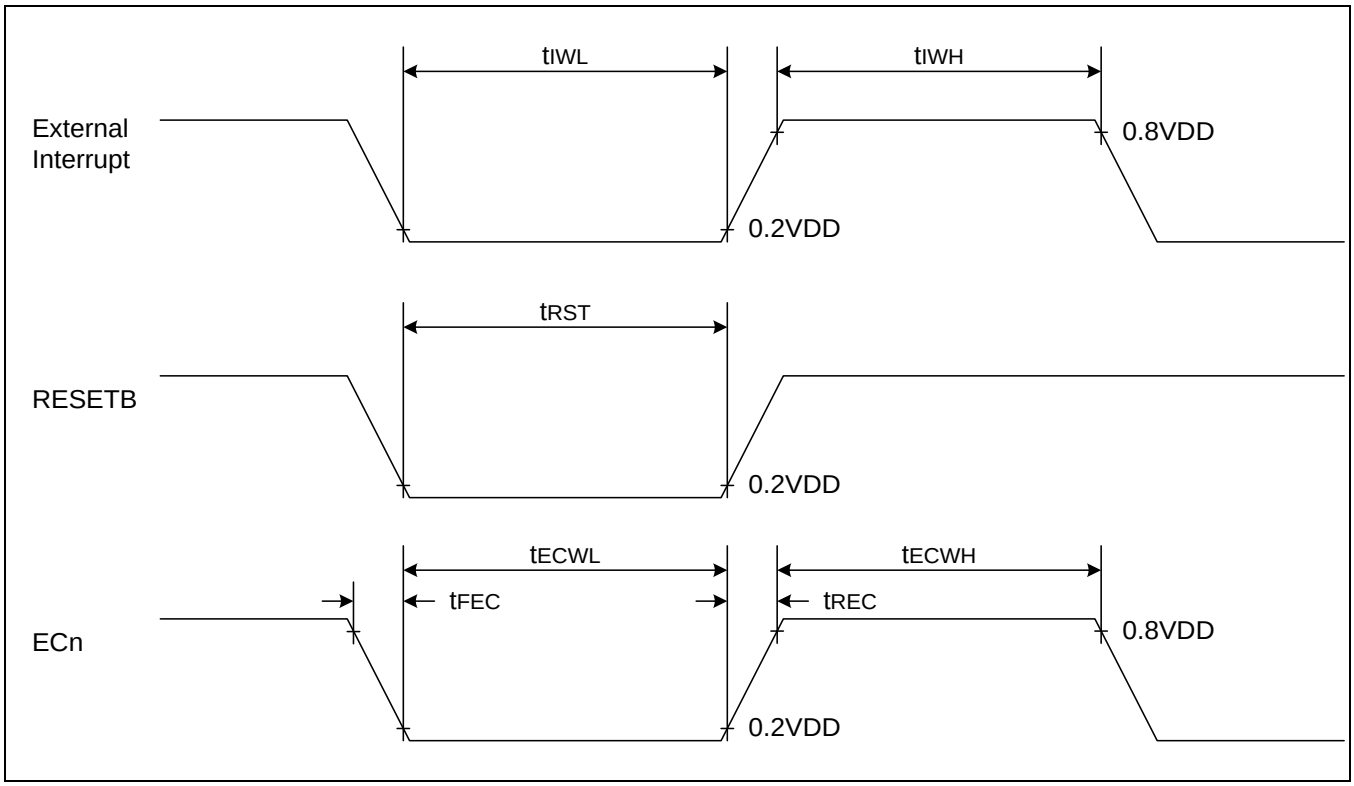


Figure 78. AC Timing

21.11 USART Characteristics

Table 29. USART Characteristics

(T_A= -40°C ~ +85°C, VDD=2.0V ~ 5.5V, f_{SCLK}=8MHz)

Parameter	Symbol	MIN	TYP	MAX	Unit
Serial port clock cycle time	t_{SCK}	1800	t_{CPU} x 16	2200	ns
Output data setup to clock rising edge	t_{S1}	8100	t_{CPU} x 13	–	ns
Clock rising edge to input data valid	t_{S2}	–	–	590	ns
Output data hold after clock rising edge	t_{H1}	t_{CPU}- 50	t_{CPU}	–	ns
Input data hold after clock rising edge	t_{H2}	0	–	–	ns
Serial port clock High, Low level width	t_{HIGH}, t_{LOW}	720	t_{CPU} x 8	1280	ns

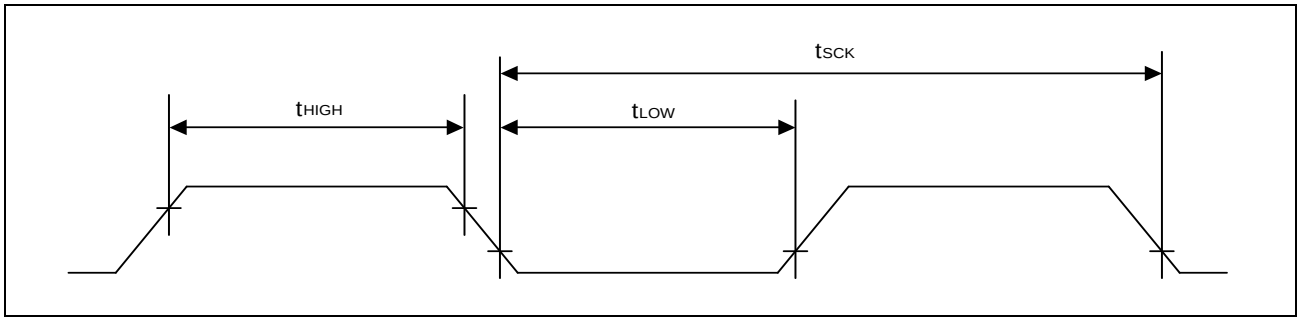


Figure 79. Waveform for USART Timing Characteristics

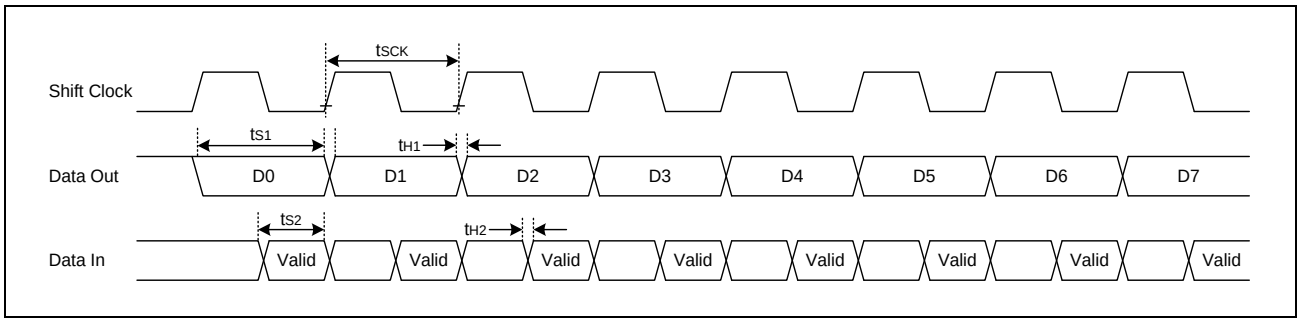


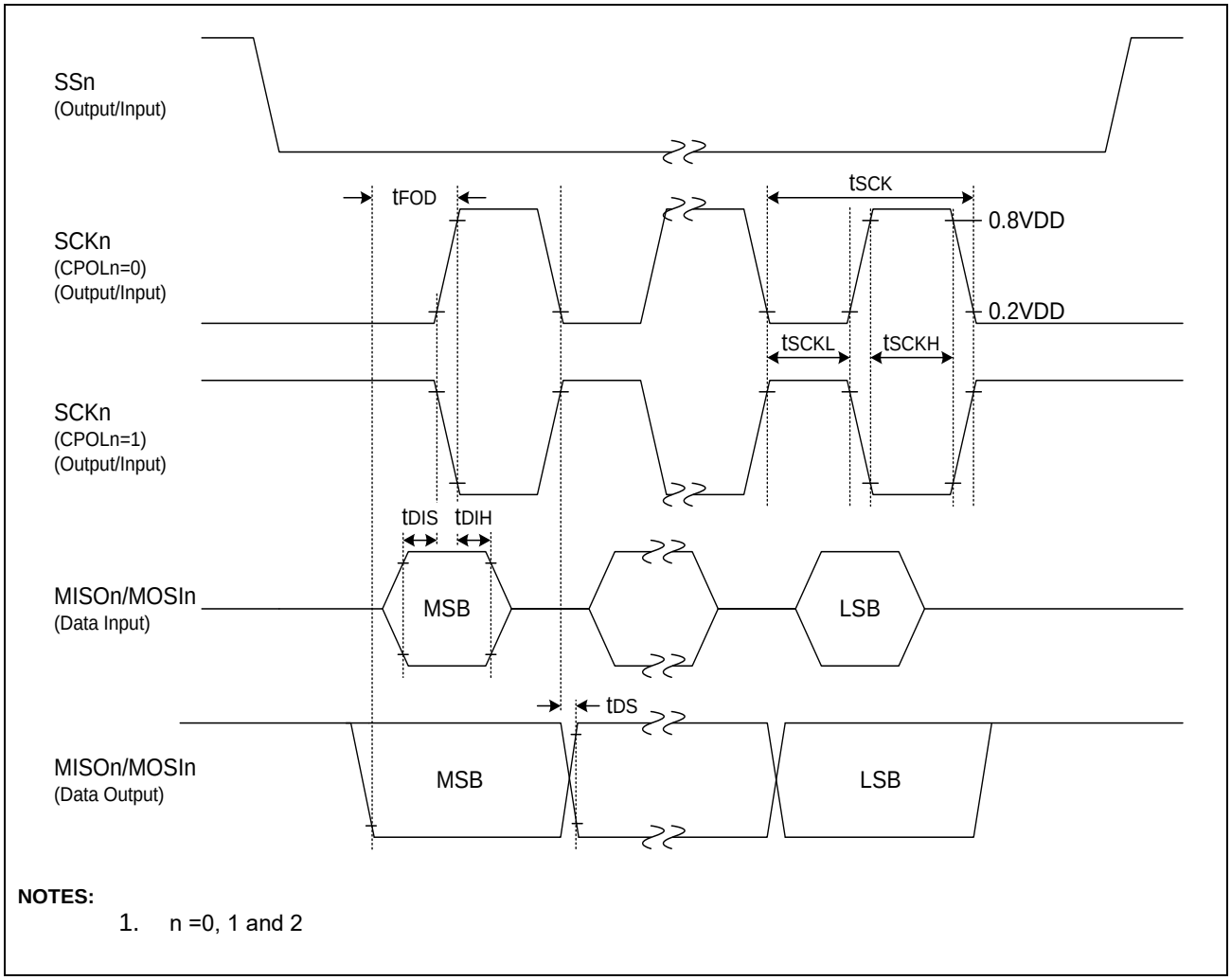
Figure 80. Timing Waveform for the USART Module

21.12 SPI0 Characteristics

Table 30. SPI0 Characteristics

(T_A=-40°C– +85°C, VDD=2.0V – 5.5V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Output Clock Pulse Period	tSCK	Internal SCK source	200	–	–	ns
Input Clock Pulse Period		External SCK source	200	–	–	
Output Clock High, Low Pulse Width	tSCKH, tSCKL	Internal SCK source	70	–	–	
Input Clock High, Low Pulse Width		External SCK source	70	–	–	
First Output Clock Delay Time	tFOD	Internal/External SCK source	100	–	–	
Output Clock Delay Time	tDS	–	–	–	50	
Input Setup Time	tDIS	–	100	–	–	
Input Hold Time	tDIH	–	150	–	–	



NOTES:

1. n =0, 1 and 2

Figure 81. SPI0/1/2 Timing

21.13 UART0 Characteristics

Table 31. UART0 Characteristics

(T_A=-40°C ~ +85°C, VDD=2.0V ~ 5.5V, f_{SCLK}=8MHz)

Parameter	Symbol	MIN	TYP	MAX	Unit
Serial port clock cycle time	t_{SCK}	1800	t_{CPU} x 16	2200	ns
Output data setup to clock rising edge	t_{S1}	810	t_{CPU} x 13	–	ns
Clock rising edge to input data valid	t_{S2}	–	–	590	ns
Output data hold after clock rising edge	t_{H1}	t_{CPU}- 50	t_{CPU}	–	ns
Input data hold after clock rising edge	t_{H2}	0	–	–	ns
Serial port clock High, Low level width	t_{HIGH}, t_{LOW}	720	t_{CPU} x 8	1280	ns

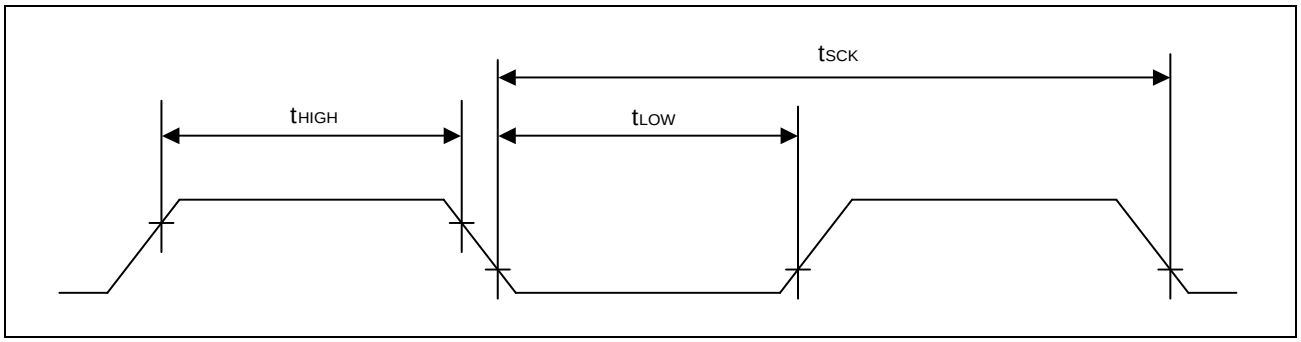


Figure 82. Waveform for UART0 Timing Characteristics

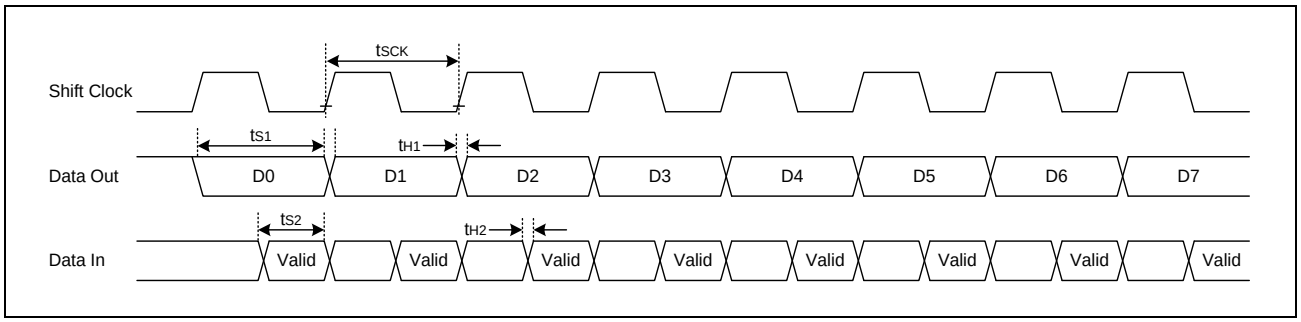


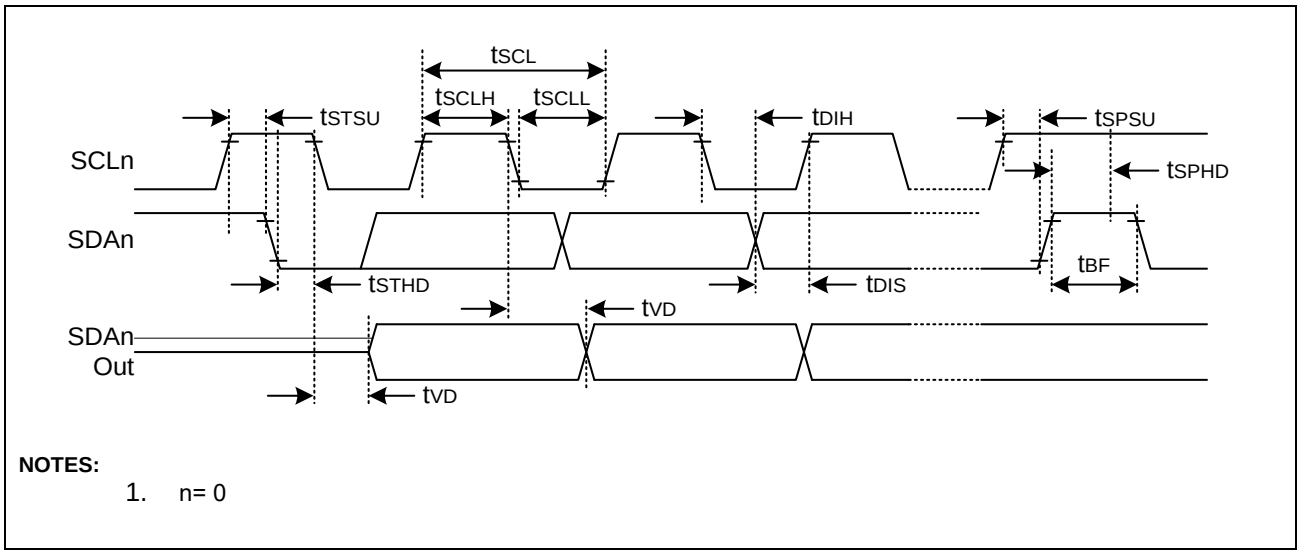
Figure 83. Timing Waveform for the UART0 Module

21.14 I2C0 Characteristics

Table 32. I2C0 Characteristics

(T_A=-40°C ~ +85°C, VDD=2.0V ~ 5.5V)

Parameter	Symbol	Standard Mode		High-Speed Mode		Unit
		MIN	MAX	MIN	MAX	
Clock frequency	tSCL	0	100	0	400	kHz
Clock High Pulse Width	tSCLH	4.0	–	0.6	–	us
Clock Low Pulse Width	tSCLL	4.7	–	1.3	–	
Bus Free Time	tBF	4.7	–	1.3	–	
Start Condition Setup Time	tSTSU	4.7	–	0.6	–	
Start Condition Hold Time	tSTHD	4.0	–	0.6	–	
Stop Condition Setup Time	tSPSU	4.0	–	0.6	–	
Stop Condition Hold Time	tSPHD	4.0	–	0.6	–	
Output Valid from Clock	tVD	0	–	0	–	
Data Input Hold Time	tDIH	0	–	0	1.0	
Data Input Setup Time	tDIS	250	–	100	–	ns



NOTES:

1. n= 0

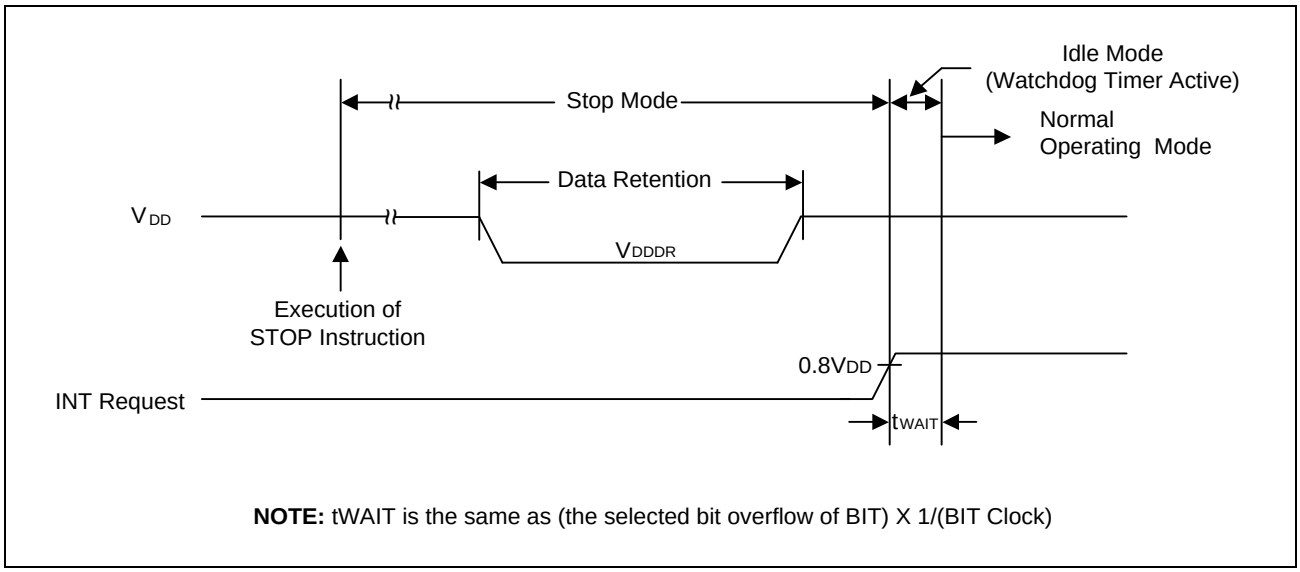
Figure 84. I2C0 Timing

21.15 Data Retention Voltage in Stop Mode

Table 33. Data Retention Voltage in Stop Mode

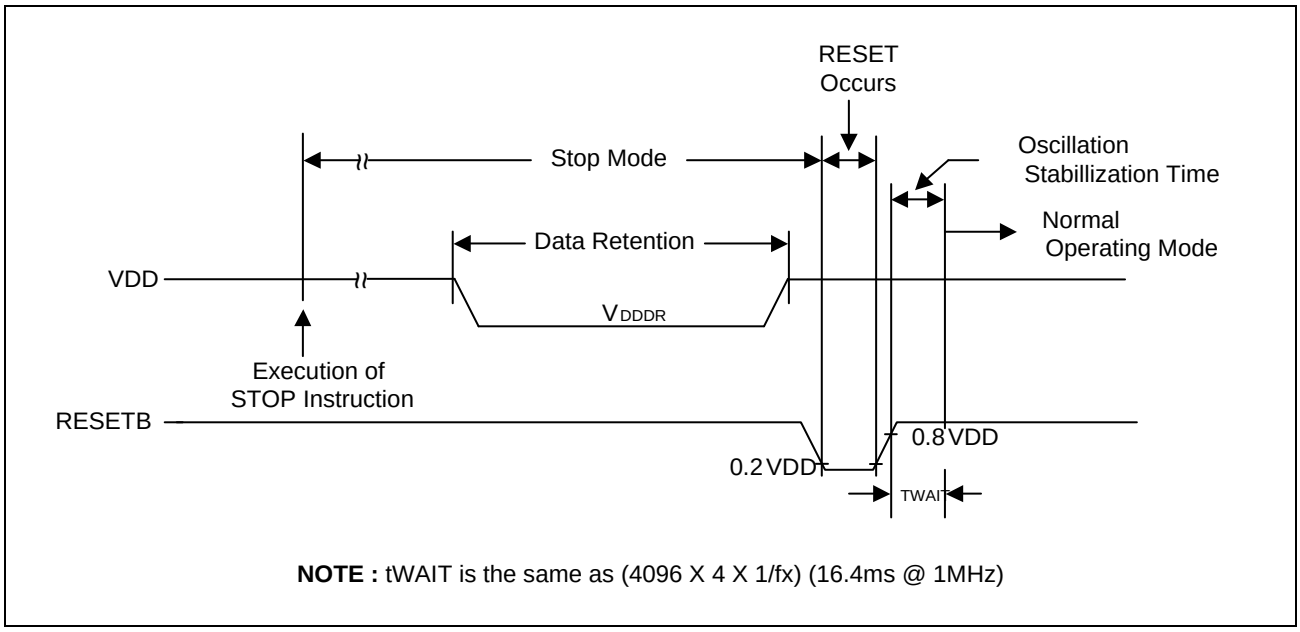
(T_A=-40°C ~ +85°C, VDD=2.0V ~ 5.5V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Data retention supply voltage	V_{DDDR}	–	2.0	–	5.5	V
Data retention supply current	I_{DDDR}	VDDR= 2.0V, (T_A= 25°C), Stop mode	–	–	1	uA



NOTE: tWAIT is the same as (the selected bit overflow of BIT) X 1/(BIT Clock)

Figure 85. Stop Mode Release Timing when Initiated by an Interrupt



NOTE : tWAIT is the same as (4096 X 4 X 1/fx) (16.4ms @ 1MHz)

Figure 86. Stop Mode Release Timing when Initiated by RESETB

21.16 Internal Flash Rom Characteristics

Table 34. Internal Flash Rom Characteristics

(T_A=-40°C ~ +85°C, VDD=2.0V ~ 5.5V, VSS= 0V)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Sector Write Time	t_{FSW}	–	–	2.5	2.7	ms
Sector Erase Time	t_{FSE}	–	–	2.5	2.7	
Code Write Protection Time	t_{FHL}	–	–	2.5	2.7	
Page Buffer Reset Time	t_{FBR}	–	–	–	5	us
Flash Programming Frequency	f_{PGM}	–	0.4	–	–	MHz
Endurance of Write/Erase	NF_{WE}	–	–	–	10,000	times

NOTES:

1. During a flash operation, SCLK[1:0] of SCCR must be set to “00” or “01” (INT-RC OSC for system clock).

21.17 Input/Output Capacitance

Table 35. Input / Output Capacitance

(T_A=-40°C ~ +85°C, VDD=0V)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Input Capacitance	C_{IN}	fx= 1MHz Unmeasured pins are connected to VSS	–	–	10	pF
Output Capacitance	C_{OUT}					
I/O Capacitance	C_{IO}					

21.18 Sub Clock Oscillator Characteristics

Table 36. Sub Clock Oscillator Characteristics

(T_A=-40°C ~ +85°C, VDD=2.0V ~ 5.5V)

Oscillator	Parameter	Condition	MIN	TYP	MAX	Unit
Crystal	Sub oscillation frequency	2.0V – 5.5V	32	32.768	38	kHz
External Clock	SXIN input frequency		32	–	100	kHz

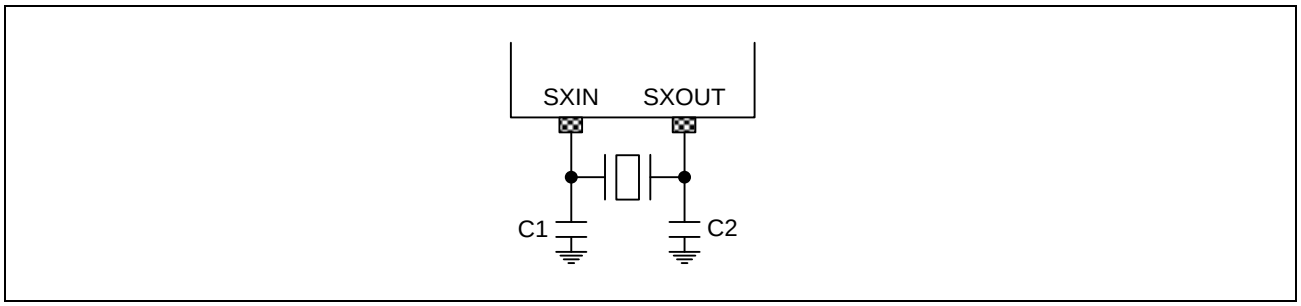


Figure 87. Crystal Oscillator

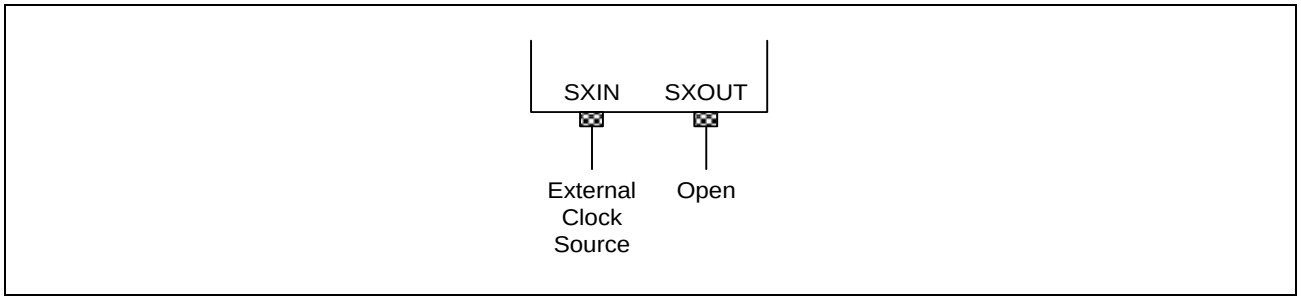


Figure 88. External Clock

21.19 Sub Oscillation Characteristics

Table 37. Sub Oscillation Stabilization Characteristics

(T_A=-40°C ~ +85°C, VDD=2.0V ~ 5.5V)

Oscillator	Parameter	MIN	TYP	MAX	Unit
Crystal	T_A=-40°C ~+85°C	–	–	10	s
	T_A= 25°C		500		ms
External Clock	SXIN input high and low width (t_{XH}, t_{XL})	5	–	15	us

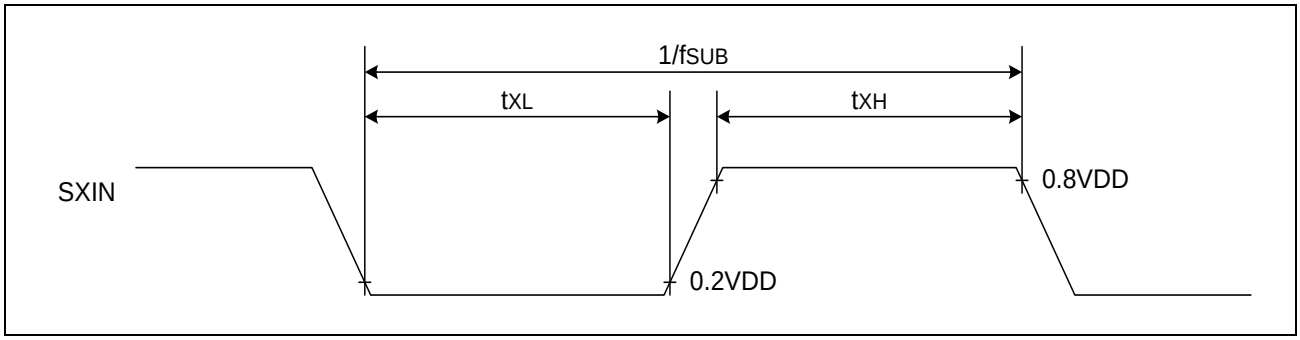


Figure 89. Clock Timing Measurement at SXIN

21.20 Operating Voltage Range

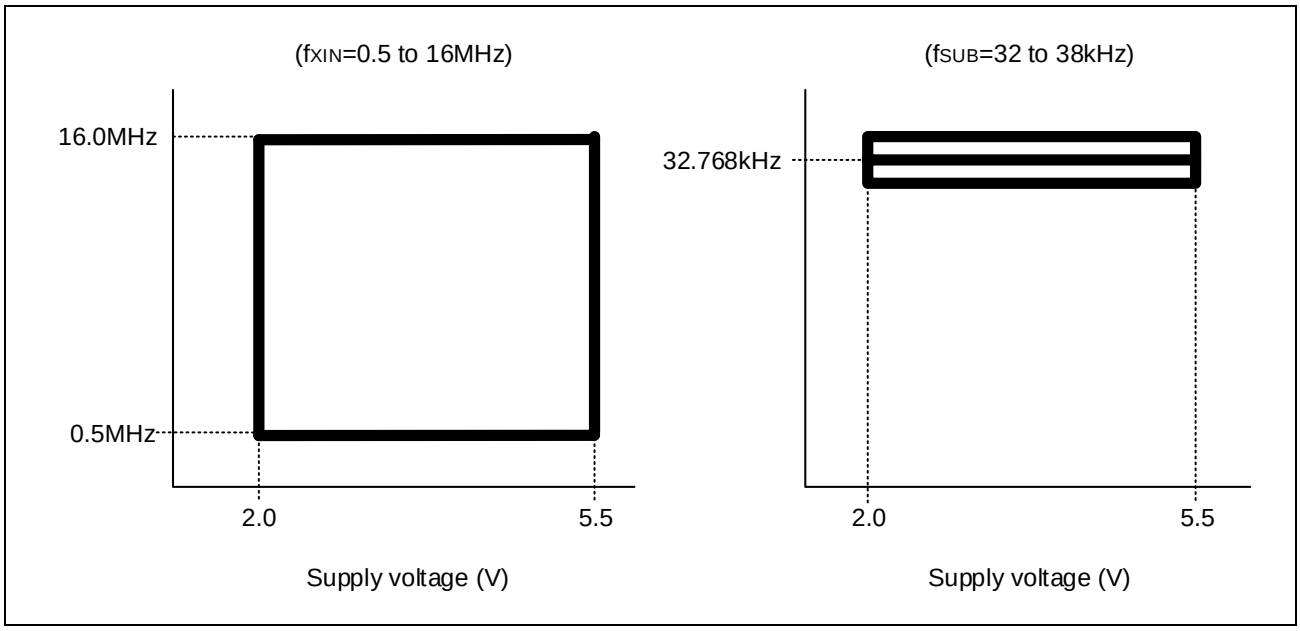


Figure 90. Operating Voltage Range

21.21 Recommended Circuit and Layout

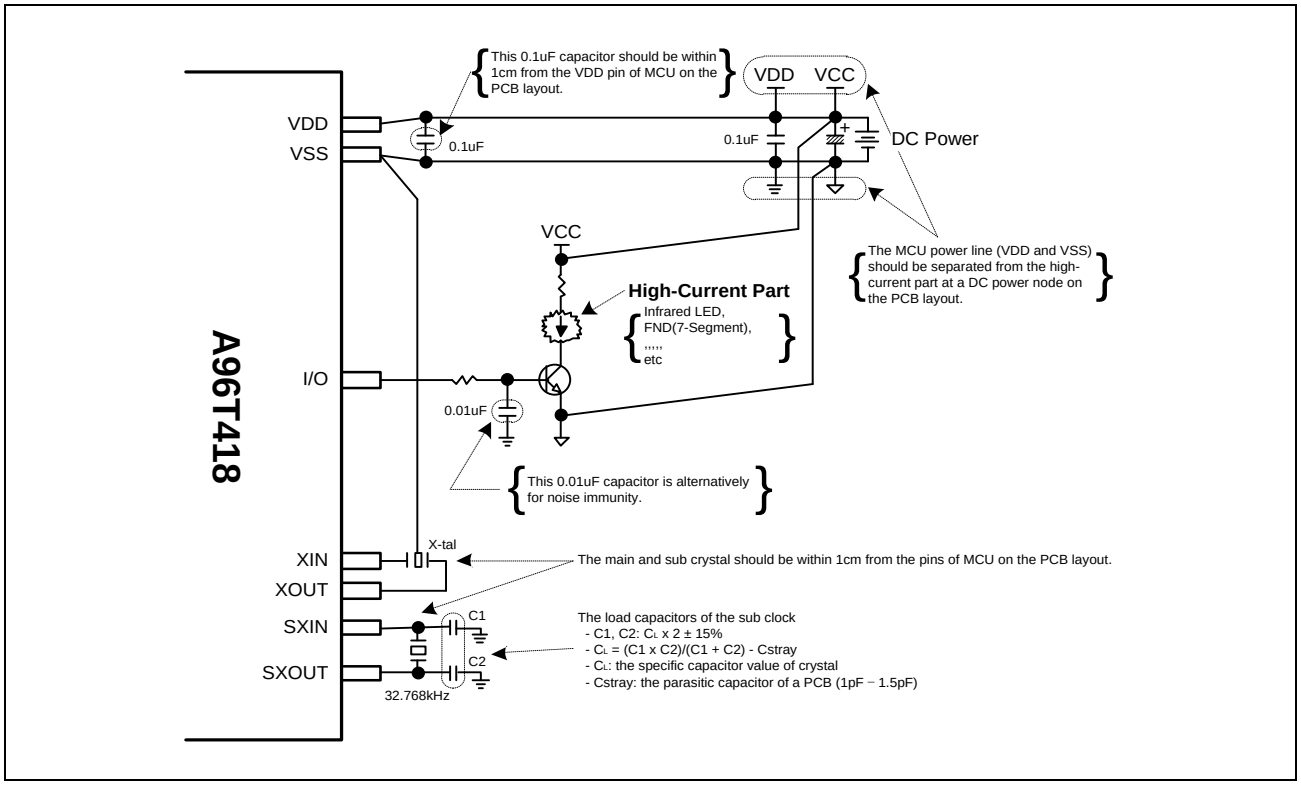


Figure 91. Recommended Voltage Range

21.22 Typical Characteristics

These graphs and tables provided in this section are only for design guidance and are not tested or guaranteed. In graphs or tables some data are out of specified operating range (e.g. out of specified VDD range). This is only for information and devices are guaranteed to operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. “Typical” represents the mean of the distribution while “max” or “min” represents (mean + 3σ) and (mean - 3σ) respectively where σ is standard deviation.

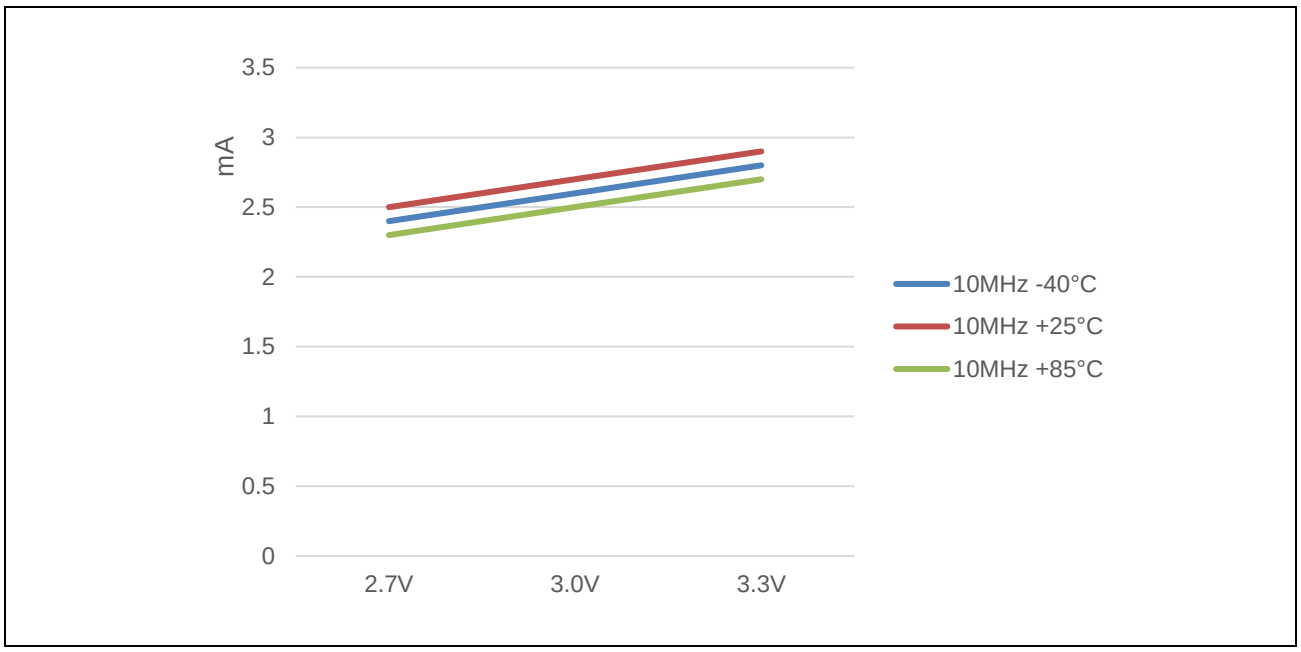


Figure 92. RUN (IDD1) Current

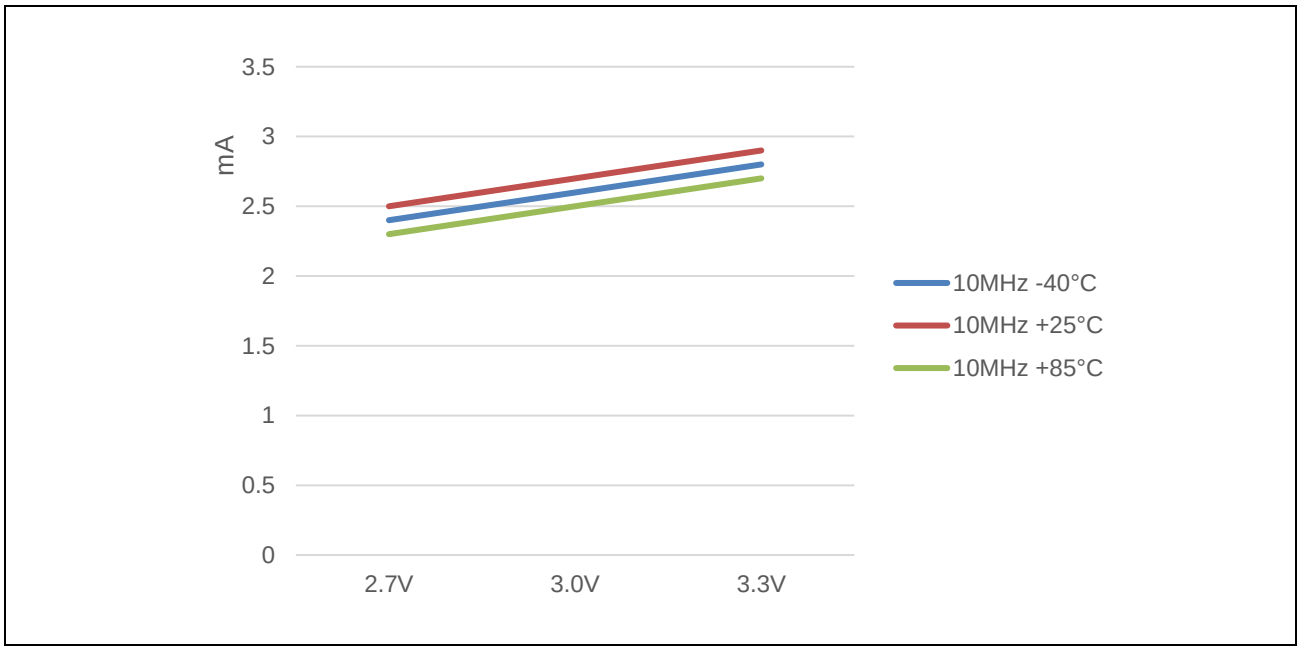


Figure 93. IDLE (IDD2) Current

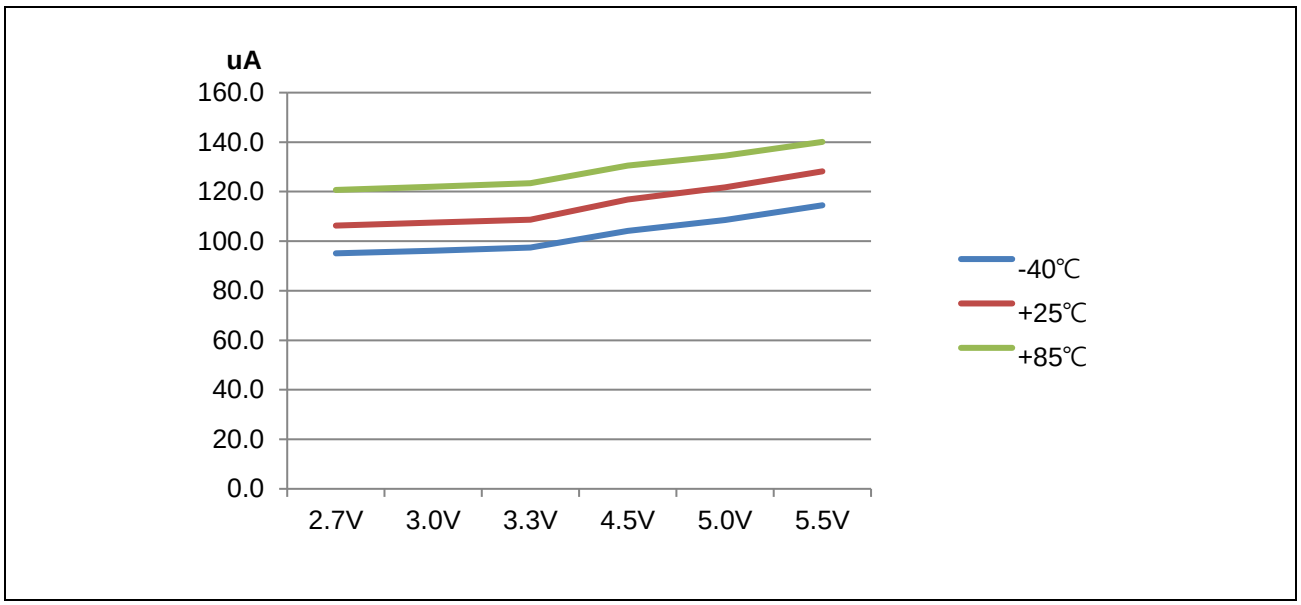


Figure 94. SUB RUN (IDD3) Current

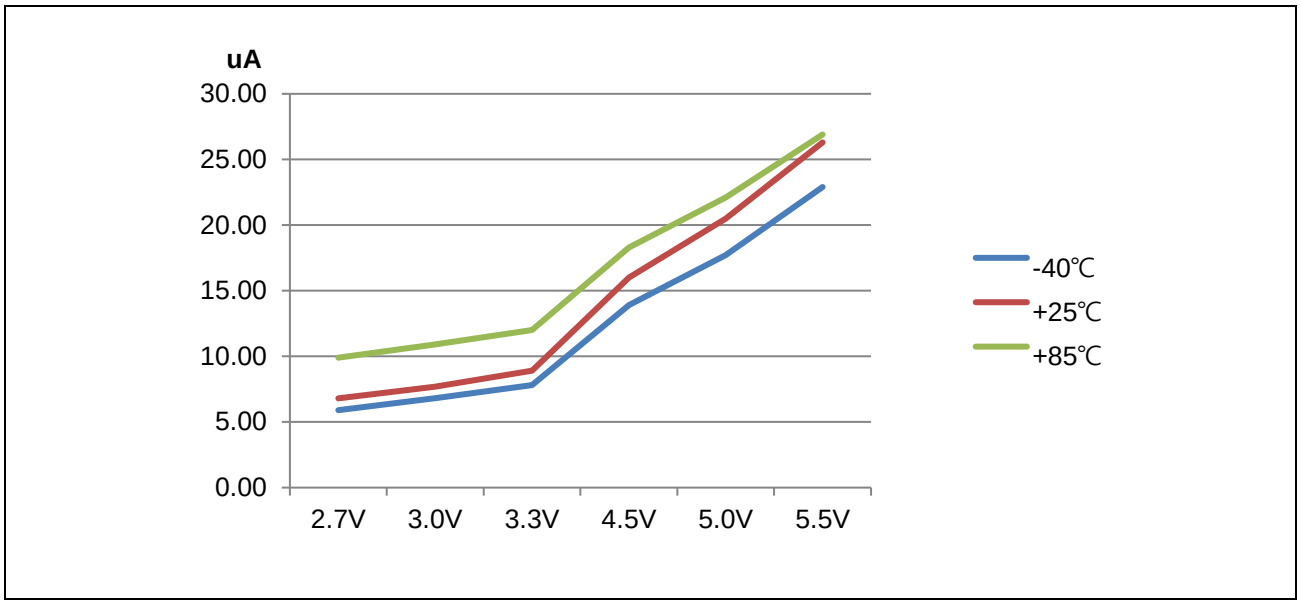


Figure 95. SUB IDLE (IDD4) Current

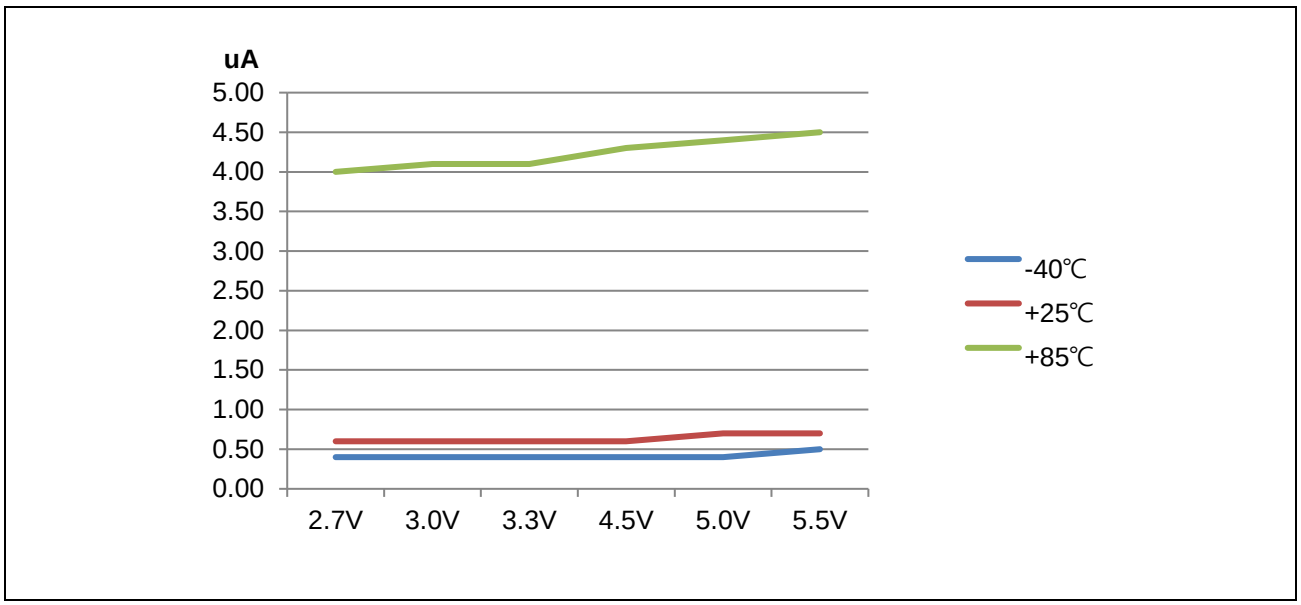


Figure 96. STOP (IDD5) Current

22 Development Tools

This chapter introduces wide range of development tools for A96T418. ABOV offers software tools, debuggers, and programmers to help a user in generating right results to match target applications. ABOV supports entire development ecosystem of the customers.

22.1 Compiler

ABOV Semiconductor does not provide compiler. It is recommended that you consult a compier provider. It is recommended to consult a compiler provider. Since A96T376 has Mentor 8051 as its core, and ROM is smaller than 64Kbytes in size, a developer can use any standard 8051 compiler of other providers.

22.2 OCD(On-chip debugger) emulator and debugger

The OCD emulator supports ABOV's 8051 series MCU emulation. The OCD uses two wires interfacing between PC and MCU, which is attached to user's system. The OCD can read or change the value of MCU's internal memory and I/O peripherals. In addition, the OCD controls MCU's internal debugging logic. This means OCD controls emulation, step run, monitoring and many more functions regarding debugging.

The OCD debugger program runs underneath MS operating system such as MS-Windows NT/ 2000/ XP/ Vista (32-bit). If a user wants to see more details, it is recommend to refer to OCD debugger manual by visiting ABOV's website (http://www.abovsemi.com) and downloading debugger S/W and corresponding manuals.

- Connection:
  - DSCL (A96T418 P02 port)
  - DSDA (A96T418 P01 port)

Figure 97 shows pinouts of OCD connector.

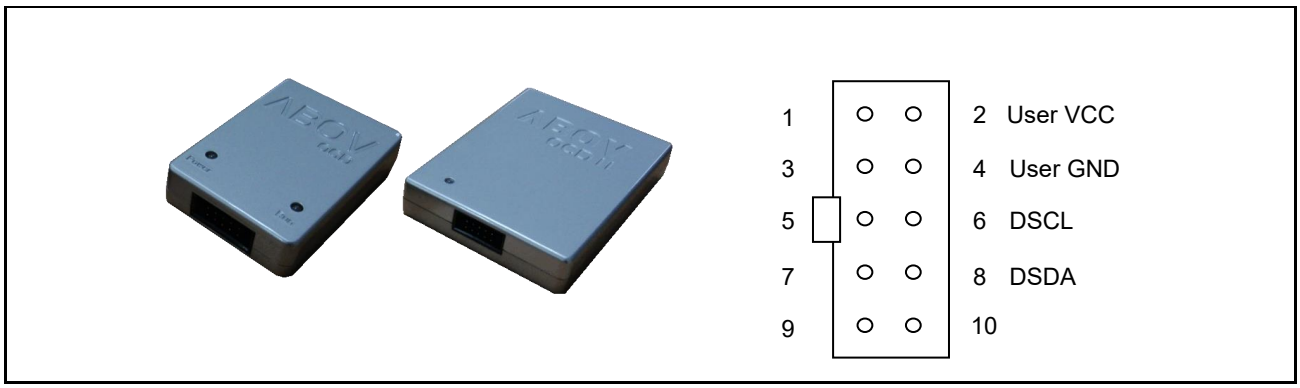


Figure 97. Debugger(OCD1/OCD2) and pin description

22.3 Programmer

22.3.1 E-PGM+

E-PGM+ USB is a single programmer. A user can program A96T376 directly using the E-PGM+.

- Support ABOV / ADAM devices
- 2~5 times faster than S-PGM+
- Main controller: 32 bit MCU @ 72MHz
- Buffer memory: 1Mbyte

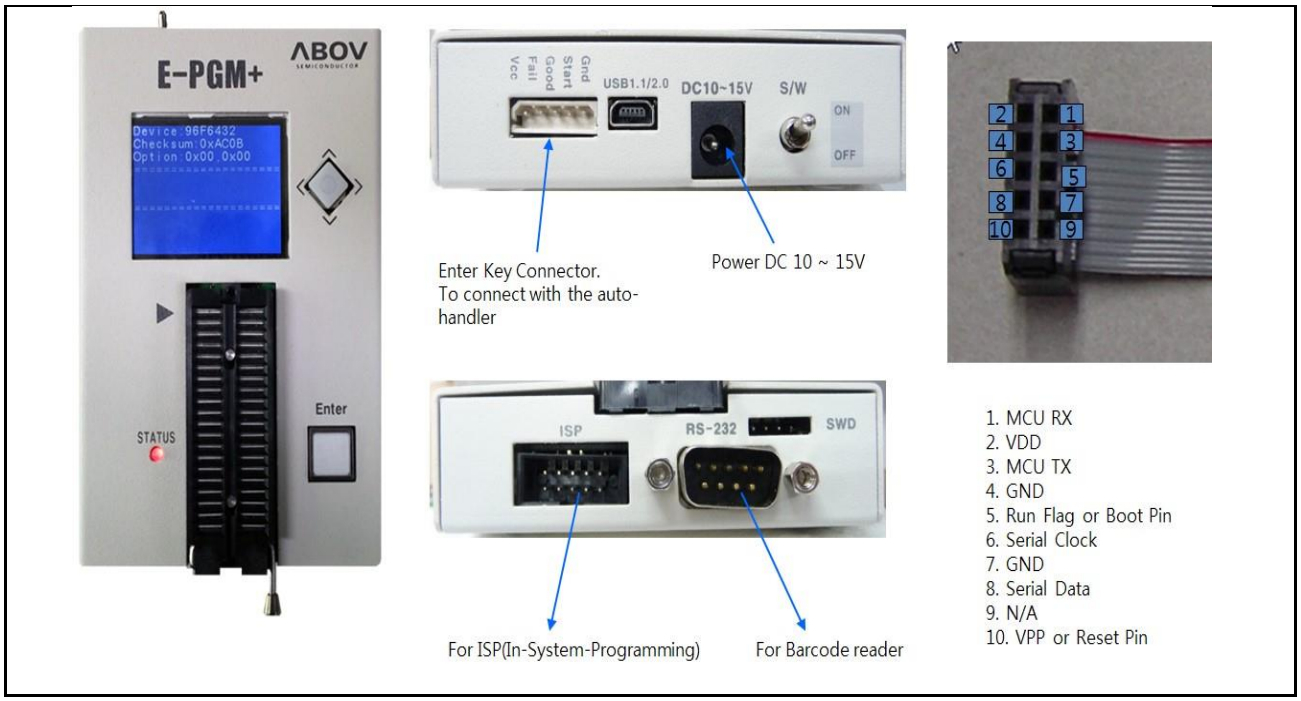


Figure 98. E-PGMplus (Single writer)

22.4 Flash Programming

22.4.1 Overview

The program memory of A96T418 is Flash Type. This flash is accessed by serial data format. There are four pins(DSCL, DSDA, VDD, and VSS) for programming/reading the flash.

Table 38. Descriptions of pins which are used to programming/reading the Flash

Pin name	Main chip pin name	During programming	
		I/O	Description
DSCL	P02	I	Serial clock pin. Input only pin.
DSDA	P01	I/O	Serial data pin. Output port when reading and input port when programming. Can be assigned as input/push-pull output port.
VDD, VSS	VDD, VSS	-	Logic power supply pin.

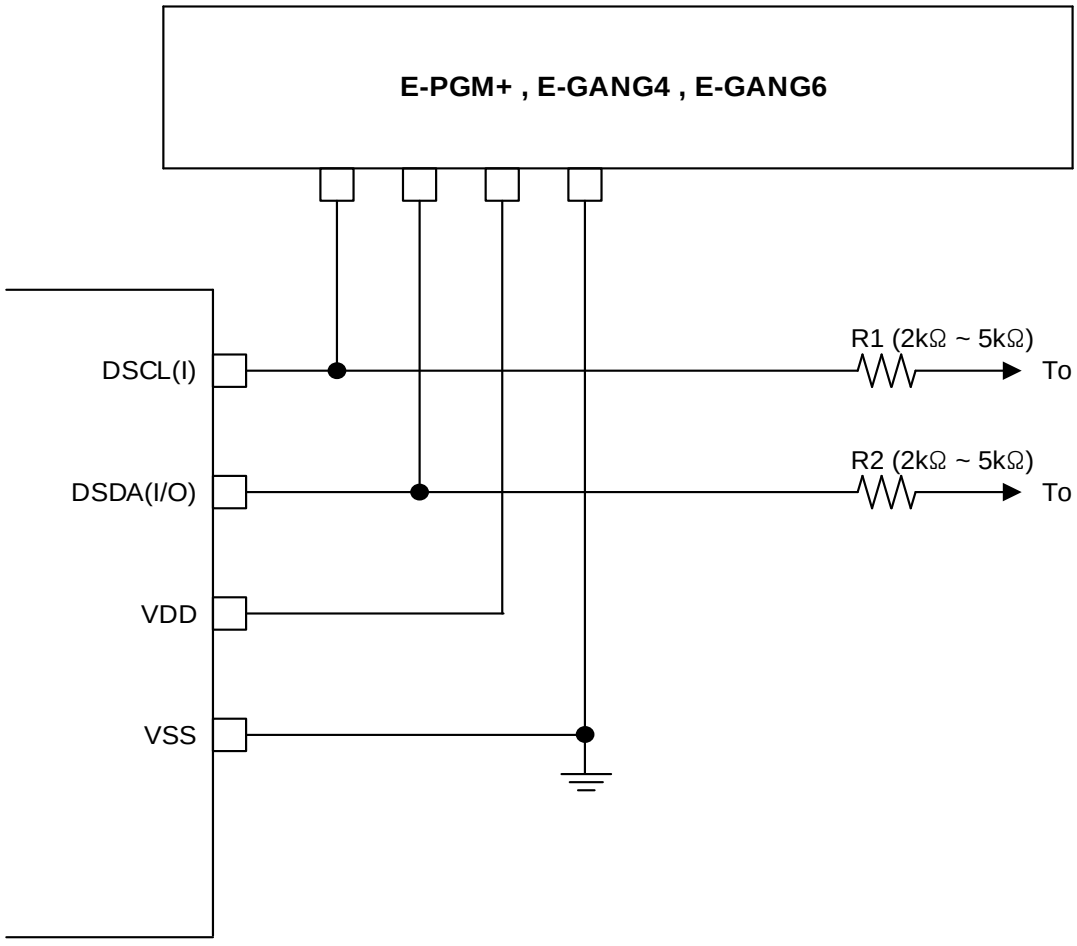
22.4.2 On-Board Programming

The A96T418 needs only four signal lines including VDD and VSS pins for programming FLASH with serial communication protocol. Therefore the on-board programming is possible if the programming signal lines are ready at the PCB of application board is designed.

22.4.3 Circuit Design Guide

When programming flash memory, the programming tool needs 4 signal lines, DSCL, DSDA, VDD, and VSS. If a user designs a PCB circuit, the user should consider the usage of these 4 signal lines for the on-board programming.

Please be careful to design the related circuit of these signal pins because rising/falling timing of DSCL and DSDA is very important for proper programming.



NOTES:

1. In on-board programming mode, very high-speed signal will be provided to pin DSCL and DSDA. And it will cause some damages to the application circuits connected to DSCL or DSDA port if the application circuit is designed as high speed response such as relay control circuit. If possible, the I/O configuration of DSDA, DSCL pins had better be set to input mode.
2. The value of R1 and R2 is recommended value. It varies with circuit of system.

Figure 99. PCB design guide for on board programming

22.4.4 OCD emulator

OCD emulator allows a user to write code on the device too, since OCD debugger supports ISP (In System Programming). It doesn't require additional H/W, except developer's target system.

22.4.5 Gang programmer

E-Gang4 and E-Gang6 allows a user to program on multiple devices at a time. They run not only in PC controlled mode but also in standalone mode without PC control. USB interface is available and it is easy to connect to the handler.

Figure 100. E-GANG4 and E-GANG6 (for Mass Production)

22.5 On-chip Debug System

A96T418supports On-Chip Debug (OCD) system. On-chip debug system of A96T418 can be used for programming the non-volatile memories and on-chip debugging. Detail descriptions for programming via the OCD interface can be found in this section. Features of the OCD is introduced in Table 39.

Table 39. Descriptions of pins which are used to programming/reading the Flash

Two wire external interface	• 1 for serial clock input • 1 for bi-directional serial data bus
Debugger accesses	• All internal peripherals • Internal data RAM • Program Counter • Flash memory and data EEPROM memory
Extensive On-Chip Debugging supports for Break Conditions	• Break instruction • Single step break • Program memory break points on single address • Programming of Flash, EEPROM, Fuses, and Lock bits through the two-wire interface • On-Chip Debugging supported by Dr. Choice®
Operating frequency	The maximum frequency of a target MCU

Figure 101 shows a block diagram of the OCD interface and the OCD system.

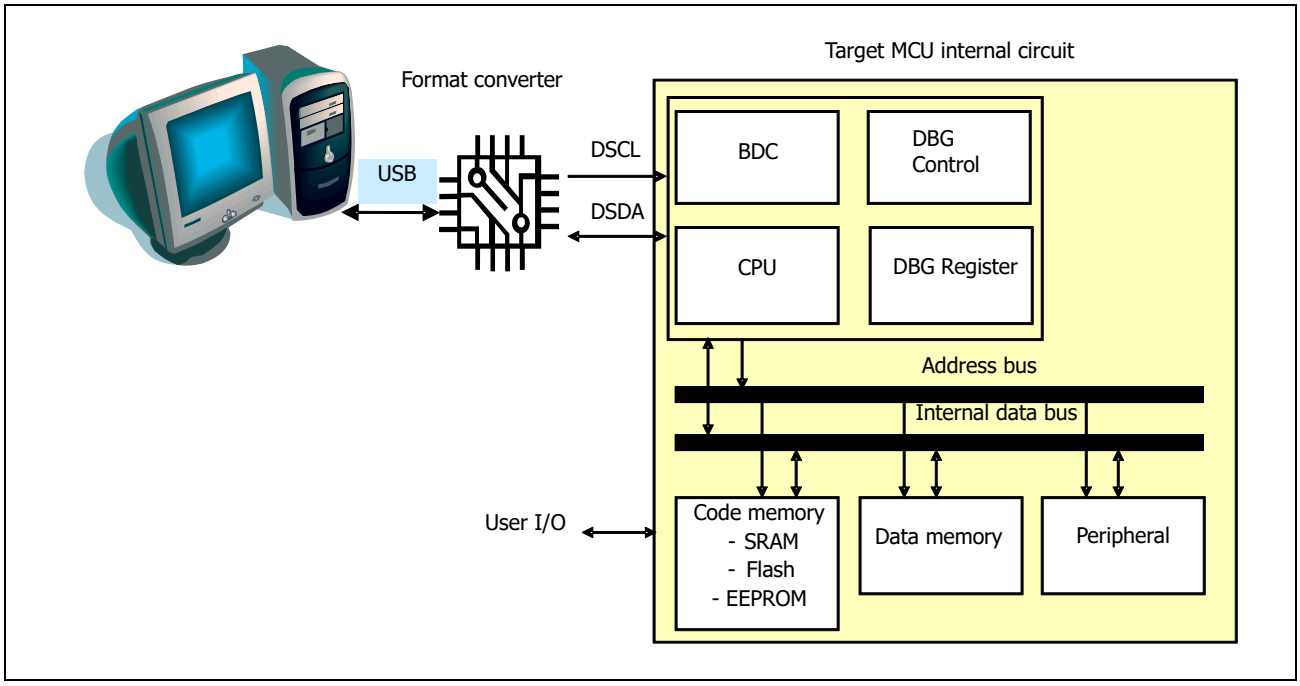


Figure 101. Block Diagram of On-Chip Debug System

22.5.1 Two-Pin External Interface

Basic Transmission Packet

- 10-bit packet transmission using two-pin interface.
- packet consists of 8-bit data, 1-bit parity and 1-bit acknowledge.
- Parity is even of '1' for 8-bit data in transmitter.
- Receiver generates acknowledge bit as '0' when transmission for 8-bit data and its parity has no error.
- When transmitter has no acknowledge (Acknowledge bit is '1' at tenth clock), error process is executed in transmitter.
- When acknowledge error is generated, host PC makes stop condition and transmits command which has error again.
- Background debugger command is composed of a bundle of packet.
- Start condition and stop condition notify the start and the stop of background debugger command respectively.

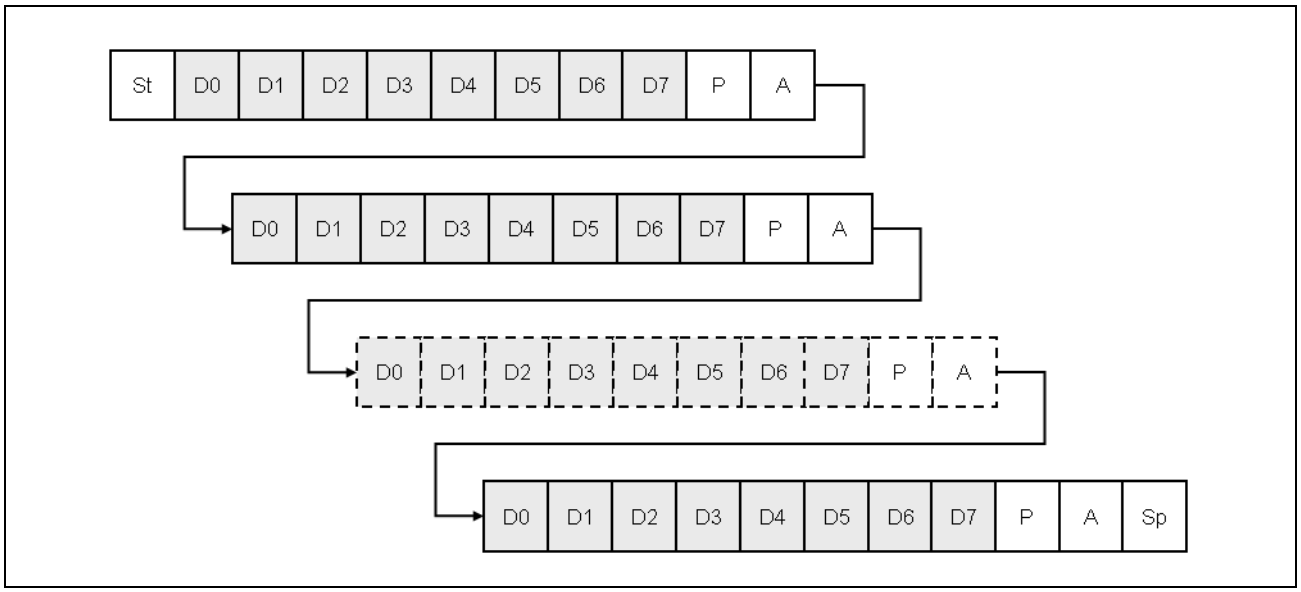


Figure 102. 10-bit Transmission Packet

Packet Transmission Timing

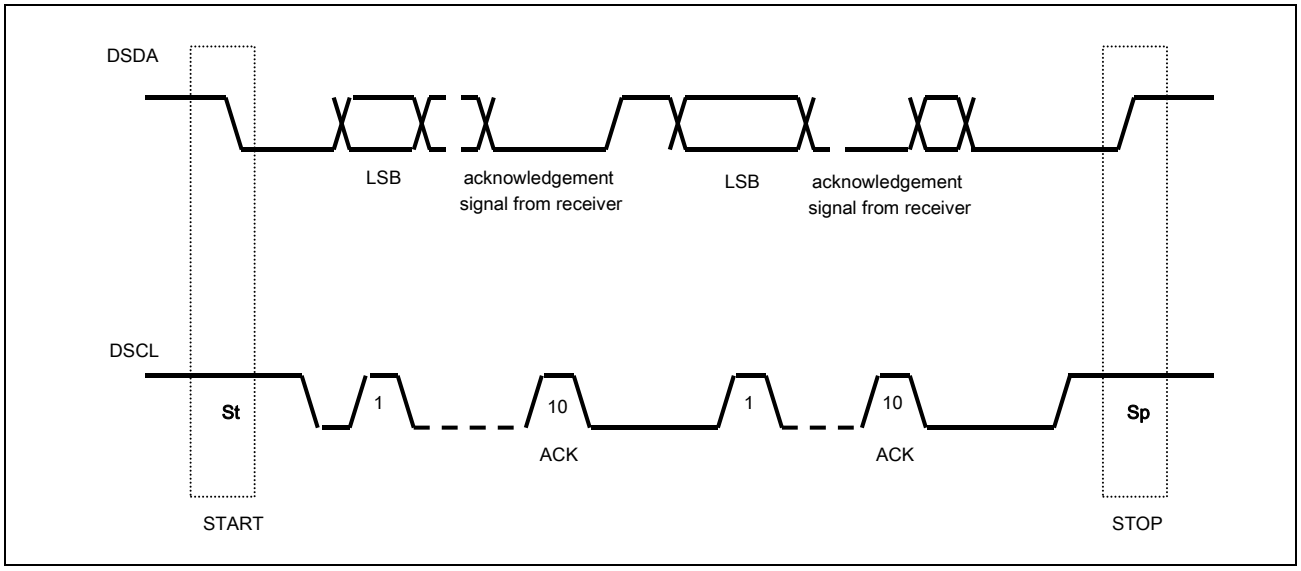


Figure 103. Data Transfer on the Twin Bus

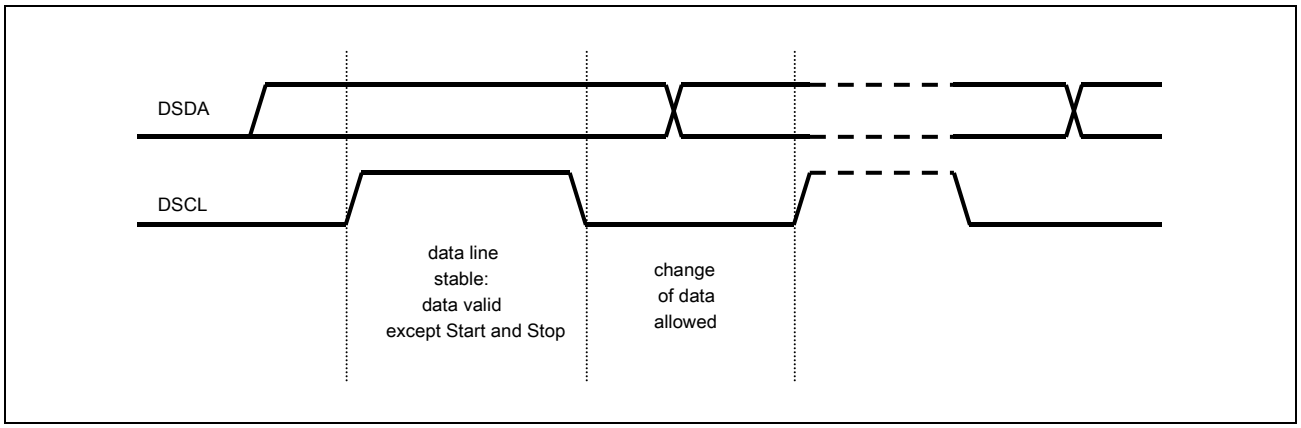


Figure 104. Bit Transfer on the Serial Bus

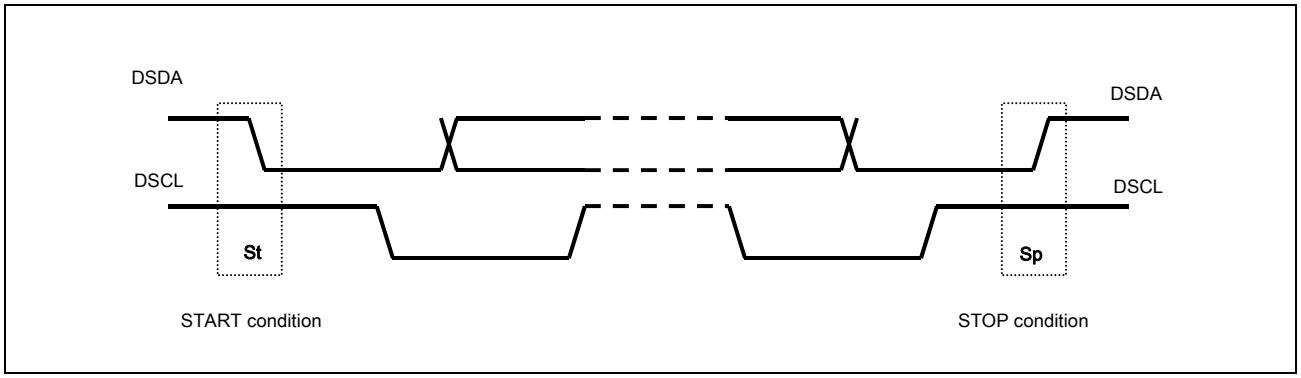


Figure 105. Start and Stop Condition

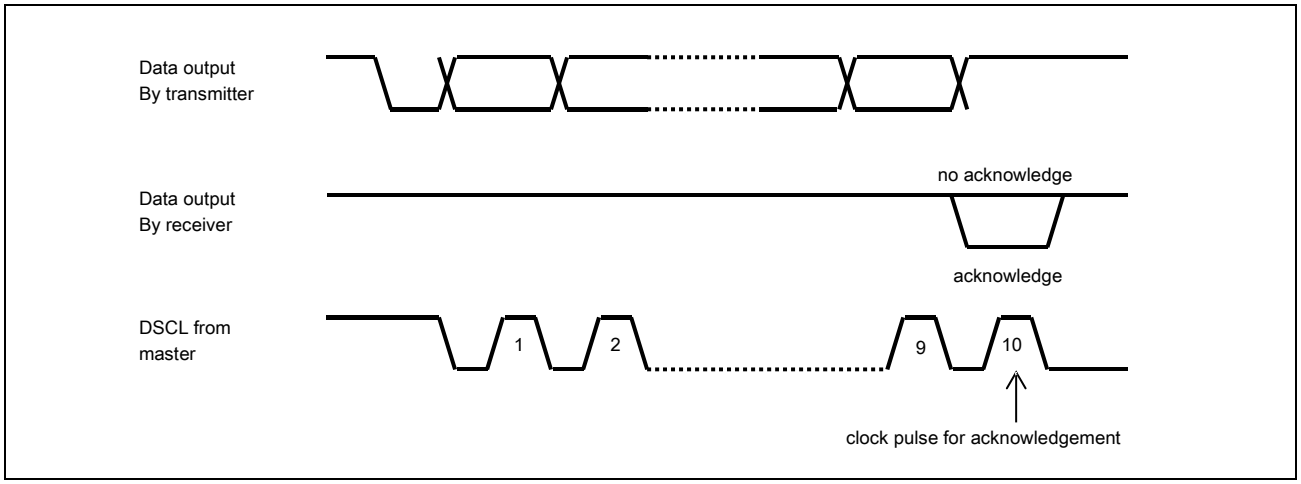


Figure 106. Acknowledge on the Serial Bus

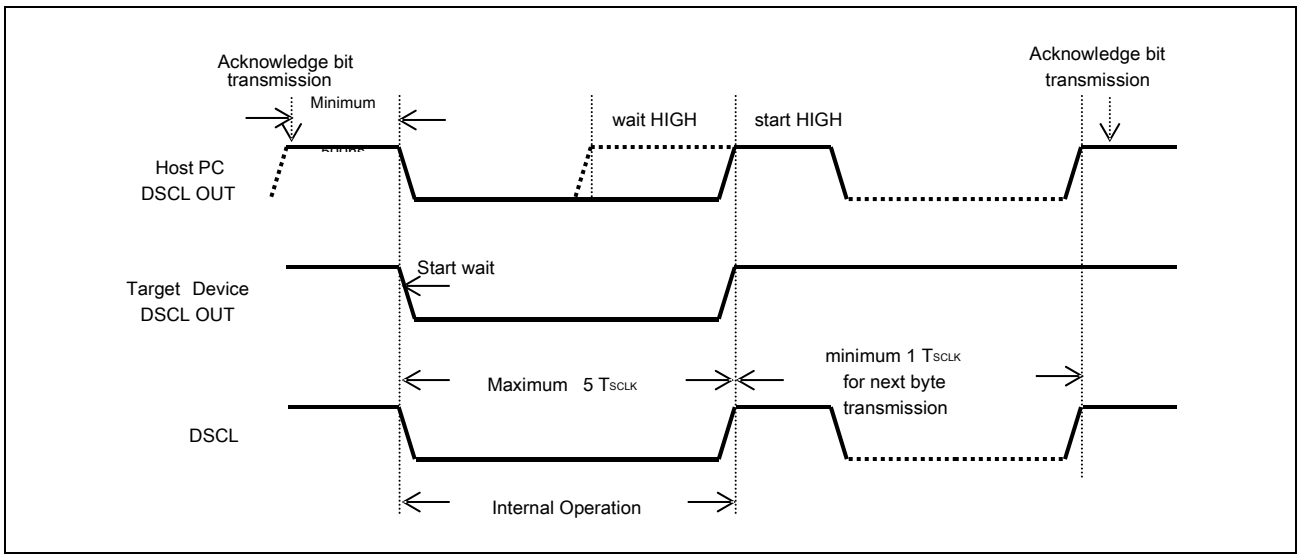


Figure 107. Clock Synchronization during Wait Procedure

Connection of Transmission

Two-pin interface connection uses open-drain(wire-AND bidirectional I/O).

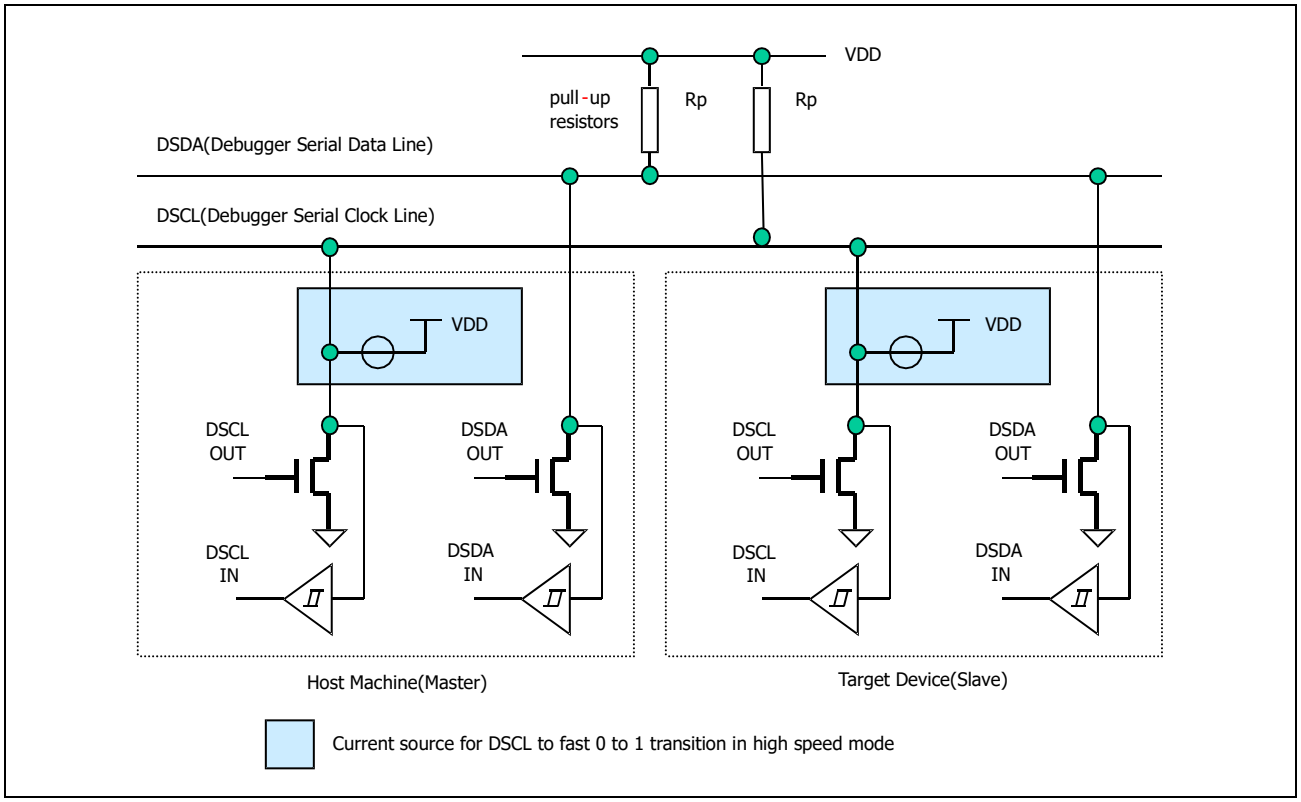


Figure 108. Connection of Transmission

23 Package Diagram

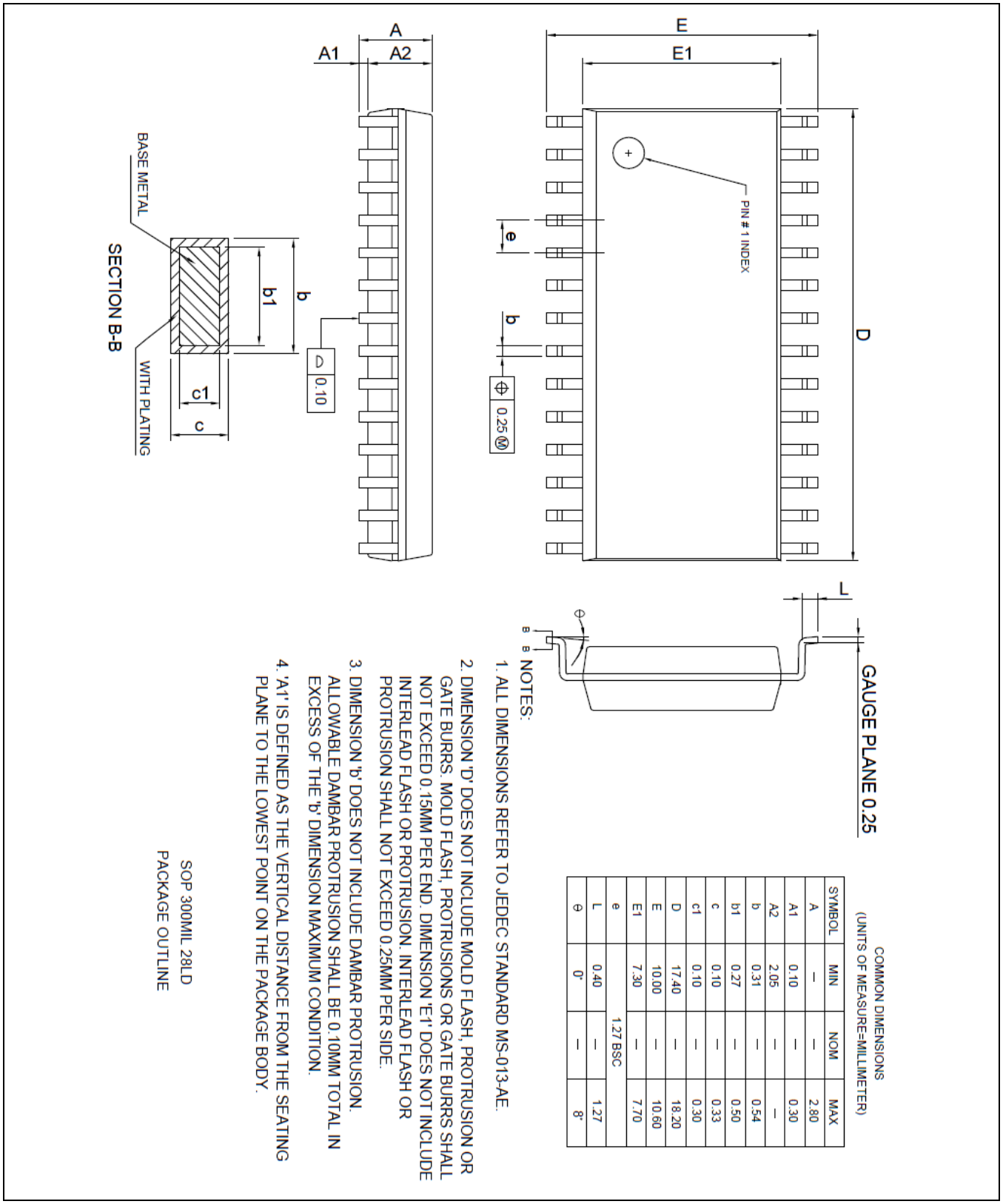


Figure 109. 28-Pin SOP Package

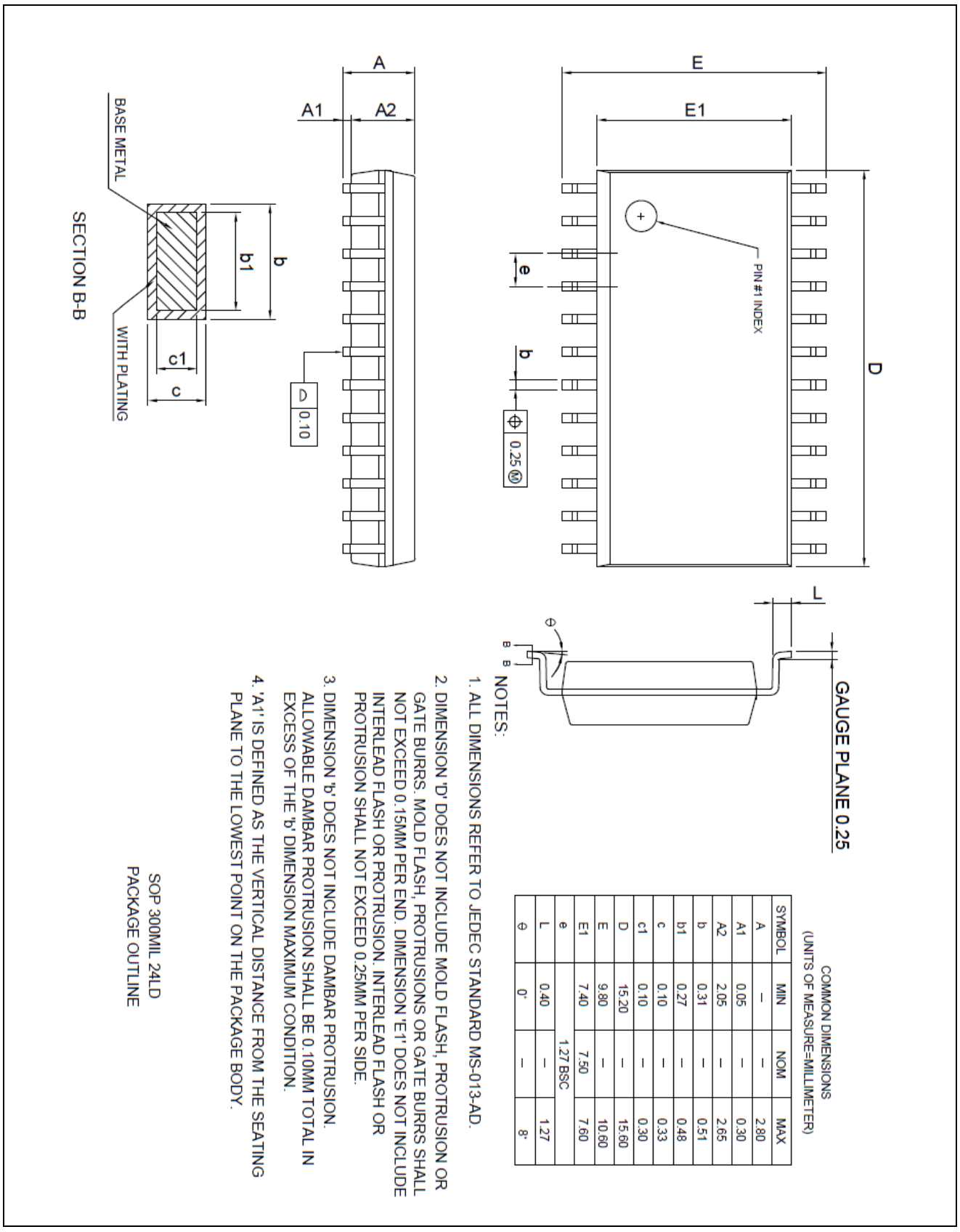
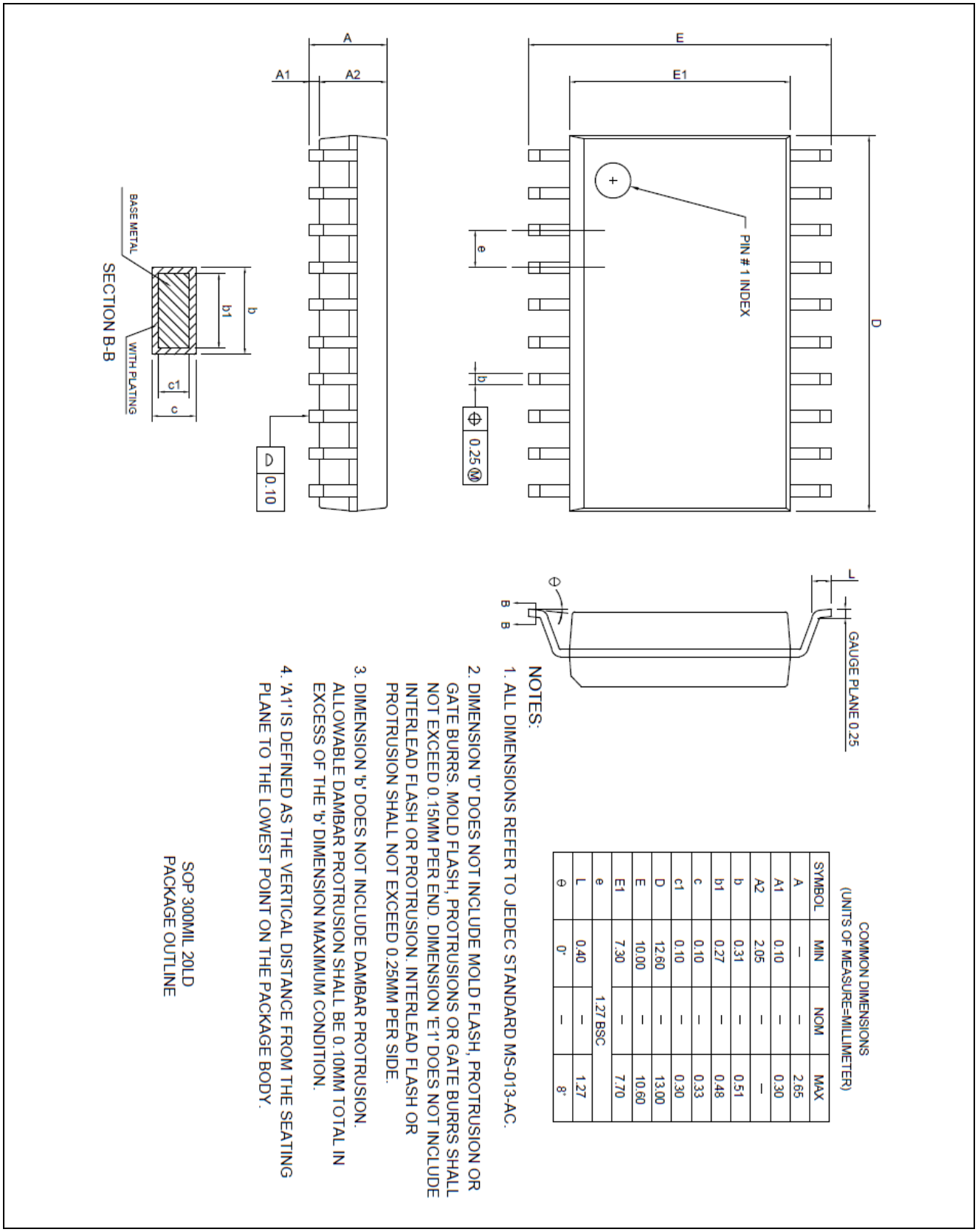


Figure 110. 24-Pin SOP Package



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	—	—	2.65
A1	0.10	—	0.30
A2	2.05	—	—
b	0.31	—	0.51
b1	0.27	—	0.48
c	0.10	—	0.33
c1	0.10	—	0.30
D	12.60	—	13.00
E	10.00	—	10.60
E1	7.30	—	7.70
e		1.27 BSC	
L	0.40	—	1.27
θ	0°	—	8°

NOTES:

1. ALL DIMENSIONS REFER TO JEDEC STANDARD MS-013-AC.
2. DIMENSION 'D' DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15MM PER END. DIMENSION 'E1' DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25MM PER SIDE.
3. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10MM TOTAL IN EXCESS OF THE 'b' DIMENSION MAXIMUM CONDITION.
4. 'A1' IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

SOP 300MIL 20LD
PACKAGE OUTLINE

Figure 111. 20-Pin SOP Package

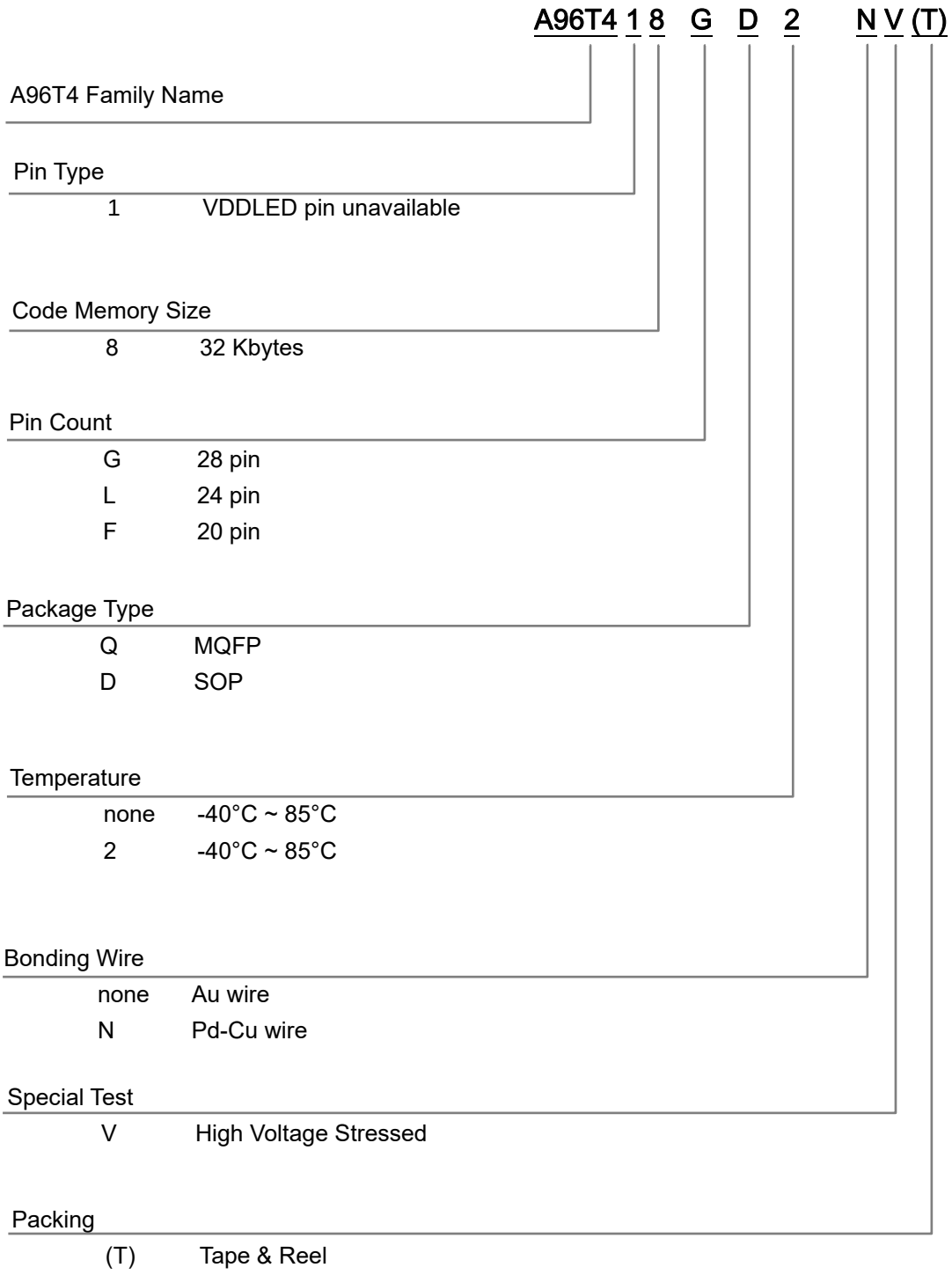
24 Ordering Information

Table 40. Ordering Information of A96T418

Device Name	FLASH	XRAM	IRAM	Touch Switch	LED Driver	ADC	I/O PORT	Package
A96T418GD	32Kbytes	1792bytes	256bytes	20-ch	8COM / 16SEG	8inputs	25	28 SOP
A96T418LD*				17-ch	8COM / 16SEG	8inputs	21	24 SOP
A96T418FD*				13-ch	8COM / 15SEG	8inputs	17	20 SOP

* For available options or further information on the device with an "*" mark, please contact the ABOV sales office.

Device Nomenclature



Appendix

Instruction Table

Instructions are either1, 2 or 3bytes long as listed in the 'Bytes' column below.

Each instruction takes either 1, 2 or 4 machine cycles to execute as listed in the following table. 1 machine cycle comprises 2 system clock cycles.

ARITHMETIC				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
ADD A,Rn	Add register to A	1	1	28-2F
ADD A,dir	Add direct byte to A	2	1	25
ADD A,@Ri	Add indirect memory to A	1	1	26-27
ADD A,#data	Add immediate to A	2	1	24
ADDC A,Rn	Add register to A with carry	1	1	38-3F
ADDC A,dir	Add direct byte to A with carry	2	1	35
ADDC A,@Ri	Add indirect memory to A with carry	1	1	36-37
ADDC A,#data	Add immediate to A with carry	2	1	34
SUBB A,Rn	Subtract register from A with borrow	1	1	98-9F
SUBB A,dir	Subtract direct byte from A with borrow	2	1	95
SUBB A,@Ri	Subtract indirect memory from A with borrow	1	1	96-97
SUBB A,#data	Subtract immediate from A with borrow	2	1	94
INC A	Increment A	1	1	04
INC Rn	Increment register	1	1	08-0F
INC dir	Increment direct byte	2	1	05
INC @Ri	Increment indirect memory	1	1	06-07
DEC A	Decrement A	1	1	14
DEC Rn	Decrement register	1	1	18-1F
DEC dir	Decrement direct byte	2	1	15
DEC @Ri	Decrement indirect memory	1	1	16-17
INC DPTR	Increment data pointer	1	2	A3
MUL AB	Multiply A by B	1	4	A4
DIV AB	Divide A by B	1	4	84
DA A	Decimal Adjust A	1	1	D4

LOGICAL				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
ANL A,Rn	AND register to A	1	1	58-5F
ANL A,dir	AND direct byte to A	2	1	55
ANL A,@Ri	AND indirect memory to A	1	1	56-57
ANL A,#data	AND immediate to A	2	1	54
ANL dir,A	AND A to direct byte	2	1	52
ANL dir,#data	AND immediate to direct byte	3	2	53
ORL A,Rn	OR register to A	1	1	48-4F
ORL A,dir	OR direct byte to A	2	1	45
ORL A,@Ri	OR indirect memory to A	1	1	46-47
ORL A,#data	OR immediate to A	2	1	44
ORL dir,A	OR A to direct byte	2	1	42
ORL dir,#data	OR immediate to direct byte	3	2	43
XRL A,Rn	Exclusive-OR register to A	1	1	68-6F
XRL A,dir	Exclusive-OR direct byte to A	2	1	65
XRL A, @Ri	Exclusive-OR indirect memory to A	1	1	66-67
XRL A,#data	Exclusive-OR immediate to A	2	1	64
XRL dir,A	Exclusive-OR A to direct byte	2	1	62
XRL dir,#data	Exclusive-OR immediate to direct byte	3	2	63
CLR A	Clear A	1	1	E4
CPL A	Complement A	1	1	F4
SWAP A	Swap Nibbles of A	1	1	C4
RL A	Rotate A left	1	1	23
RLC A	Rotate A left through carry	1	1	33
RR A	Rotate A right	1	1	03
RRC A	Rotate A right through carry	1	1	13

DATA TRANSFER				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
MOV A,Rn	Move register to A	1	1	E8-EF
MOV A,dir	Move direct byte to A	2	1	E5
MOV A,@Ri	Move indirect memory to A	1	1	E6-E7
MOV A,#data	Move immediate to A	2	1	74
MOV Rn,A	Move A to register	1	1	F8-FF
MOV Rn,dir	Move direct byte to register	2	2	A8-AF
MOV Rn,#data	Move immediate to register	2	1	78-7F
MOV dir,A	Move A to direct byte	2	1	F5
MOV dir,Rn	Move register to direct byte	2	2	88-8F
MOV dir,dir	Move direct byte to direct byte	3	2	85
MOV dir,@Ri	Move indirect memory to direct byte	2	2	86-87
MOV dir,#data	Move immediate to direct byte	3	2	75
MOV @Ri,A	Move A to indirect memory	1	1	F6-F7
MOV @Ri,dir	Move direct byte to indirect memory	2	2	A6-A7
MOV @Ri,#data	Move immediate to indirect memory	2	1	76-77
MOV DPTR,#data	Move immediate to data pointer	3	2	90
MOVC A,@A+DPTR	Move code byte relative DPTR to A	1	2	93
MOVC A,@A+PC	Move code byte relative PC to A	1	2	83
MOVX A,@Ri	Move external data(A8) to A	1	2	E2-E3
MOVX A,@DPTR	Move external data(A16) to A	1	2	E0
MOVX @Ri,A	Move A to external data(A8)	1	2	F2-F3
MOVX @DPTR,A	Move A to external data(A16)	1	2	F0
PUSH dir	Push direct byte onto stack	2	2	C0
POP dir	Pop direct byte from stack	2	2	D0
XCH A,Rn	Exchange A and register	1	1	C8-CF
XCH A,dir	Exchange A and direct byte	2	1	C5
XCH A,@Ri	Exchange A and indirect memory	1	1	C6-C7
XCHD A,@Ri	Exchange A and indirect memory nibble	1	1	D6-D7

BOOLEAN				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
CLR C	Clear carry	1	1	C3
CLR bit	Clear direct bit	2	1	C2
SETB C	Set carry	1	1	D3
SETB bit	Set direct bit	2	1	D2
CPL C	Complement carry	1	1	B3
CPL bit	Complement direct bit	2	1	B2
ANL C,bit	AND direct bit to carry	2	2	82
ANL C,/bit	AND direct bit inverse to carry	2	2	B0
ORL C,bit	OR direct bit to carry	2	2	72
ORL C,/bit	OR direct bit inverse to carry	2	2	A0
MOV C,bit	Move direct bit to carry	2	1	A2
MOV bit,C	Move carry to direct bit	2	2	92

BRANCHING				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
ACALL addr 11	Absolute jump to subroutine	2	2	11→F1
LCALL addr 16	Long jump to subroutine	3	2	12
RET	Return from subroutine	1	2	22
RETI	Return from interrupt	1	2	32
AJMP addr 11	Absolute jump unconditional	2	2	01→E1
LJMP addr 16	Long jump unconditional	3	2	02
SJMP rel	Short jump (relative address)	2	2	80
JC rel	Jump on carry = 1	2	2	40
JNC rel	Jump on carry = 0	2	2	50
JB bit,rel	Jump on direct bit = 1	3	2	20
JNB bit,rel	Jump on direct bit = 0	3	2	30
JBC bit,rel	Jump on direct bit = 1 and clear	3	2	10
JMP @A+DPTR	Jump indirect relative DPTR	1	2	73
JZ rel	Jump on accumulator = 0	2	2	60
JNZ rel	Jump on accumulator ≠0	2	2	70
CJNE A,dir,rel	Compare A,direct jne relative	3	2	B5
CJNE A,#d,rel	Compare A,immediate jne relative	3	2	B4
CJNE Rn,#d,rel	Compare register, immediate jne relative	3	2	B8-BF
CJNE @Ri,#d,rel	Compare indirect, immediate jne relative	3	2	B6-B7
DJNZ Rn,rel	Decrement register, jnz relative	2	2	D8-DF
DJNZ dir,rel	Decrement direct byte, jnz relative	3	2	D5

MISCELLANEOUS				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
NOP	No operation	1	1	00

ADDITIONAL INSTRUCTIONS (selected through EO[7:4])				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
MOVC @(DPTR++),A	M8051W/M8051EW-specific instruction supporting software download into program memory	1	2	A5
TRAP	Software break command	1	1	A5

In the above table, an entry such as E8-EF indicates a continuous block of hex opcodes used for 8 different registers, the register numbers of which are defined by the lowest three bits of the corresponding code. Non-continuous blocks of codes, shown as 11→F1 (for example), are used for absolute jumps and calls, with the top 3 bits of the code being used to store the top three bits of the destination address.

The CJNE instructions use the abbreviation #d for immediate data; other instructions use #data.

Revision History

Version	Date	Revision list
1.00	2020.10.12	The First Release.
1.01	2021.02.10	HSIRC tolerance table updated. detailed DC Characteristics of LED drive current.
1.02	2021.04.28	HSIRC tolerance table updated.
1.03	2021.10.28	LED driver of Feature table updated.
1.04	2021.11.23	Buzzer block diagram, frequency table, and BUZCR reg. updated.

Korea

Regional Office, Seoul
R&D, Marketing & Sales
8th Fl., 330, Yeongdong-daero,
Gangnam-gu, Seoul,
06177, Korea

Tel: +82-2-2193-2200
Fax: +82-2-508-6903
http://www.abovsemi.com/

HQ, Ochang
R&D, QA, and Test Center
93, Gangni 1-gil, Ochang-eup, Cheongwon-gun,
Chungcheongbuk-do,
28126, Korea

Tel: +82-43-219-5200
Fax: +82-43-217-3534
http://www.abovsemi.com/

Domestic Sales Manager
Tel: +82-2-2193-2206
Fax: +82-2-508-6903
Email: sales_kr@abov.co.kr

Global Sales Manager
Tel: +82-2-2193-2281
Fax: +82-2-508-6903
Email: sales_gl@abov.co.kr

China Sales Manager
Tel: +86-755-8287-2205
Fax: +86-755-8287-2204
Email: sales_cn@abov.co.kr