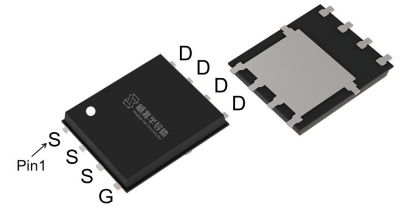


## Features

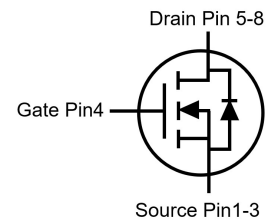
- Enhancement mode
- VitoMOS<sup>®</sup> II Technology
- Fast Switching and High efficiency
- 100% Avalanche Tested

$V_{DS}$	40	V
$R_{DS(on),TYP@ V_{GS}=10V}$	6.5	mΩ
$R_{DS(on),TYP@ V_{GS}=4.5V}$	10	mΩ
$I_{D(Silicon Limited)}$	40	A
$I_{D(Package Limited)}$	23	A

### PDFN5x6



Part ID	Package Type	Marking	Packing
VS4620GP	PDFN5x6	4620GP	3000pcs/Reel



## Maximum ratings, at $T_A=25\text{ }^\circ\text{C}$ , unless otherwise specified

Symbol	Parameter	Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage	40	V
$V_{GS}$	Gate-Source voltage	$\pm 20$	V
$I_S$	Diode continuous forward current	$T_C = 25^\circ\text{C}$	40 A
$I_D$	Continuous drain current @ $V_{GS}=10V$ (Silicon limited)	$T_C = 25^\circ\text{C}$	40 A
$I_D$	Continuous drain current @ $V_{GS}=10V$ (Silicon limited)	$T_C = 100^\circ\text{C}$	25 A
$I_D$	Continuous drain current @ $V_{GS}=10V$ (Wire bond limited)	$T_C = 25^\circ\text{C}$	23 A
$I_{DM}$	Pulse drain current tested ①	$T_C = 25^\circ\text{C}$	160 A
$I_{DSM}$	Continuous drain current @ $V_{GS}=10V$	$T_A = 25^\circ\text{C}$	13 A
		$T_A = 70^\circ\text{C}$	10 A
$E_{AS}$	Avalanche energy, single pulsed ②	16	mJ
$P_D$	Maximum power dissipation	$T_C = 25^\circ\text{C}$	22 W
		$T_C = 100^\circ\text{C}$	8.6 W
$P_{DSM}$	Maximum power dissipation ③	$T_A = 25^\circ\text{C}$	2.1 W
		$T_A = 70^\circ\text{C}$	1.3 W
$T_{STG,TJ}$	Storage and Junction Temperature Range	-55 to 150	$^\circ\text{C}$

## Thermal Characteristics

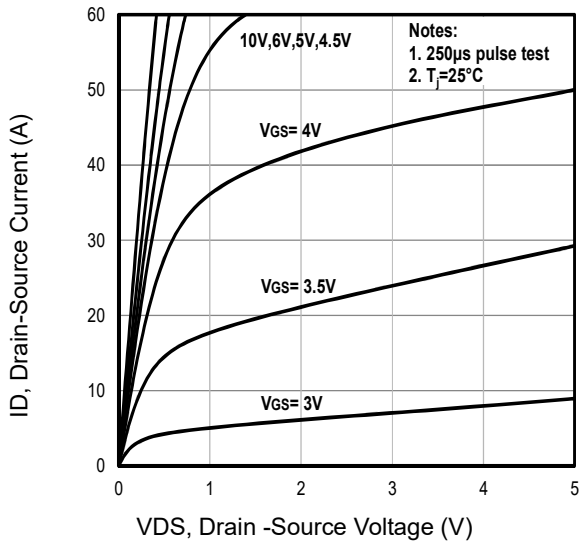
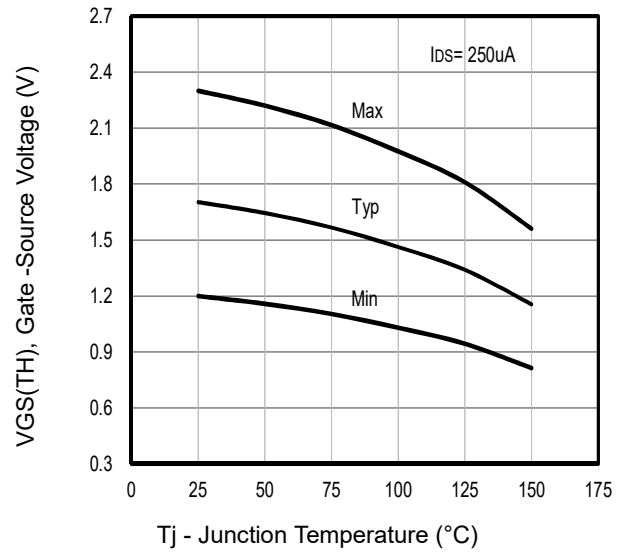
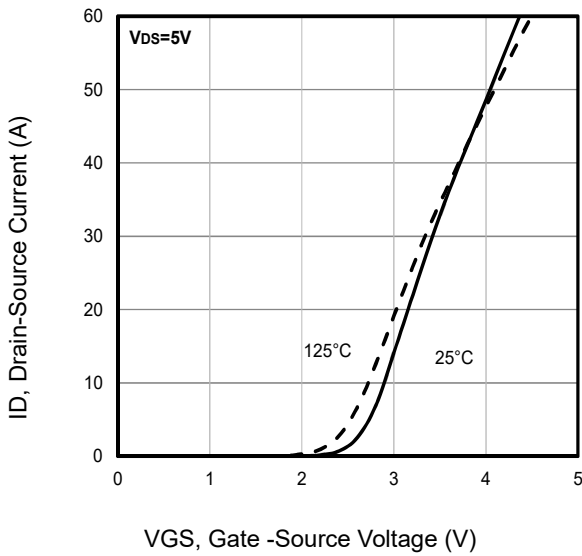
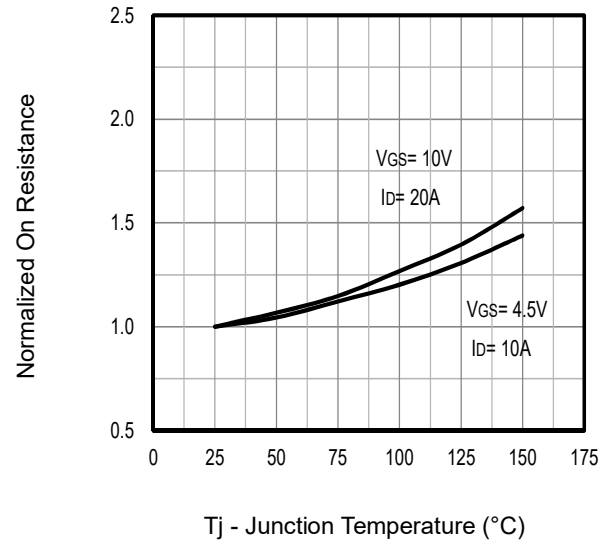
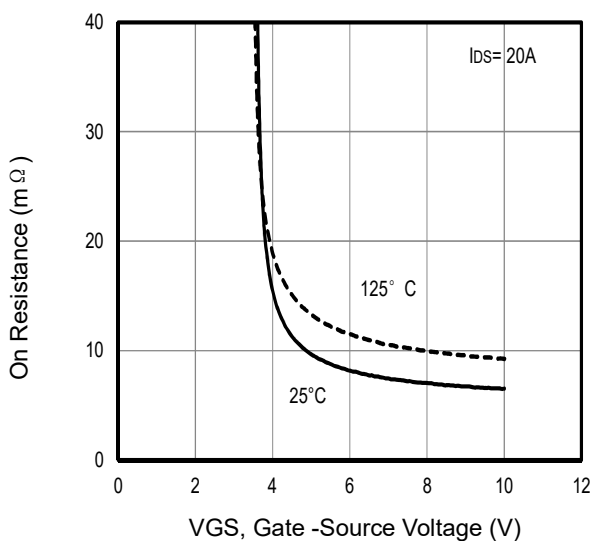
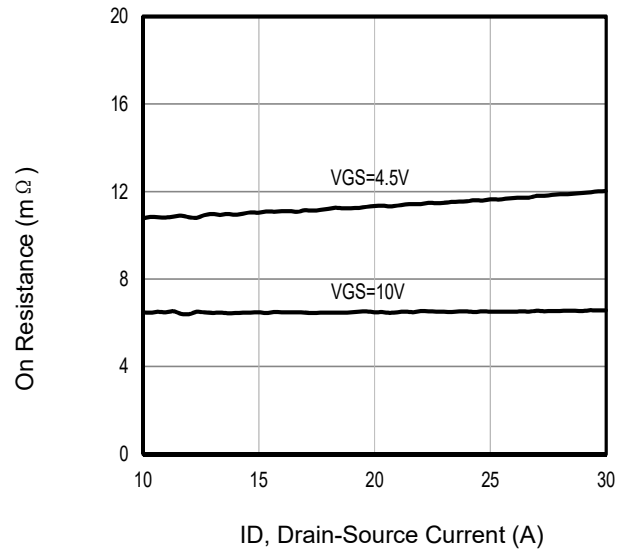
Symbol	Parameter	Typical	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	4.8	5.8	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	50	60	$^\circ\text{C/W}$

**Electrical Characteristics**

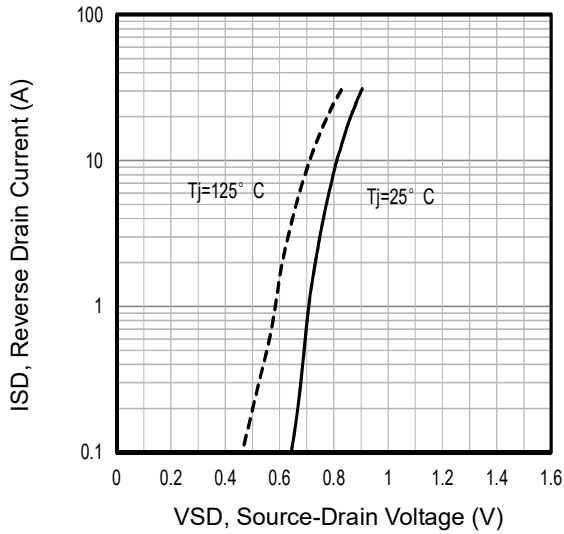
Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
<b>Static Electrical Characteristics @ T<sub>j</sub> = 25°C (unless otherwise stated)</b>						
V(BR)DSS	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	40	--	--	V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current(T <sub>j</sub> =25°C)	V <sub>DS</sub> =40V, V <sub>GS</sub> =0V	--	--	1	μA
	Zero Gate Voltage Drain Current(T <sub>j</sub> =125°C)	V <sub>DS</sub> =40V, V <sub>GS</sub> =0V	--	--	100	μA
I <sub>GSS</sub>	Gate-Body Leakage Current	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	--	--	±100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.2	1.7	2.3	V
R <sub>DS(on)</sub>	Drain-Source On-State Resistance ④	V <sub>GS</sub> =10V, I <sub>D</sub> =20A	--	6.5	8.5	mΩ
		T <sub>j</sub> =100°C	--	8.3	--	mΩ
R <sub>DS(on)</sub>	Drain-Source On-State Resistance ④	V <sub>GS</sub> =4.5V, I <sub>D</sub> =10A	--	10	13	mΩ
<b>Dynamic Electrical Characteristics @ T<sub>j</sub> = 25°C (unless otherwise stated)</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =20V, V <sub>GS</sub> =0V, f=1MHz	410	815	1425	pF
C <sub>oss</sub>	Output Capacitance		130	265	460	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		15	30	60	pF
R <sub>g</sub>	Gate Resistance	f=1MHz	0.2	2.3	5	Ω
Q <sub>g(10V)</sub>	Total Gate Charge	V <sub>DS</sub> =20V, I <sub>D</sub> =20A, V <sub>GS</sub> =10V	--	15.5	27	nC
Q <sub>g(4.5V)</sub>	Total Gate Charge		--	7.7	13	nC
Q <sub>gs</sub>	Gate-Source Charge		--	3.1	5.4	nC
Q <sub>gd</sub>	Gate-Drain Charge		--	3.3	5.8	nC
<b>Switching Characteristics</b>						
T <sub>d(on)</sub>	Turn-on Delay Time	V <sub>DD</sub> =20V, I <sub>D</sub> =20A, R <sub>G</sub> =3Ω, V <sub>GS</sub> =10V	--	5.8	--	ns
T <sub>r</sub>	Turn-on Rise Time		--	45	--	ns
T <sub>d(off)</sub>	Turn-Off Delay Time		--	16	--	ns
T <sub>f</sub>	Turn-Off Fall Time		--	7.6	--	ns
<b>Source- Drain Diode Characteristics @ T<sub>j</sub> = 25°C (unless otherwise stated)</b>						
V <sub>SD</sub>	Forward on voltage	I <sub>SD</sub> =20A, V <sub>GS</sub> =0V	--	0.9	1.2	V
T <sub>rr</sub>	Reverse Recovery Time	I <sub>sd</sub> =20A, V <sub>GS</sub> =0V	--	15	30	ns
Q <sub>rr</sub>	Reverse Recovery Charge	di/dt=100A/μs	--	3.5	7	nC

NOTE:

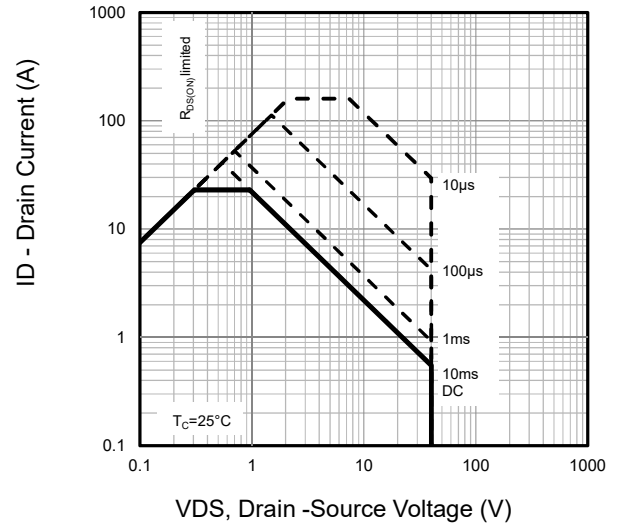
- ① Single pulse; pulse width ≤ 100μs.
- ② Limited by T<sub>Jmax</sub>, starting T<sub>J</sub> = 25°C, L = 0.5mH, R<sub>G</sub> = 25Ω, I<sub>AS</sub> = 8A, V<sub>GS</sub> = 10V. Part not recommended for use above this value
- ③ The power dissipation P<sub>DSM</sub> is based on R<sub>θJA</sub> and the maximum allowed junction temperature of 150°C.
- ④ Pulse width ≤ 380μs; duty cycle ≤ 2%.

**Typical Characteristics**

**Fig1.** Typical Output Characteristics

**Fig2.** Typical  $V_{GS(TH)}$  Gate-Source Voltage Vs.  $T_j$ 

**Fig3.** Typical Transfer Characteristics

**Fig4.** Typical Normalized On-Resistance Vs.  $T_j$ 

**Fig5.** Typical On Resistance Vs Gate-Source Voltage

**Fig6.** Typical On Resistance Vs Drain Current and Gate Voltage

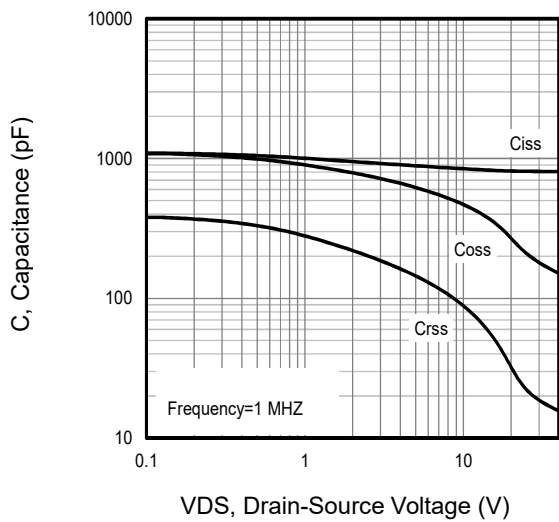
**Typical Characteristics**



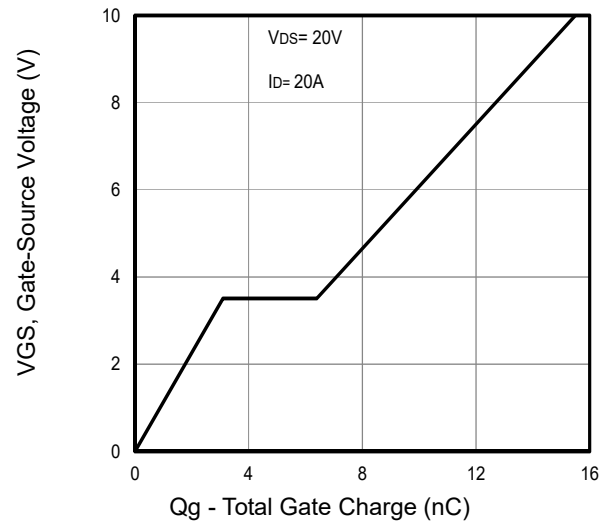
**Fig7.** Typical Source-Drain Diode Forward Voltage



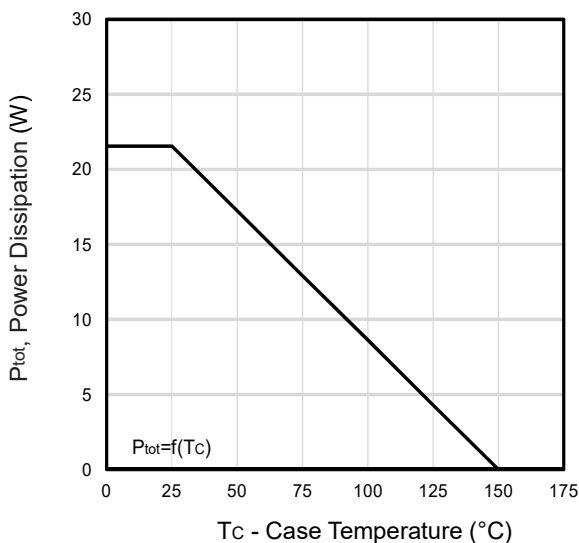
**Fig8.** Maximum Safe Operating Area



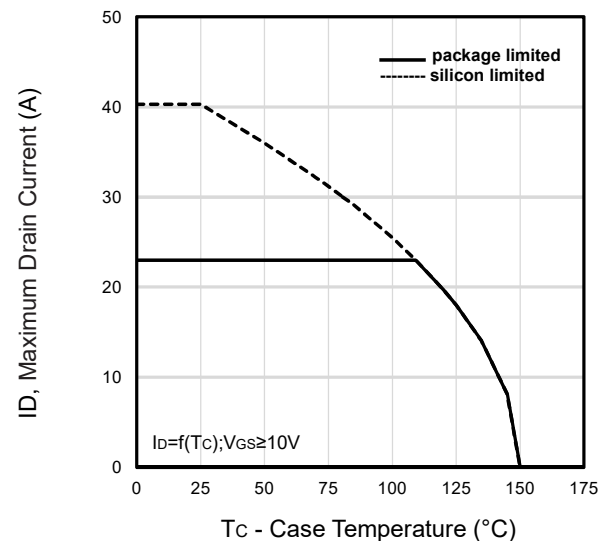
**Fig9.** Typical Capacitance Vs. Drain-Source Voltage



**Fig10.** Typical Gate Charge Vs. Gate-Source Voltage

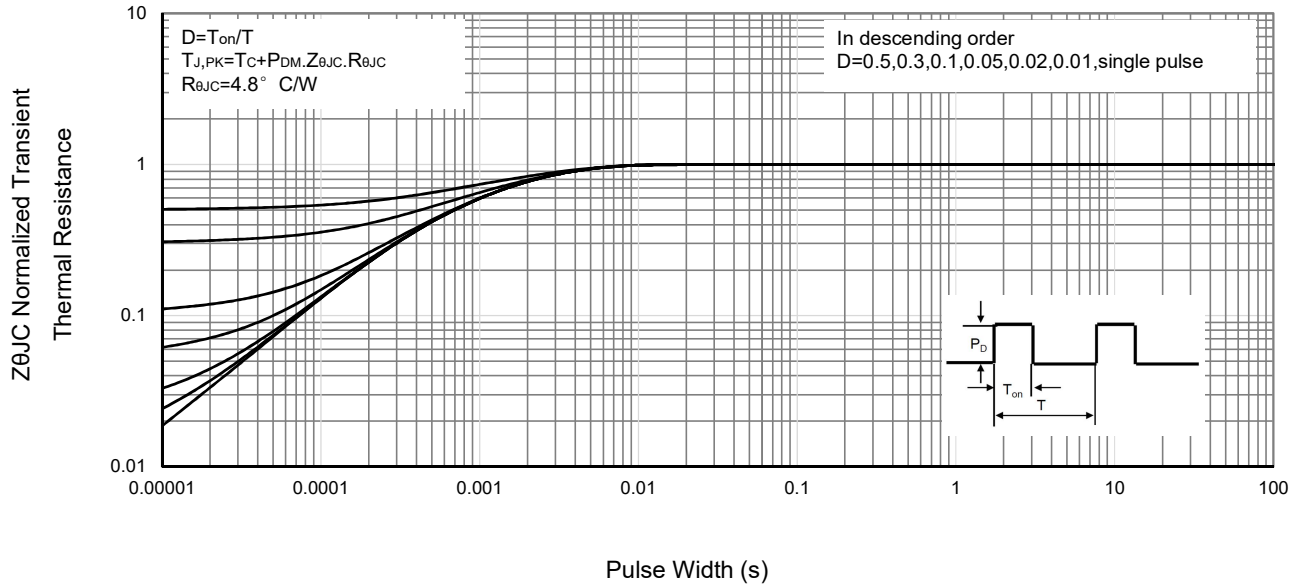


**Fig11.** Power Dissipation Vs. Case Temperature

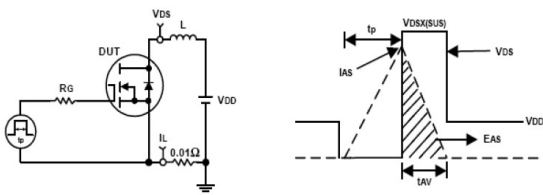


**Fig12.** Maximum Drain Current Vs. Case Temperature

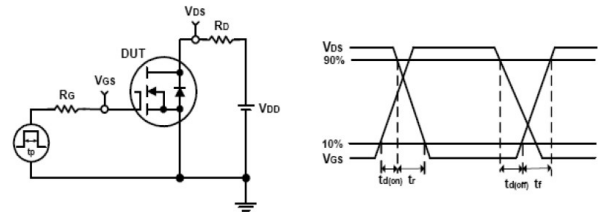
**Typical Characteristics**



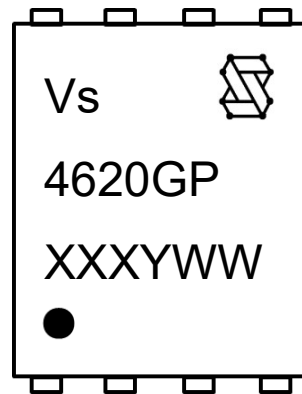
**Fig13 . Normalized Maximum Transient Thermal Impedance**



**Fig14. Unclamped Inductive Test Circuit and waveforms**



**Fig15. Switching Time Test Circuit and waveforms**

**Marking Information**


1st line: Vergiga Code (Vs), Vergiga Logo

2nd line: Part Number (4620GP)

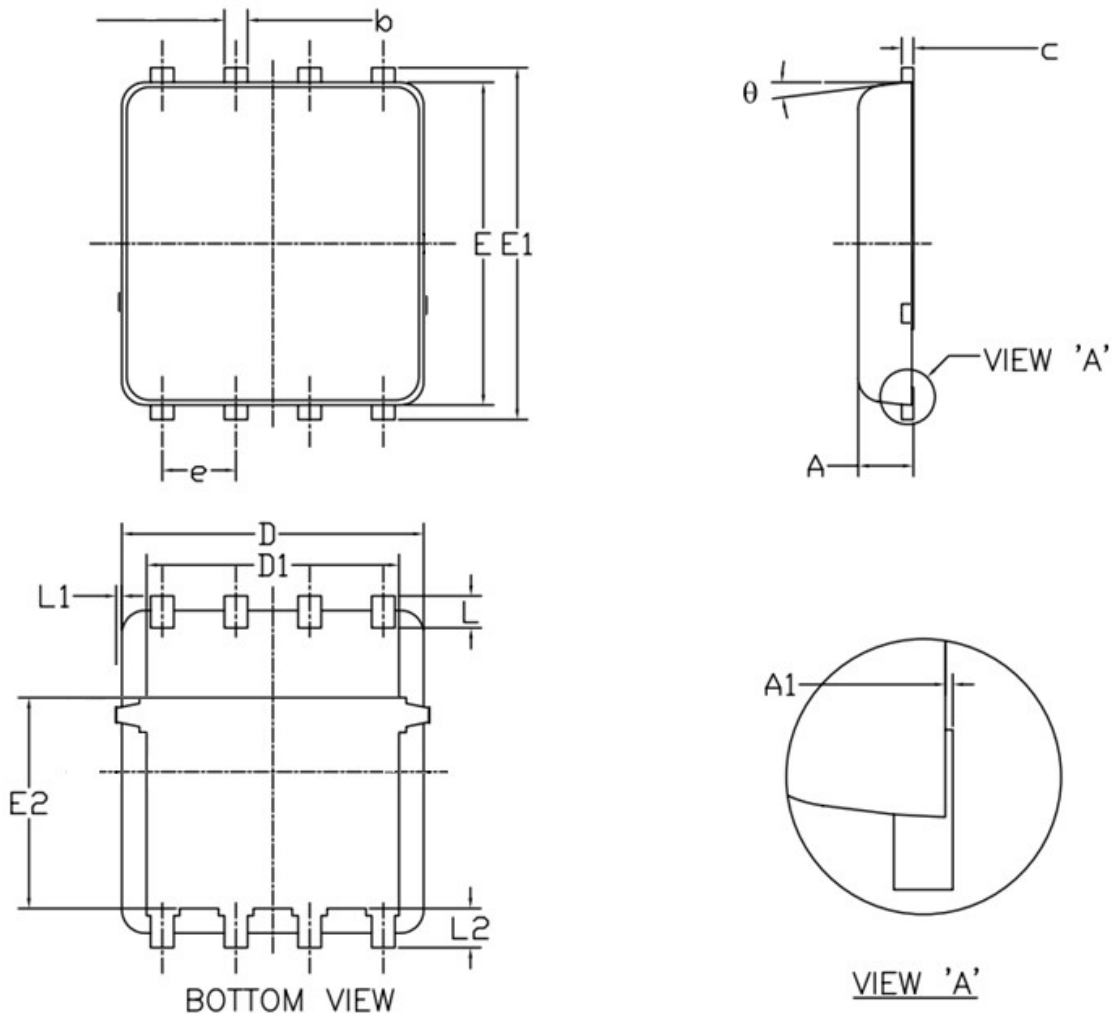
3rd line: Date code (XXXYYWW)

XXX: Wafer Lot Number Code, code changed with Lot Number

Y: Year Code, refer to table below

WW: Week Code (01 to 53)

Code	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T
Year	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030

**PDFN5x6 Package Outline Data**


Symbol	DIMENSIONS (unit : mm)		
	Min	Typ	Max
<b>A</b>	0.90	1.00	1.20
<b>A1</b>	0.00	--	0.05
<b>b</b>	0.30	0.40	0.51
<b>c</b>	0.20	0.25	0.33
<b>D</b>	4.80	4.90	5.40
<b>D1</b>	3.61	4.00	4.25
<b>E</b>	5.65	5.80	6.06
<b>E1</b>	5.90	6.10	6.35
<b>E2</b>	3.38	3.58	3.92
<b>e</b>	1.27 BSC		
<b>L</b>	0.51	0.61	0.71
<b>L1</b>	--	--	0.15
<b>L2</b>	0.41	0.51	0.61
<b><math>\theta</math></b>	0°	--	12°

**Notes:**

1. Refer to JEDEC MO-240 variation AA.
2. Dimensions "D" and "E" do NOT include mold flash protrusions or gate burrs.
3. Dimensions "D" and "E" include interterminal flash or protrusion. Interterminal flash or protrusion shall not exceed 0.25mm per side.

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