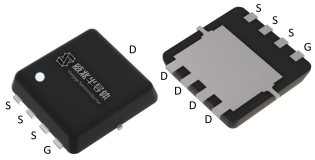
Features

- Enhancement mode
- VitoMOS® Ⅱ Technology
- Fast Switching and High efficiency
- 100% Avalanche test

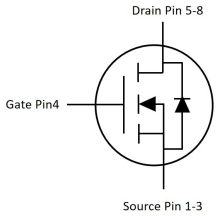
V_{DS}	40	V
$R_{DS(on),TYP}$@ V_{GS}=10 V	6.4	mΩ
$R_{DS(on),TYP}$@ V_{GS}=4.5 V	10	mΩ
$I_{D(Silicon\ Limited)}$	54	A
$I_{D(Package\ Limited)}$	36	A

PDFN3333



Pb-Free RoHS HF Halogen-Free

Part ID	Package Type	Marking	Packing
VS4620GEMC	PDFN3333	4620GE	5000PCS/Reel



Maximum ratings, at T_A =25°C, unless otherwise specified

Symbol	Parameter		Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage		40	V
V_{GS}	Gate-Source voltage		±20	V
I_S	Diode continuous forward current	T_C = 25°C	54	A
I_D	Continuous drain current @VGS=10V (Silicon limited)	T_C = 25°C	54	A
I_D	Continuous drain current @VGS=10V (Silicon limited)	T_C = 100°C	34	A
I_D	Continuous drain current @VGS=10V (Wire bond limited)	T_C = 25°C	36	A
I_{DM}	Pulse drain current tested ①	T_C = 25°C	150	A
I_{DSM}	Continuous drain current @VGS=10V	T_A = 25°C	19	A
		T_A = 70°C	15	A
EAS	Avalanche energy, single pulsed ②		16	mJ
P_D	Maximum power dissipation	T_C = 25°C	30	W
		T_C = 100°C	12	W
P_{DSM}	Maximum power dissipation ③	T_A = 25°C	3.6	W
		T_A = 70°C	2.3	W
T_{STG},T_J	Storage and Junction Temperature Range		-55 to 150	°C

Thermal Characteristics

Symbol	Parameter	Typical	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	4.2	5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	35	42	°C/W

Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_j=25°C (unless otherwise stated)						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	40	45	--	V
I_{DSS}	Zero Gate Voltage Drain Current(T_j=25℃)	V_{DS}=40V,V_{GS}=0V	--	--	1	μA
	Zero Gate Voltage Drain Current(T_j=125℃)	V_{DS}=40V,V_{GS}=0V	--	--	100	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=±20V,V_{DS}=0V	--	--	±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250μA	1.1	1.65	2.3	V
$R_{DS(on)}$	Drain-Source On-State Resistance ④	V_{GS}=10V, I_D=20A	--	6.4	8.3	mΩ
		(T_j=100℃)	--	7.8	--	mΩ
$R_{DS(on)}$	Drain-Source On-State Resistance ④	V_{GS}=4.5V, I_D=10A	--	10	13	mΩ
Dynamic Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
Ciss	Input Capacitance	V_{DS}=20V,V_{GS}=0V, f=1MHz	550	735	980	pF
Coss	Output Capacitance		215	285	380	pF
Crss	Reverse Transfer Capacitance		15	25	60	pF
Rg	Gate Resistance	f=1MHz	0.2	1.7	5	Ω
Qg(10V)	Total Gate Charge	V_{DS}=20V,I_D=20A, V_{GS}=10V	--	15	20	nC
Qg(4.5V)	Total Gate Charge		--	7.6	10	nC
Qgs	Gate-Source Charge		--	3	4	nC
Qgd	Gate-Drain Charge		--	3.3	5	nC
Switching Characteristics						
Td(on)	Turn-on Delay Time	V_{DD}=20V, I_D=20A, R_G=3Ω, V_{GS}=10V	--	5.6	--	ns
Tr	Turn-on Rise Time		--	47	--	ns
Td(off)	Turn-Off Delay Time		--	15	--	ns
Tf	Turn-Off Fall Time		--	6.4	--	ns
Source- Drain Diode Characteristics@ T_j = 25°C (unless otherwise stated)						
V_{SD}	Forward on voltage	I_{SD}=20A,V_{GS}=0V	--	0.9	1.2	V
Trr	Reverse Recovery Time	I_{sd}=20A, V_{GS}=0V di/dt=100A/μs	--	6.1	12	ns
Qrr	Reverse Recovery Charge		--	0.6	1.2	nC

NOTE: ① Single pulse; pulse width ≤ 100μs.

② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.5mH, R_G = 25Ω, I_{AS} = 8A, V_{GS} =10V. Part not recommended for use above this value

③ The power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C.

④ Pulse width ≤ 380μs; duty cycle≤ 2%.

Typical Characteristics

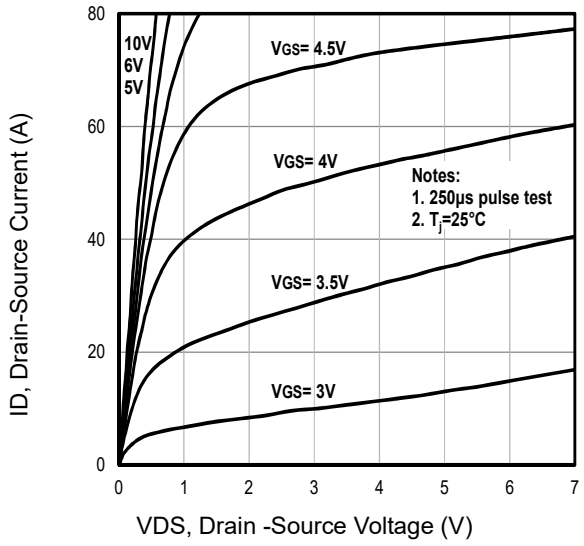


Fig1. Typical Output Characteristics

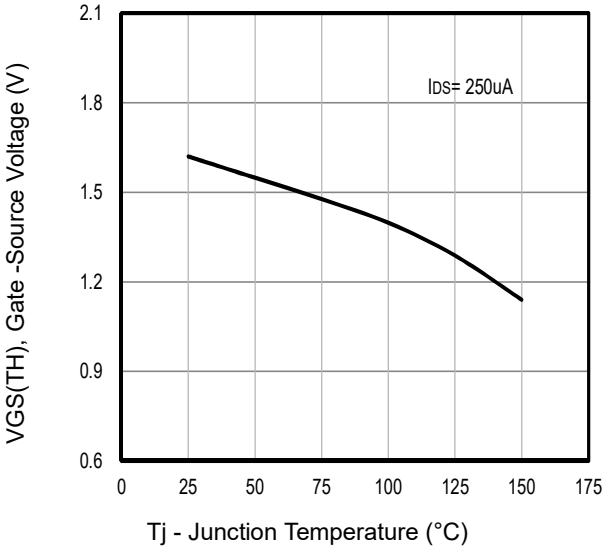


Fig2. $V_{GS(TH)}$ Gate -Source Voltage Vs. Tj

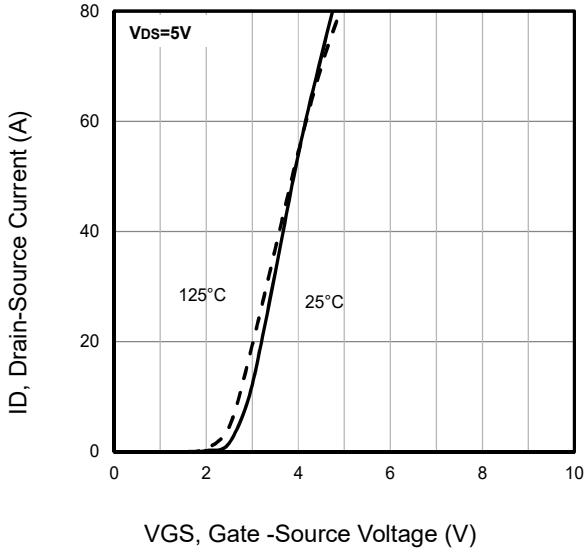


Fig3. Typical Transfer Characteristics

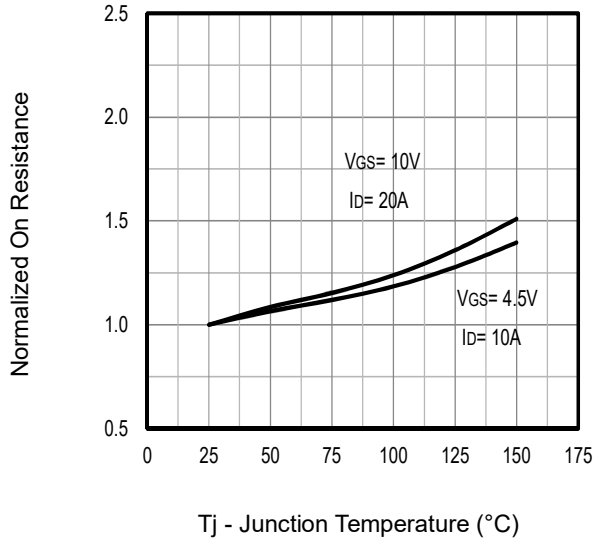


Fig4. Normalized On-Resistance Vs. Tj

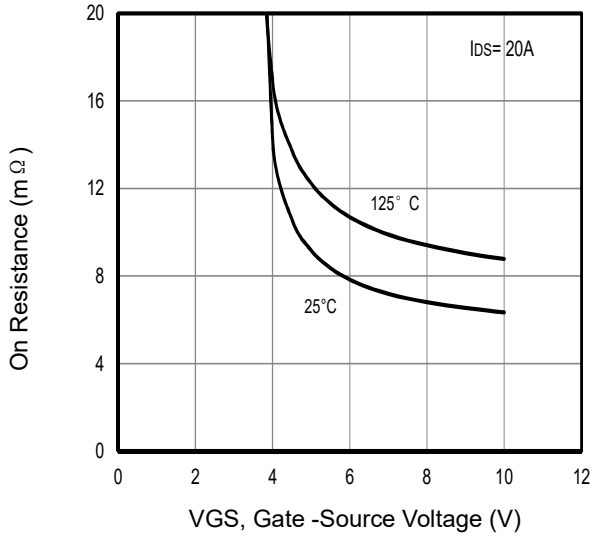


Fig5. On Resistance Vs Gate -Source Voltage

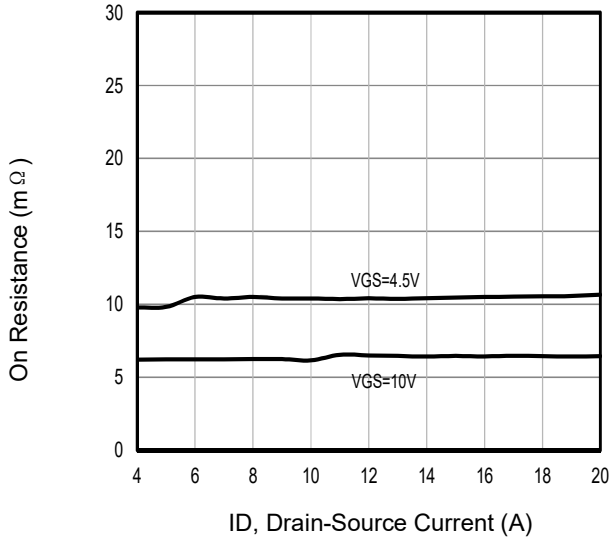


Fig6. On Resistance Vs Drain Current and Gate Voltage

Typical Characteristics

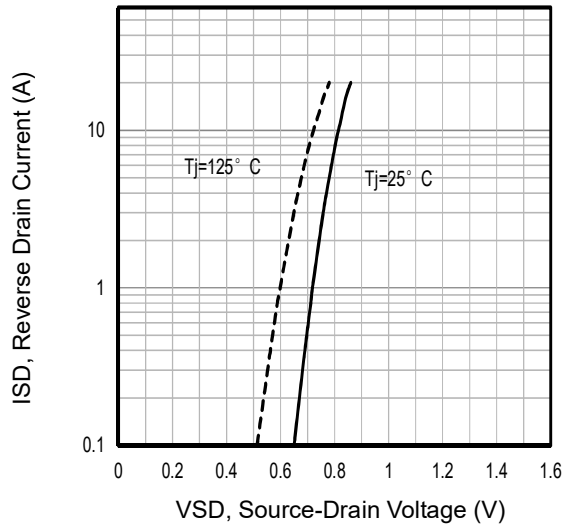


Fig7. Typical Source-Drain Diode Forward Voltage

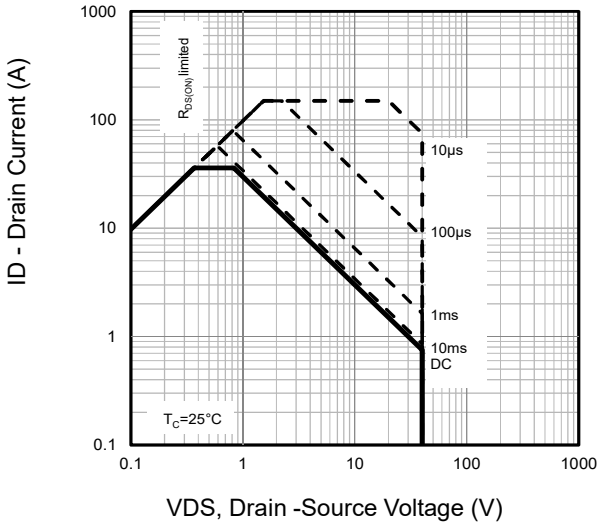


Fig8. Maximum Safe Operating Area

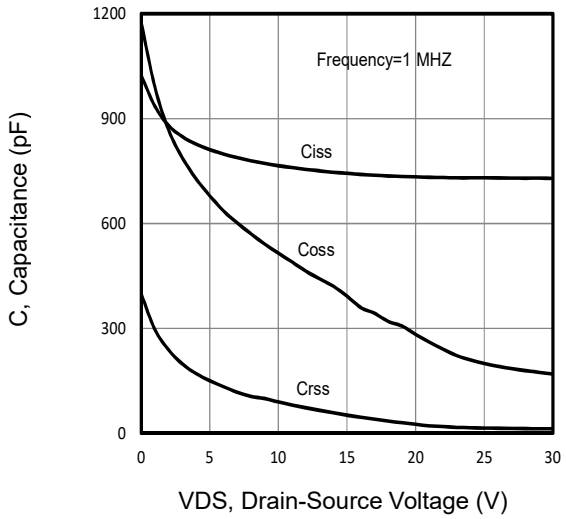


Fig9. Typical Capacitance Vs. Drain-Source Voltage

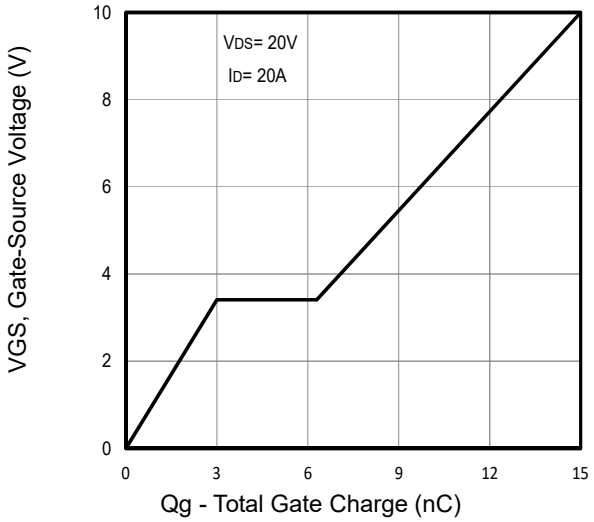


Fig10. Typical Gate Charge Vs. Gate-Source Voltage

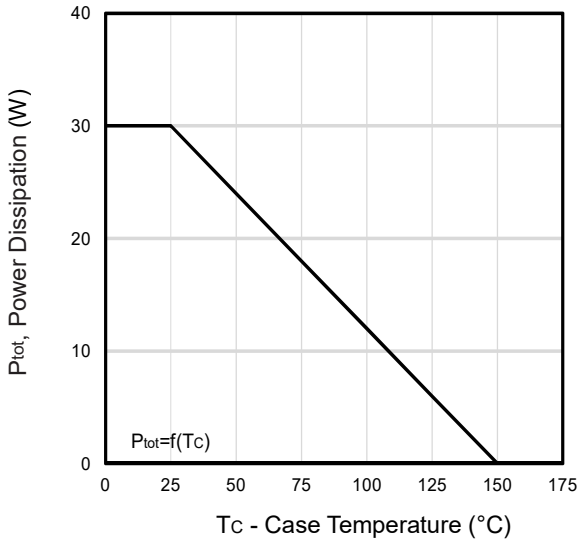


Fig11. Power Dissipation Vs. Case Temperature

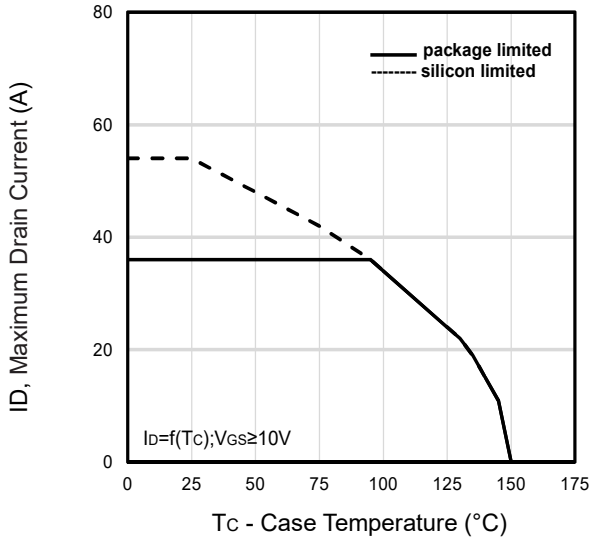


Fig12. Maximum Drain Current Vs. Case Temperature

Typical Characteristics

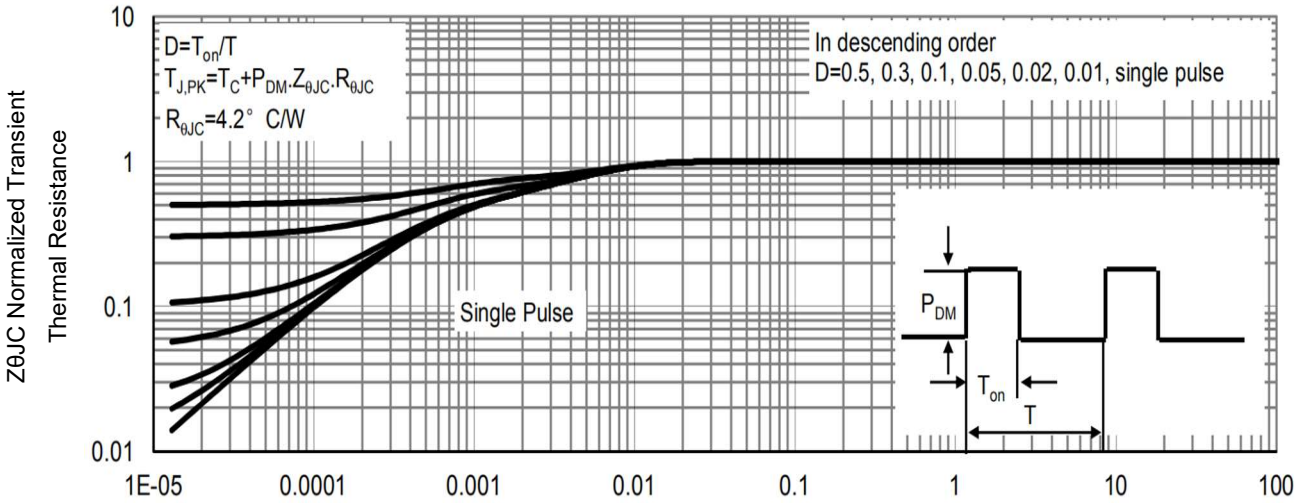


Fig13 . Normalized Maximum Transient Thermal Impedance

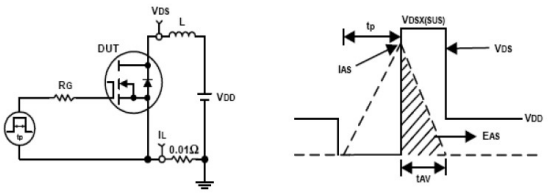


Fig14. Unclamped Inductive Test Circuit and waveforms

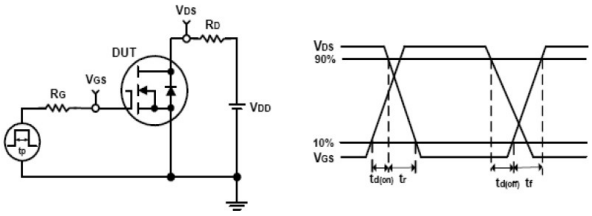
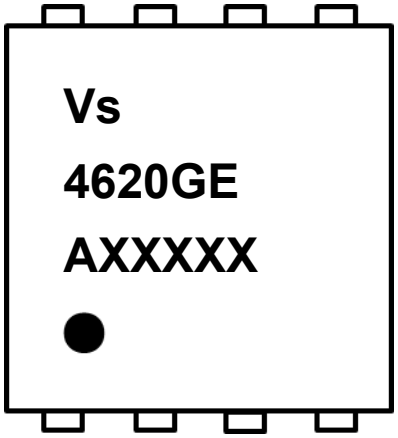


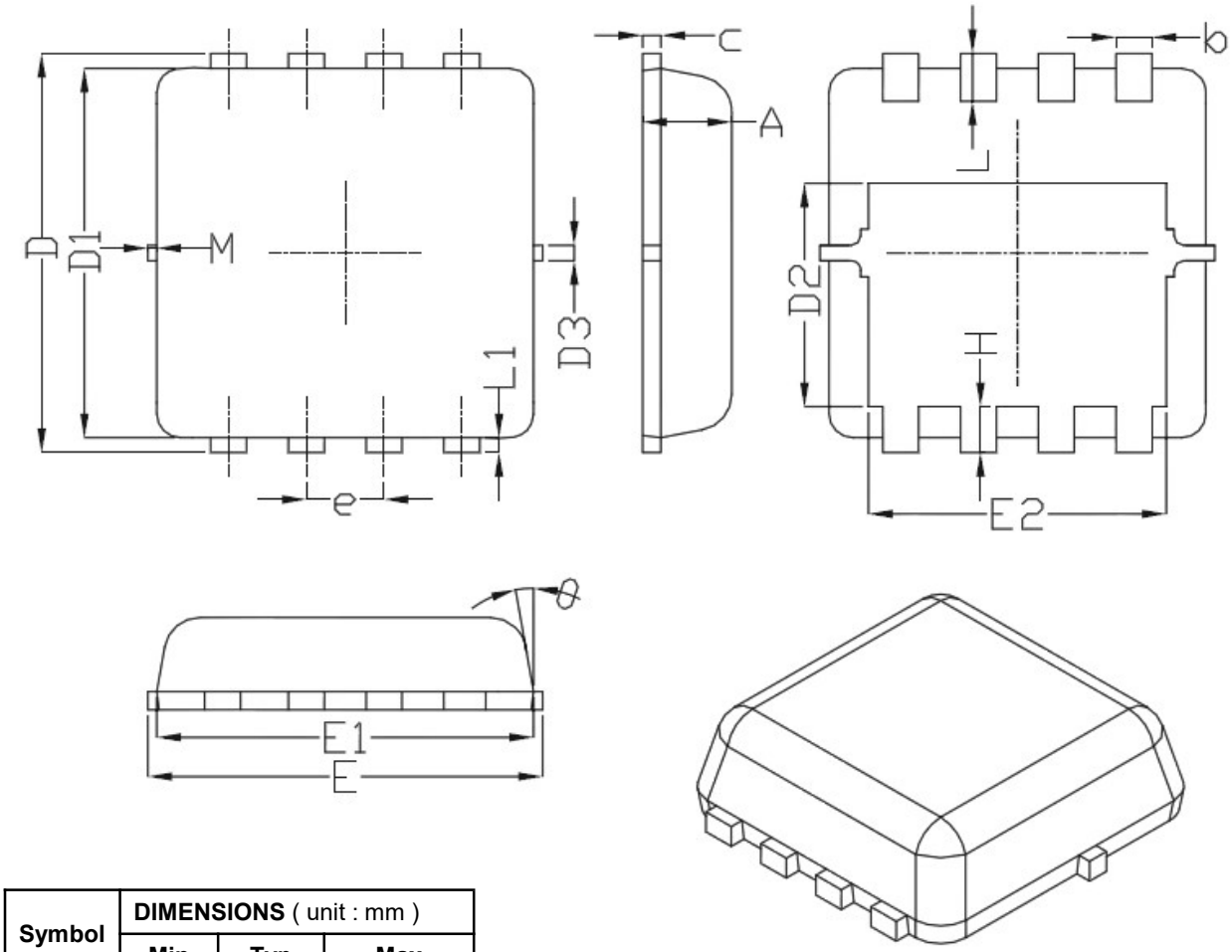
Fig15. Switching Time Test Circuit and waveforms

Marking Information



1st line: Vergiga Code（Vs）
2nd line: Part Number（4620GE）
3rd line: Date code （AXXXXX）
A: Manufacturer Factory Code
XXXXX: Wafer Lot Tracibility Code

PDFN3333 Package Outline Data



Symbol	DIMENSIONS (unit : mm)		
	Min	Typ	Max
A	0.7	0.75	0.8
b	0.25	0.3	0.35
C	0.1	0.15	0.25
D	3.25	3.35	3.45
D1	3	3.1	3.2
D2	1.78	1.88	1.98
D3	--	0.13	--
E	3.2	3.3	3.4
E1	3	3.15	3.2
E2	2.39	2.49	2.59
e	0.65 BSC		
H	0.3	0.39	0.5
L	0.3	0.4	0.5
L1	--	0.13	--
θ	--	10°	12°
M	*	*	0.15
* Not specified			

Notes:

1. Follow JEDEC MO-240 variation CA.
2. Dimensions "D1" and "E1" do NOT include mold flash protrusions or gate burrs.
3. Dimensions "D1" and "E1" include interterminal flash or protrusion. Interterminal flash or protrusion shall not exceed 0.25mm per side.

Customer Service

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