Si4356 Standalone Sub-GHz Receiver

Features

- Pin configurable
- Frequency range = 315–917 MHz
- Supply Voltage = 1.8–3.6 V
- Receive sensitivity = Up to –113 dBm
- Modulation
  - (G)FSK
  - OOK
- Low RX Current = 12 mA
- Low standby current = 50 nA
- Max data rate = 120 kbps
- Automatic gain control (AGC)
- System clock output
- Low BOM
- 20-pin 3x3 mm QFN package

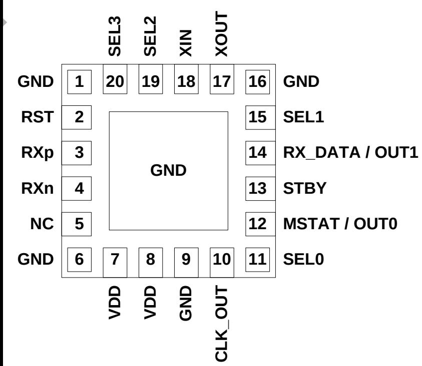
Applications

- Remote control
- Home security and alarm
- Garage and gate openers
- Remote keyless entry
- Home automation
- Industrial control
- Sensor networks
- Health monitors

Description

Silicon Laboratories' Si4356 is a pin-strap configurable, low current, sub-GHz EZRadio® receiver. With no external MCU control needed, the Si4356 provides a true plug-and-play receive option. Excellent sensitivity up to –113 dBm allows for a longer operating range, while the low current consumption of 12 mA active and 50 nA standby provides for superior battery life. The Si4356 provides receive data as well as a system clock output for use by an external microcontroller or decoder.

Pin Assignments



20-pin QFN
(Top View)

Patents pending

Functional Block Diagram

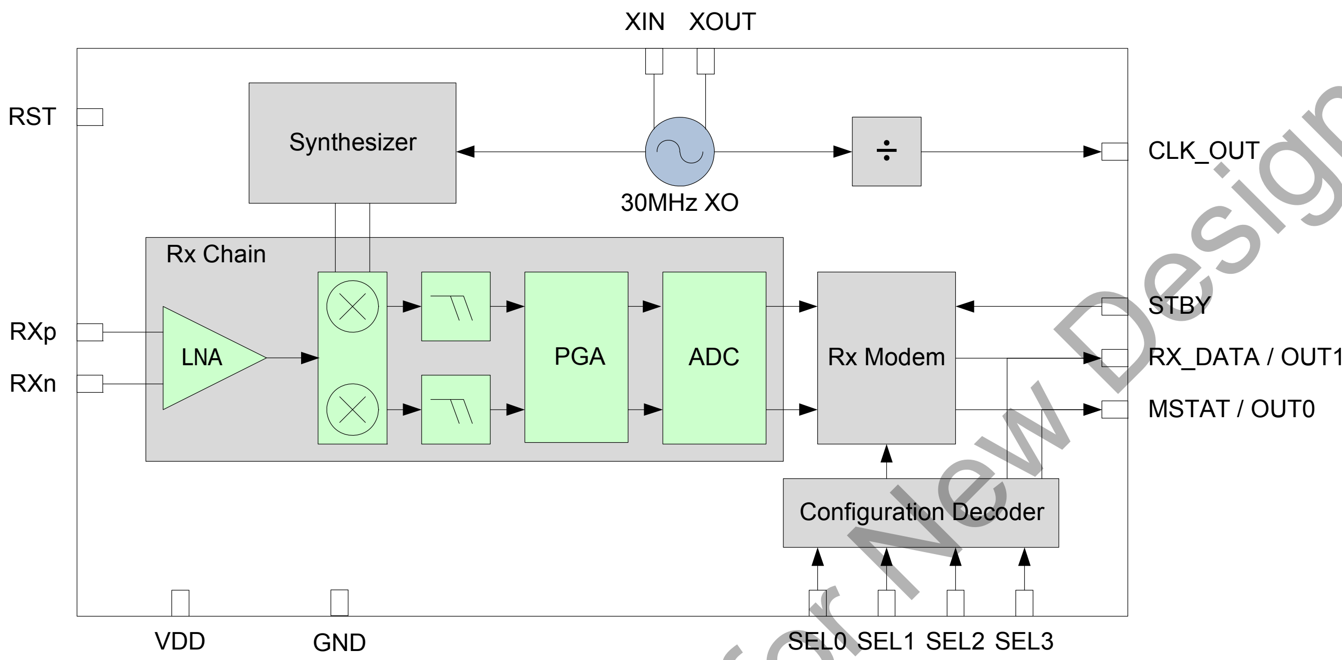


TABLE OF CONTENTS

Section **Page**

1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Temperature	T_A	—	–40	25	85	°C
Supply Voltage	V_{DD}	—	1.8	—	3.6	V
I/O Drive Voltage	V_{GPIO}	—	1.8	—	3.6	V

Table 2. DC Characteristics*

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Standby Mode Current	$I_{Standby}$	Configuration retained, all other functions OFF	—	50	—	nA
RX Mode Current	I_{RX}	—	—	12	—	mA

***Note:** All specifications guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in the "Production Test Conditions" section of "1.1. Definition of Test Conditions" on page 8.

Table 3. Receiver Electrical Characteristics[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency Range	F_{RANGE}	Only frequencies listed in Table 9 supported	315	—	917	MHz
Sensitivity[2]	P_{FSK}	BER < 0.1%, 2.4 kbps, (G)FSK, Configuration = FSK1 (See Section 3.)	—	–113	—	dBm
	P_{FSK}	BER < 0.1%, 2.4 kbps, (G)FSK, Configuration = FSK6 (See Section 3.)		–104		dBm
	P_{OOK}	BER < 0.1%, 2.4 kbps, OOK, Configuration = OOK6 (See Section 3.)	—	–111	—	dBm
RX Channel Bandwidth[3]	BW	—	100	—	535	kHz
BER Variation vs Power Level[3]	P_{RX_RES}	Up to +5 dBm Input Level	—	0	0.1	ppm

Notes:
1. Test conditions and max limits are listed in section “1.1. Definition of Test Conditions”.
2. Sensitivity measured at 434 MHz using a PN9 modulated input signal. Received signal is filtered, deglitched, and retimed using an external RC filter (R = 1 kΩ, C = 47 nF) and MCU.
3. Guaranteed by qualification. Qualification test conditions are listed in section “1.1. Definition of Test Conditions”.

Table 3. Receiver Electrical Characteristics[1] (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
±200 kHz Selectivity[3]	$C/I_{1\text{-}CH}$	Desired Ref Signal 3 dB above sensitivity, BER < 0.1%. Interferer is CW and desired modulated with 2.4 kbps ΔF = 30 kHz (G)FSK, BT = 0.5, Rx BW = 155 kHz,	—	–42	—	dB
±400 kHz Selectivity[3]	$C/I_{2\text{-}CH}$		—	–50	—	dB
Blocking 1 MHz Offset[3]	—	Desired Ref Signal 3 dB above sensitivity, BER < 0.1% Interferer is CW and desired modulated with 2.4 kbps ΔF = 30 kHz (G)FSK, BT = 0.5, RX BW = 155 kHz	—	–57	—	dB
Blocking 8 MHz Offset[3]	—		—	–68	—	dB
Image Rejection[3]	Im_{REJ}	IF = 468 kHz	—	–35	—	dB
Spurious Emissions[3]	P_{OB_RX1}	Measured at RX pins	—	—	–54	dBm

Notes:
1. Test conditions and max limits are listed in section “1.1. Definition of Test Conditions”.
2. Sensitivity measured at 434 MHz using a PN9 modulated input signal. Received signal is filtered, deglitched, and retimed using an external RC filter (R = 1 kΩ, C = 47 nF) and MCU.
3. Guaranteed by qualification. Qualification test conditions are listed in section “1.1. Definition of Test Conditions”.

Table 4. Auxiliary Block Specifications[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
XTAL Nominal Cap[3]	—	—	—	10	—	pF
XTAL Frequency	—	—	—	30	—	MHz
XTAL Series Resistance	—	—	—	—	50	Ω
XTAL Stability	—	—	—	±50	—	ppm
Reset to RX Time[2]	t_{RST}	—	—	—	20	ms

Notes:
1. Test conditions and max limits are listed in section in “1.1. Definition of Test Conditions”.
2. Guaranteed by qualification. Qualification test conditions are listed in the "Qualification Test Conditions" subsection of section “1.1. Definition of Test Conditions”.
3. Targeted nominal capacitive load for both XIN and XOUT pins.

Table 5. Digital I/O Specifications (STBY, RX_DATA, MSTAT, CLK_OUT)[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Rise Time	T_{RISE}	$0.1xV_{DD}$ to $0.9xV_{DD}$, C_L=10pF, DRV<1:0≥HH	—	2.3	—	ns
Fall Time	T_{FALL}	$0.9xV_{DD}$ to $0.1xV_{DD}$, C_L=10pF, DRV<1:0≥HH	—	2.0	—	ns
Input Capacitance	C_{IN}	—	–	2	—	pF
Logic High Level Input Voltage	V_{IH}	—	V_{DD}x0.7	–	—	V
Logic Low Level Input Voltage	V_{IL}	—	—	—	V_{DD}x0.3	V
Input Current (STBY)[2]	I_{IN}	$0<V_{IN}<V_{DD}$	–10	—	10	µA
Input Current (STBY)[2]	I_{INP}	V_{IL} = 0 V	1	—	10	µA
Drive Strength for Output Low Level[2, 3]	I_{OL}	RX_DATA, MSTAT, CLK_OUT	—	1.13	—	mA
Drive Strength for Output High Level[2, 3]	I_{OH}	RX_DATA, MSTAT	—	0.96	—	mA
Drive Strength for Output High Level[2, 3]	I_{OH}	CLK_OUT	—	0.80	—	mA
Logic High Level Output Voltage	V_{OH}	I_{OUT} = 500 µA	V_{DD}x0.8	–	—	V
Logic Low Level Output Voltage	V_{OL}	I_{OUT} = 500 µA	—	—	V_{DD}x0.2	V
CLK_OUT Frequency	F_{CLK}	Rx Freq = 315 MHZ	—	10	—	MHz
		All other frequencies	—	15	—	MHz
CLK_OUT Duty Cycle	—	—	—	50	—	%

Notes:
1. Guaranteed by qualification. Qualification test conditions are listed in Section “1.1. Definition of Test Conditions”.
2. Currents listed are during normal operation after power up sequence is complete.
3. Output currents measured at 3.3 VDC V_{DD} with V_{OH} = 2.64 VDC and V_{OL} = 0.66 VDC.

Table 6. Thermal Characteristics

Parameter	Symbol	Test Condition	Value	Unit
Thermal Resistance Junction to Ambient	Θ_{JA}	Still Air	30	°C/W

Table 7. Absolute Maximum Ratings

Parameter	Value	Unit
V_{DD} to GND	–0.3 to +3.6	V
Voltage on Digital Control Inputs	–0.3 to V_{DD} + 0.3	V
Voltage on Analog Inputs	–0.3 to V_{DD} + 0.3	V
RX Input Power	+10	dBm
Operating Ambient Temperature Range T_A	–40 to +85	°C
Storage Temperature Range T_{STG}	–55 to +125	°C

Note: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at or beyond these ratings in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Caution: ESD sensitive device.

1.1. Definition of Test Conditions

Production Test Conditions:

- T_A = +25 °C
- V_{DD} = +3.3 VDC
- External reference signal (XIN) = 1.0 V_{PP} at 30 MHz, centered around 0.8 VDC
- Production test schematic (unless noted otherwise)
- All RF input levels referred to the pins of the Si4356 (not the RF module)

Qualification Test Conditions:

- T_A = –40 to +85 °C (typical = 25 °C)
- V_{DD} = +1.8 to +3.6 VDC (typical = 3.3 VDC)
- Using reference design or production test schematic
- All RF input levels are referred to the antenna port of Si4356 reference design or to the pins of the Si4356 when the production test setup is used.

2. Typical Applications Circuit

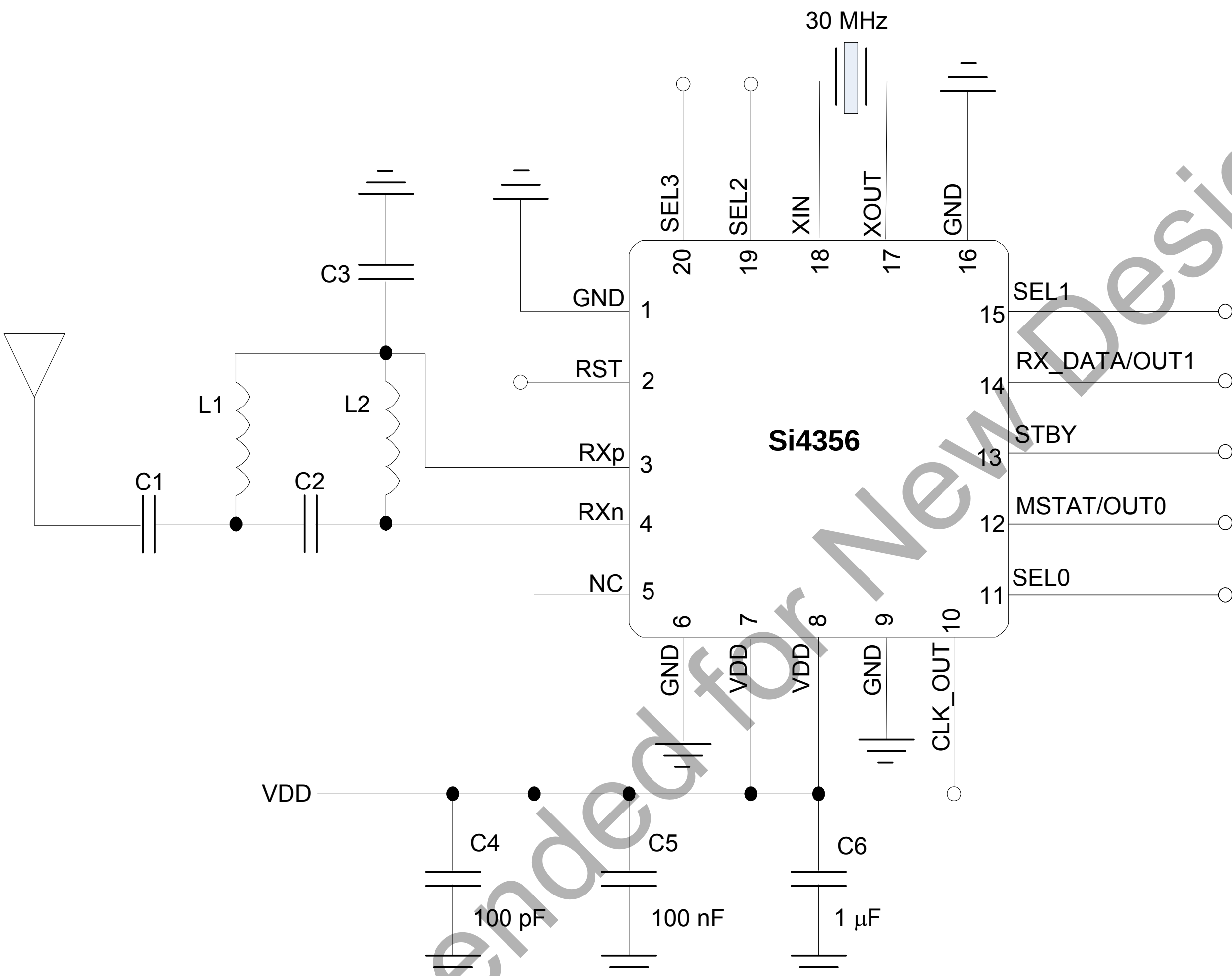


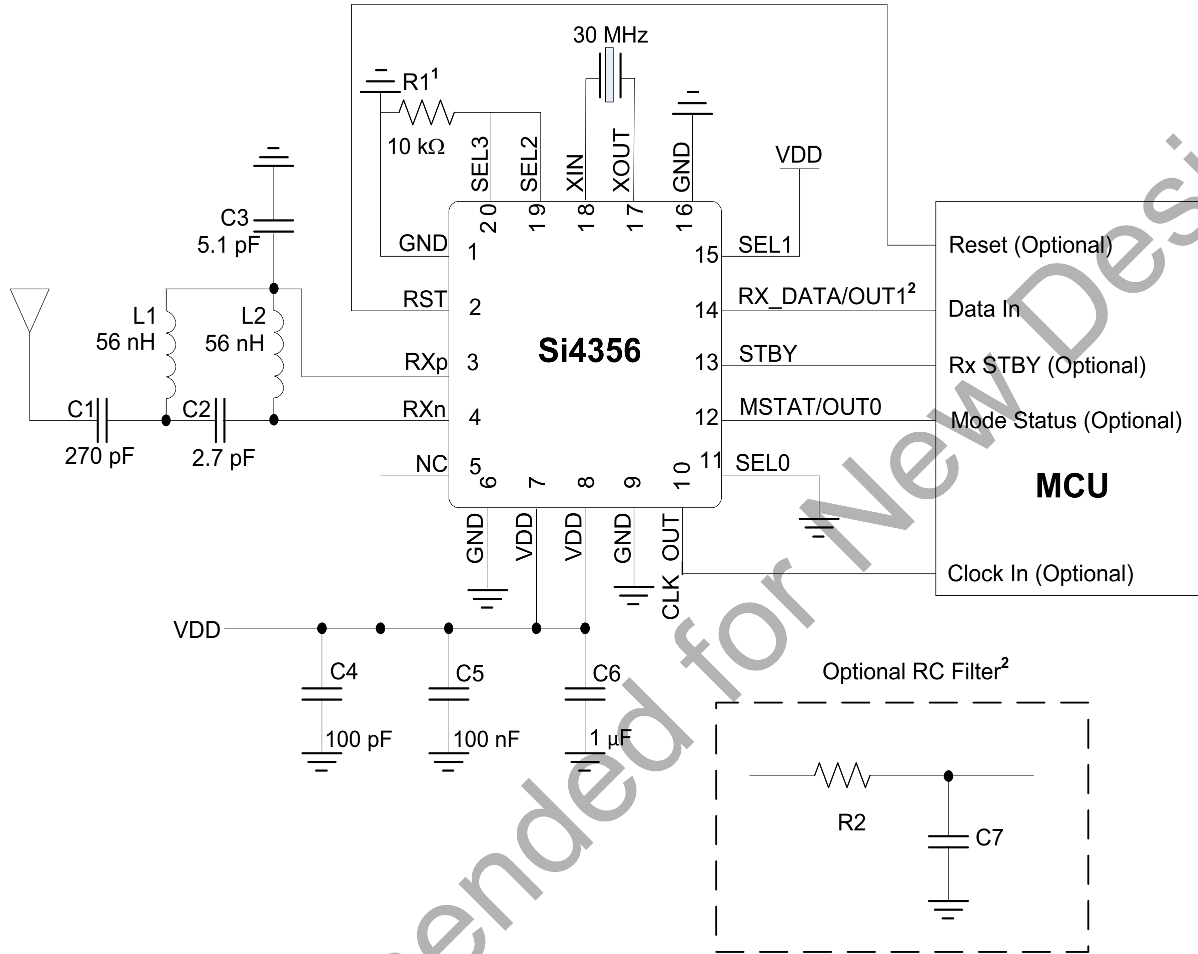
Figure 1. Si4356 Applications Circuit

Table 8. Si4356 Recommended Matching Values

Frequency (MHz)	C1 (pF)	C2 (pF)	C3 (pF)	L1 (nH)	L2 (nH)
433.92	270	2.7	5.1	56	56
315.00	470	3.0	6.2	82	100
434.15	270	2.7	5.1	56	56
867.84	68	1.2	3.0	22	18
868.30	56	1.2	3.0	22	18
917.00	56	1.0	3.0	22	18

Note: Multi-layer inductors and ceramic chip capacitors with tolerance of ±5% are recommended.

Figure 2 shows the application circuit for a particular radio configuration (433.92 MHz, OOK, 2 kbps, 206 kHz RxBW) with all optional connections. See Sections 5 and 7 for Si4356 pin functionality.



Note:

1. R1 is required to minimize power up current. R1 is only necessary for pin configurations where SEL2 or SEL3 is mapped to GND.
2. An optional external low-pass RC filter may be connected to RX_DATA to filter the output and improve sensitivity. R2 and C7 should be selected to realize a cut-off frequency that is ~40% larger than that targeted data rate according to $f_c = 1/(2\pi RC)$.

Figure 2. Si4356 Application Circuit Example

3. Device Configuration

The Si4356 is configured for operation using the four configuration selector pins (SEL0 – SEL3). These pins will be connected to one of four possible inputs: GND, VDD, RX DATA/OUT1 (pin 14), or OUT0 (pin 12). Refer to the tables below for how these pins should be connected for the desired configuration.

SEL0 and SEL1 may be connected to VDD, GND, or OUT1 to choose desired frequency. Note that a 10 kΩ resistor should be inserted between SEL1 and OUT1 when SEL1 is mapped to OUT1. See Table 9 for frequency settings.

Table 9. Frequency Selection

SEL0	SEL1	Frequency (MHz)
GND	VDD	433.92
VDD	VDD	315.00
OUT1	VDD	434.15
GND	OUT1	867.84
VDD	OUT1	868.30
OUT1	OUT1	917.00

SEL2 and SEL3 may be connected to VDD, GND, or OUT1 to choose desired modem configuration. See Table 10 for basic configurations. Note that a 10 kΩ resistor should inserted between SEL2 and/or SEL3 and GND when SEL2 and/or SEL3 are mapped to GND.

Table 10. Basic Configuration

Config. Name	SEL2	SEL3	Mod	Data Rate (kbps)	RxBW (kHz)	Squelch	Recommended F_{DEV} (kHz)
OOK1	GND	GND	OOK	0.5–5	206	Disabled	—
OOK2	VDD	GND	OOK	1–10	370	Disabled	—
OOK3	OUT1	GND	OOK	10–50	370	Disabled	—
OOK4	OUT0	GND	OOK	50–120	370	Disabled	—
OOK5	GND	VDD	OOK	50–120	535	Disabled	—
OOK6	VDD	VDD	OOK	0.5–2.4	100	Disabled	—
FSK1	GND	OUT1	(G)FSK	0.5–30	155	Disabled	30
FSK2	VDD	OUT1	(G)FSK	0.5–30	185	Disabled	70
FSK3	OUT1	OUT1	(G)FSK	0.5–30	275	Disabled	30
FSK4	OUT0	OUT1	(G)FSK	10–120	275	Disabled	70
FSK5	GND	OUT0	(G)FSK	10–120	535	Disabled	70
FSK6	VDD	OUT0	(G)FSK	0.5–2.4	155	Enabled	30
FSK7	OUT1	OUT0	(G)FSK	0.5–2.4	275	Enabled	30

To disable the system clock, connect CLK_OUT to OUT0. Otherwise, CLK_OUT is enabled. See Table 11 settings.

Table 11. System Clock

CLK_OUT (Pin 10)	Clock Output
OUT0	OFF
X	ON

4. Functional Description

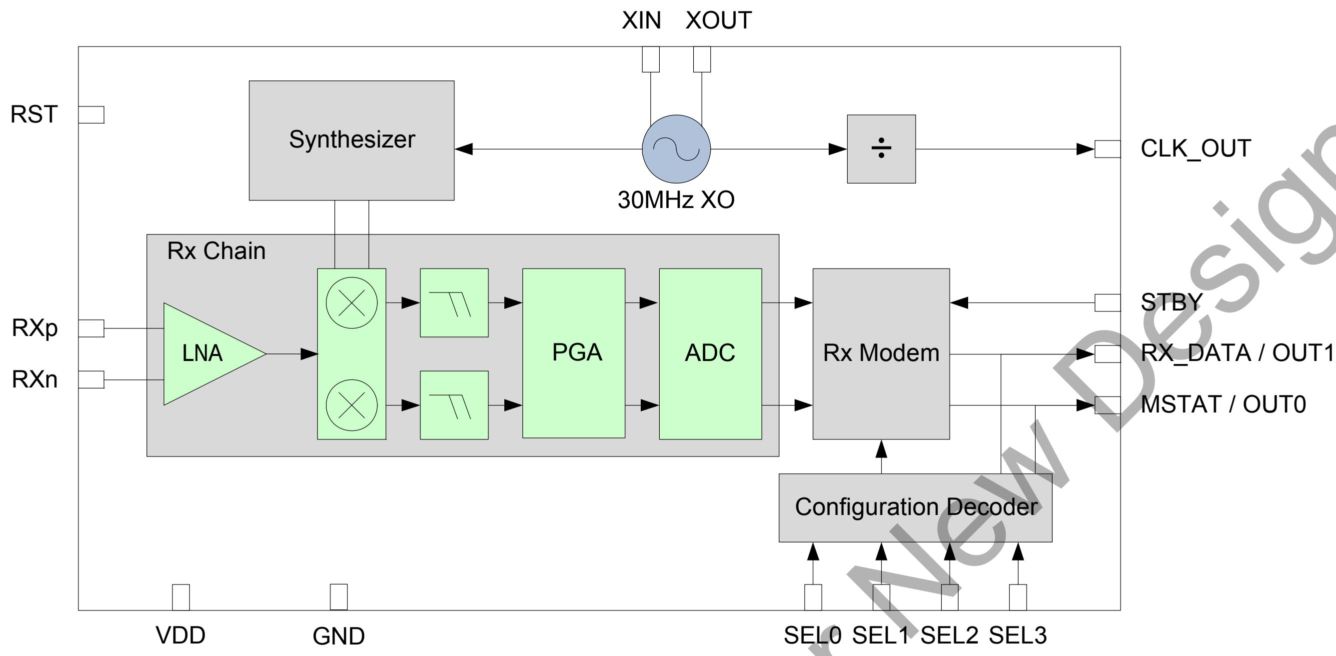


Figure 3. Si4356 Functional Block Diagram

The Si4356 is an easy-to-use, size efficient, low current wireless receiver that covers the sub-GHz bands. The wide operating voltage range of 1.8–3.6 V and low current consumption make the Si4356 an ideal solution for battery powered applications. The Si4356 uses a single-conversion mixer to downconvert the (G)FSK or OOK modulated receive signal to a low IF frequency. Following a programmable gain amplifier (PGA), the signal is converted to the digital domain by a high performance $\Delta\Sigma$ ADC, thus allowing filtering and demodulation to be performed in the built-in DSP and increasing the receiver's performance and flexibility versus analog based architectures. The receiver demodulates the incoming data asynchronously by oversampling the incoming transmission. The resulting demodulated signal is output to the system MCU through data output pin RX_DATA.

Integrated configuration tables allow the Si4356 to be completely configured using the four selector pins. The state of each of these pins is read internally at startup and used to determine which pre-loaded configuration should be used. The Si4356 then loads this configuration without the need for any external MCU control.

The Si4356 includes an integrated crystal oscillator. The design is differential with the typical crystal load capacitance integrated on-chip to accommodate a 30 MHz off-chip crystal.

5. Modes and Timing

At initial startup, the Si4356 reads the selector pins and loads all registers with the appropriate values for the selected configuration, as shown in the Figure 4.

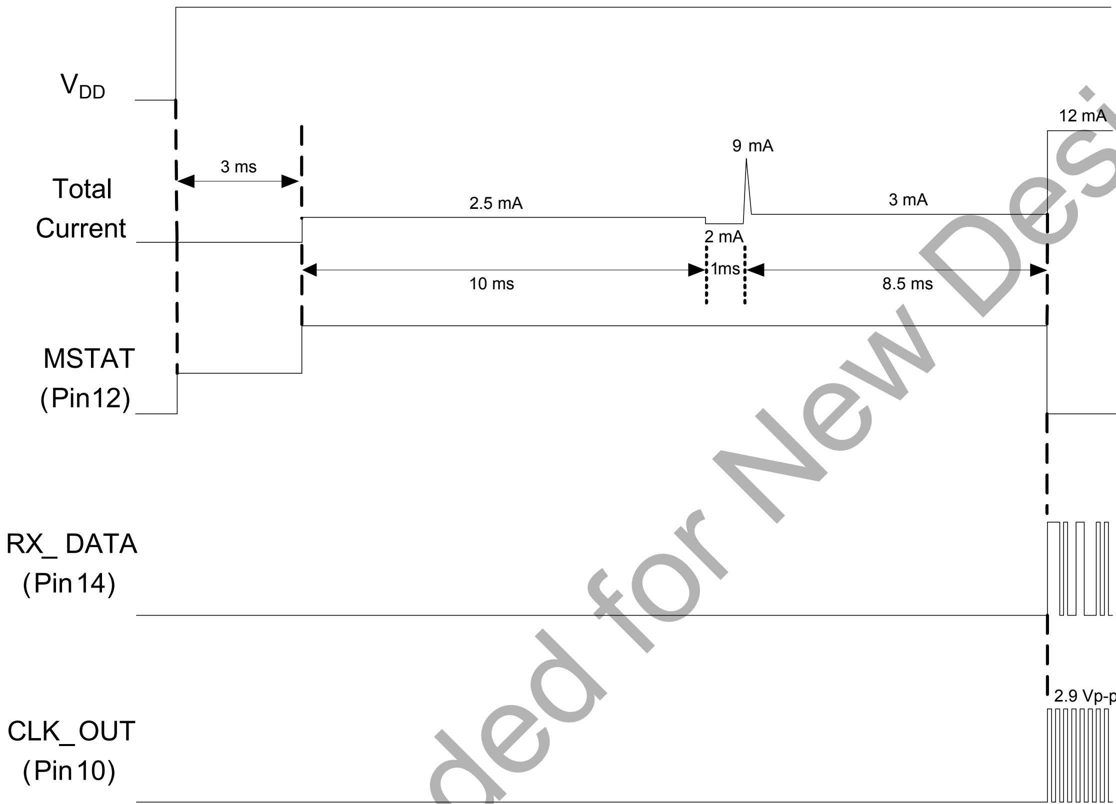


Figure 4. Power Up Timing

5.1. Power on Reset (POR)

A Power On Reset (POR) sequence is used to boot the device up from a fully off or shutdown state. To execute this process, VDD must ramp within 1ms and must remain applied to the device for at least 10 ms. If VDD is removed, then it must stay below 0.15 V for at least 10 ms before being applied again. See Figure 5 and Table 12 for details.

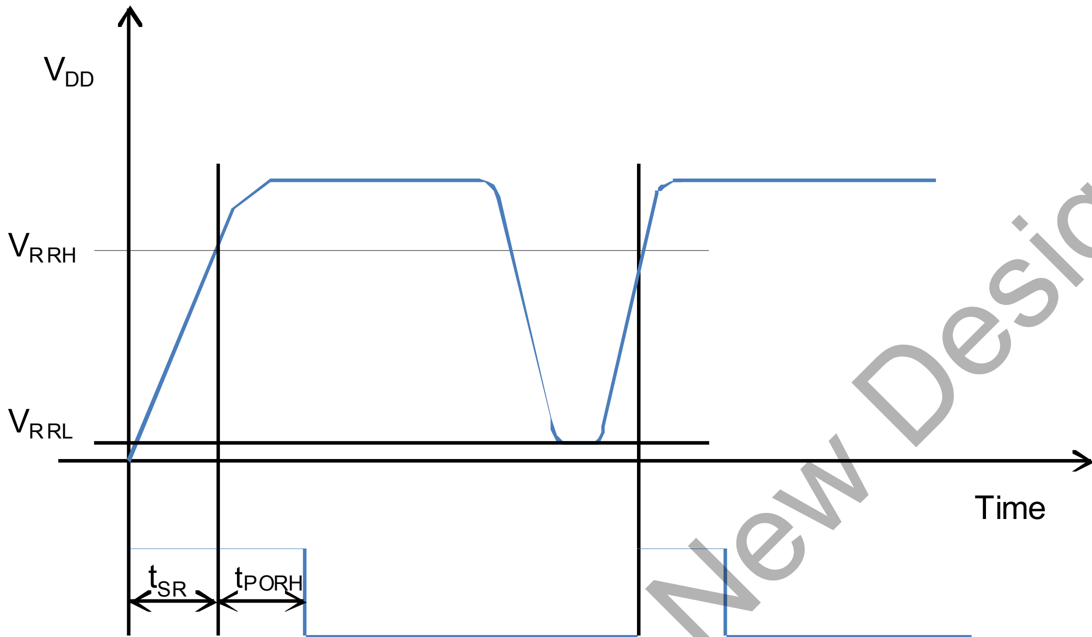


Figure 5. POR Timing Diagram

Table 12. POR Timing

Variable	Description	Min	Typ	Max	Units
t_{PORH}	High time for VDD to fully settle POR circuit	10			ms
t_{PORL}	Low time for VDD to enable POR	10			ms
V_{RRH}	Voltage for successful POR	90% x Vdd			V
V_{RRL}	Starting Voltage for successful POR	0		150	mV
t_{SR}	Slew rate of VDD for successful POR			1	ms

The Si4356 provides two operating modes, a receive mode and a standby mode. The operating mode can be changed by toggling STBY (pin 13) as described in Figure 6. Care should be taken to minimize the trace connected to STBY to avoid external noise coupling that could result in unintended mode changes. The MSTAT signal (pin 12) indicates the current operating mode of the device as defined in Table 13 and illustrated in Figure 6.

Table 13. Operating Mode Status

Pin 12 (MSTAT)	Mode
LOW	Receive
HIGH	Standby

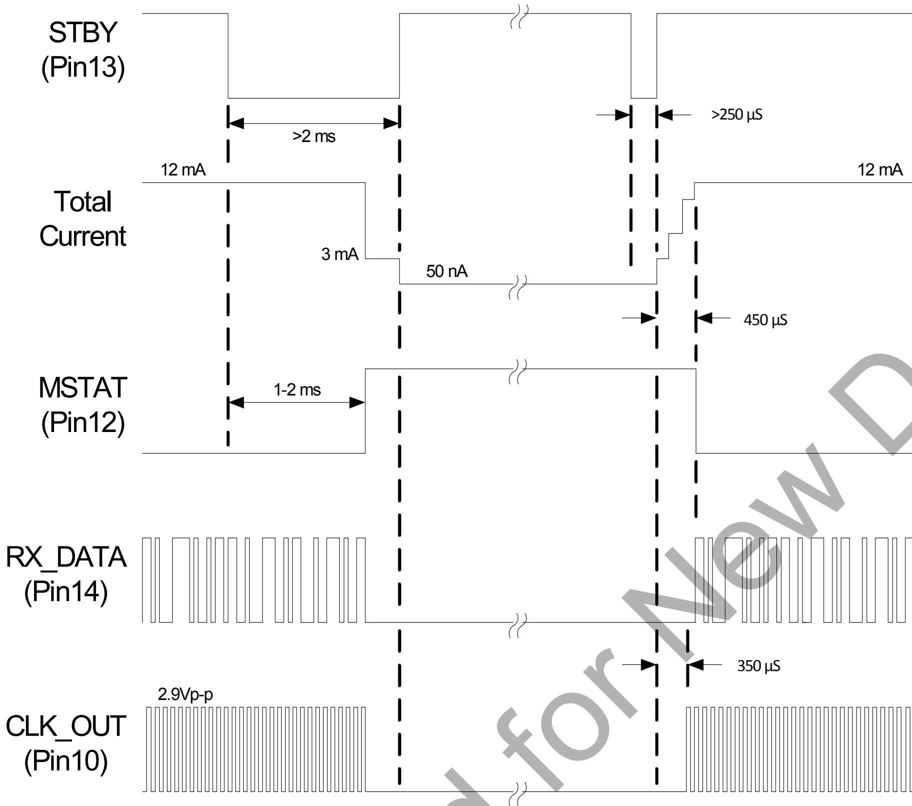


Figure 6. Standby Control and Timing

Once in standby mode, the device shuts down most functions, allowing for very low current consumption, but it still maintains all register settings for a fast transition back to the receive operating mode, as shown in Table 14.

Table 14. Operating State Response Time and Current Consumption

State / Mode	Response Time to Rx	Current in State/Mode
Standby	0.5 ms	50 nA
Receive	N/A	12 mA

It is also possible to reset the device by using RST (pin 2). This mode briefly cycles power on the device, before retuning the device to the receive operating mode as shown in Figure 7. The device takes approximately 20 ms to transition from reset to Receive mode.

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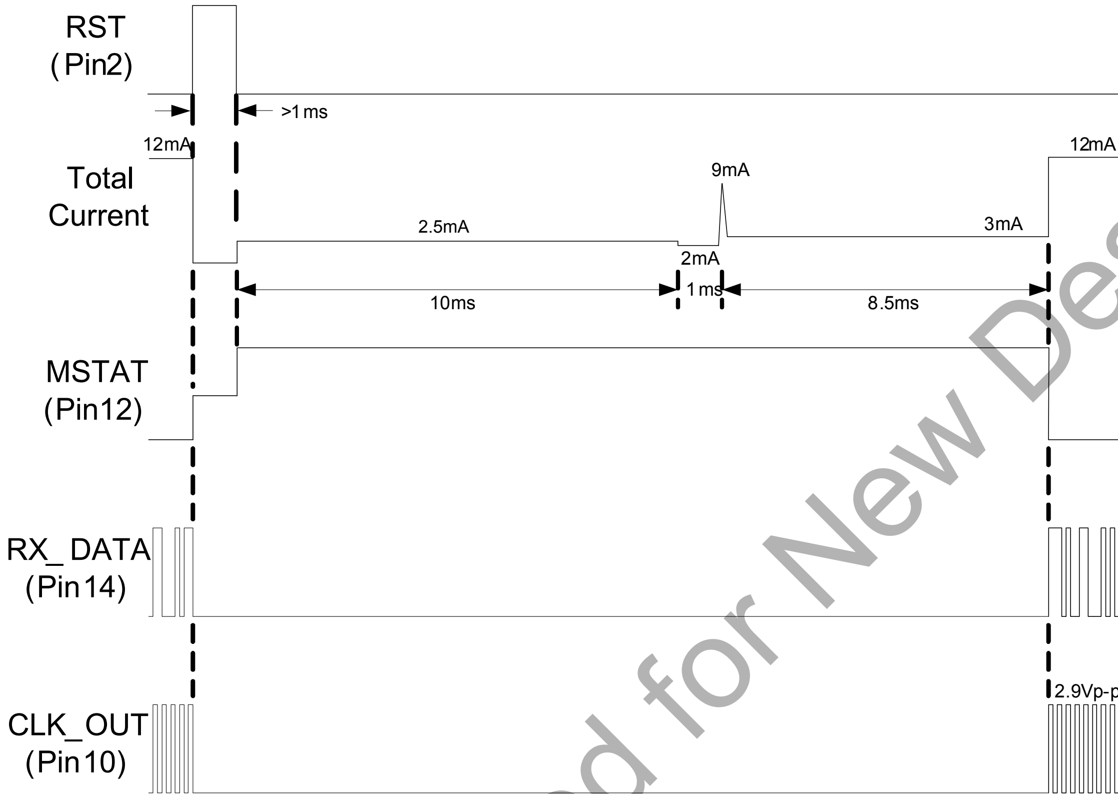


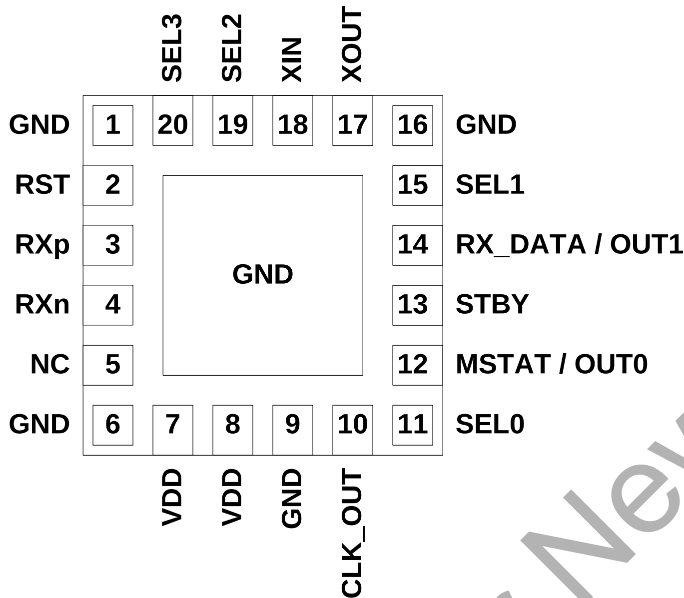
Figure 7. Device Reset Control and Timing

6. Additional Features

6.1. System Clock Output

A clock output is available on CLK_OUT (pin 10) of the Si4356, which can be used to drive an external MCU and avoid the need for additional oscillators in the application. The clock signal is valid when MSTAT is low. The clock frequency is set to 10 MHz for 315 MHz RX frequency selection and 15 MHz for all other frequencies. If this clock signal is not needed, then it can be turned off by connecting CLK_OUT (pin 10) to MSTAT/OUT0 (pin 12). The clock signal is turned off during Standby and Device Reset modes.

7. Pin Descriptions



Pin	Pin Name	I/O	Description
1	GND	GND	Ground
2	RST	I	Device reset
3	RXp	I	Differential RF receiver input pin
4	RXn	I	Differential RF receiver input pin
5	NC		No Connect
6	GND	GND	Ground
7	VDD	V_{DD}	Supply Voltage
8	VDD	V_{DD}	Supply Voltage
9	GND	GND	Ground
10	CLK_OUT	O	System reference clock output
11	SEL0	I	Configuration selector pin
12	MSTAT OUT0	O O	Mode status (Rx = 0, STBY = 1) Configuration output pin
13	STBY	I	Standby mode toggle
14	RX_DATA OUT1	O O	Receiver raw data output Configuration output pin
15	SEL1	I	Configuration selector pin

Pin	Pin Name	I/O	Description
16	GND	GND	GND
17	XOUT	O	Crystal oscillator output
18	XIN	I	Crystal oscillator input
19	SEL2	I	Configuration selector pin
20	SEL3	I	Configuration selector pin

8. Ordering Information

Part Number*	Description	Package Type	Operating Temperature
Si4356-B1A-FM	Si4356 EZRadio Standalone Receiver	3x3 QFN-20 Pb-free	–40 to 85 °C

***Note:** Add an “R” at the end of the device part number to denote tape and reel option.

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9. Package Outline

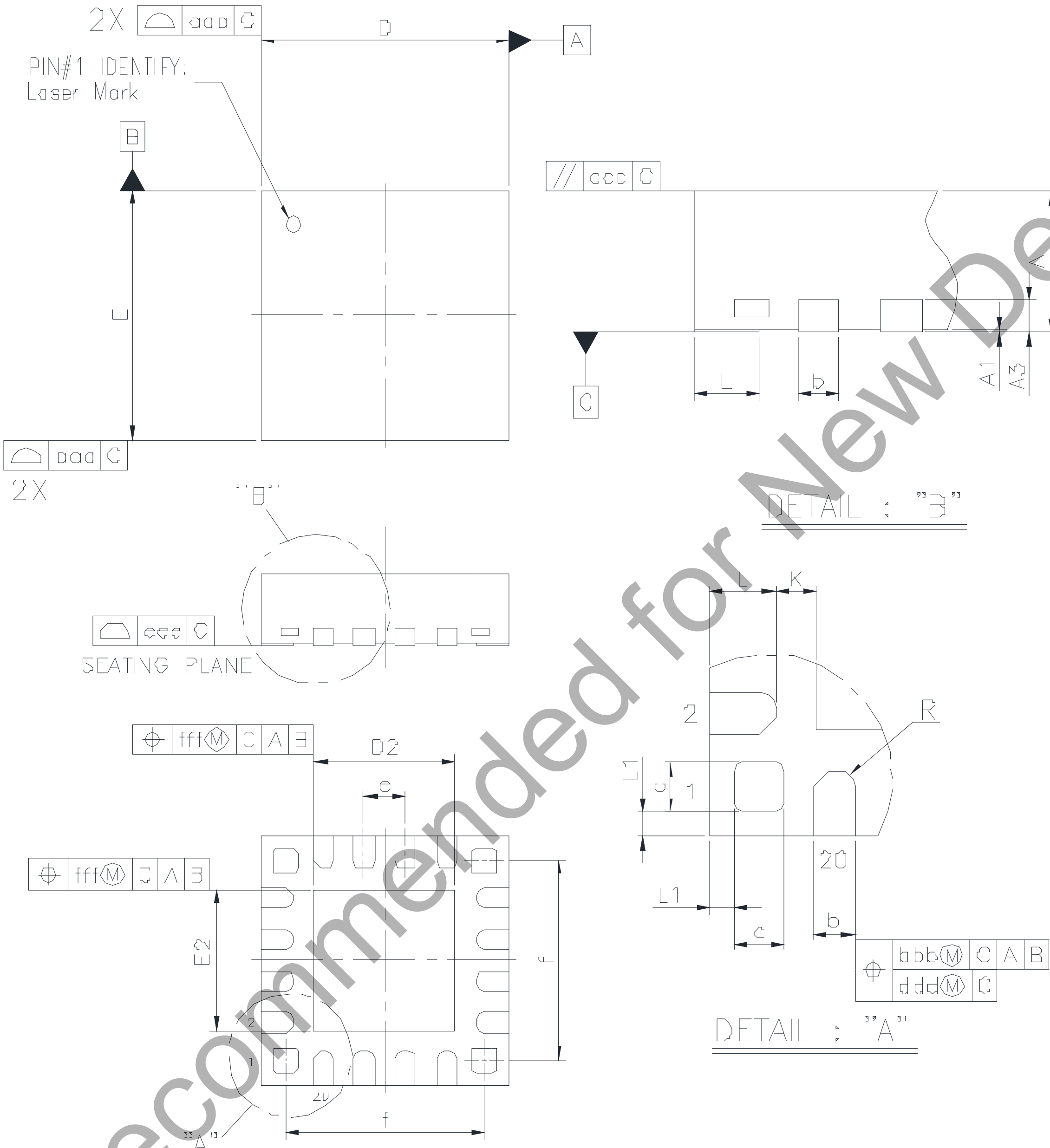

Figure 8. 20-pin QFN Package

Table 15. Package Diagram Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	0.20 REF		
b	0.18	0.25	0.30
c	0.25	0.30	0.35
D	3.00 BSC.		
D2	1.55	1.70	1.85
e	0.50 BSC.		
E	3.00 BSC.		
E2	1.55	1.70	1.85
f	2.40 BSC.		
L	0.30	0.40	0.50
aaa	0.15		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		
Note: All dimensions shown are in millimeters (mm) unless otherwise noted.			

10. PCB Land Pattern

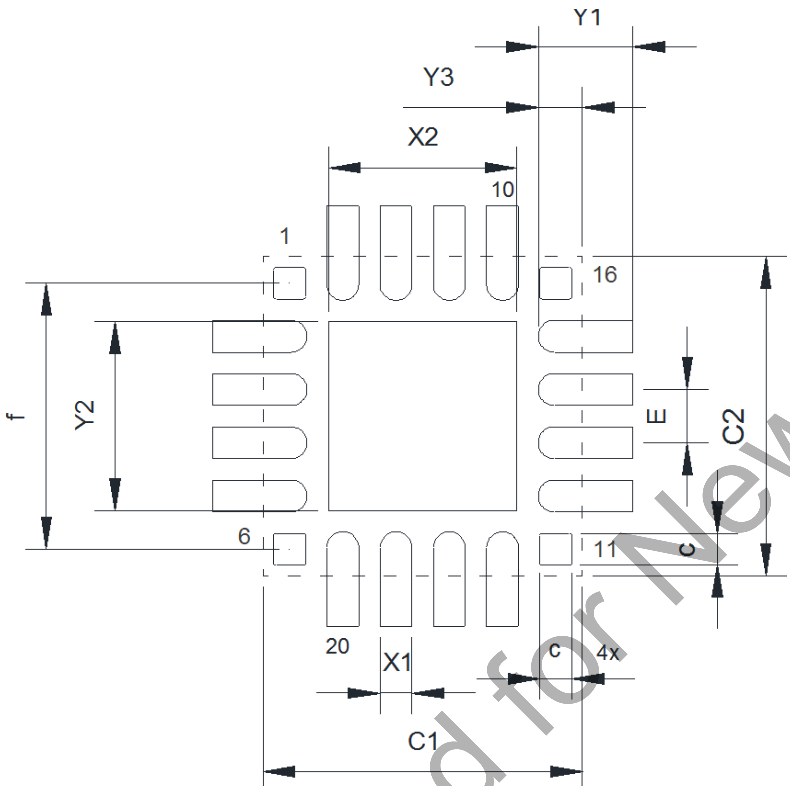

Figure 9. 20-pin QFN PCB Land Pattern (Top View)

Table 16. PCB Land Pattern Dimensions

Dimension	Min	Max
C1	3.00	
C2	3.00	
E	0.50 REF	
X1	0.25	0.35
X2	1.65	1.75
Y1	0.85	0.95
Y2	1.65	1.75
Y3	0.37	0.47
f	2.40 REF	
c	0.25	0.35
Note: : All dimensions shown are in millimeters (mm) unless otherwise noted.		

11. Top Marking

11.1. Si4356 Top Marking

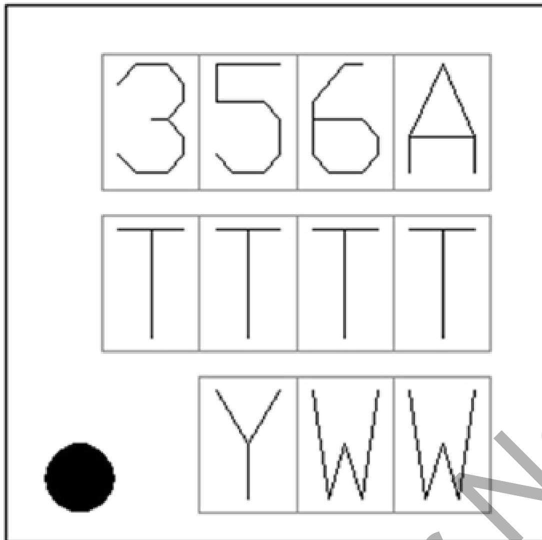

Figure 10. Si4356 Top Marking

11.2. Top Marking Explanation

Mark Method:	Laser	
Pin 1 Mark	Circle = 0.5 mm Diameter	
Font Size	0.6 mm Right Justified	
Line 1 Marking:	Product ID	356A
Line 2 Marking:	TTTT = Trace Code	Internal tracking number
Line 3 Marking:	YWW = Date Code	Corresponds to the last digit of the current year (Y) and the work week (WW) of the assembly date.

Document Change List

Revision 1.1 to Revision 1.2

January 18, 2016

- Added POR Information to Section 5.

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