

Description

The G75P04K uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is well suited for high current load applications.

General Features

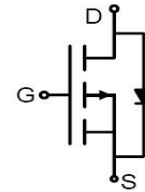


V_{DSS}	$R_{DS(ON)}$ @-10V(Typ)	I_D
-40V	7.5m Ω	-70A

- High density cell design for ultra low R_{dson}
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability
- RoHS Compliant

Application

- Power switch
- Load switch in high current applications
- DC/DC converters



Schematic diagram



Marking and pin assignment



Ordering Information

Part Number	Marking	Case	Packaging
G75P04K	G75P04	TO-252	2500pcs/Reel

Absolute Maximum Ratings ($T_C=25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-40	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	-70	A
Drain Current-Continuous($T_C=100^{\circ}C$)	$I_D(100^{\circ}C)$	-49.5	A
Pulsed Drain Current	I_{DM}	-200	A
Maximum Power Dissipation	P_D	130	W
Derating factor		1.04	W/ $^{\circ}C$
Single pulse avalanche energy (Note 5)	E_{AS}	1012	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^{\circ}C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	0.96	°C/W
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Electrical Characteristics ($T_C=25^\circ\text{C}$ unless otherwise noted)

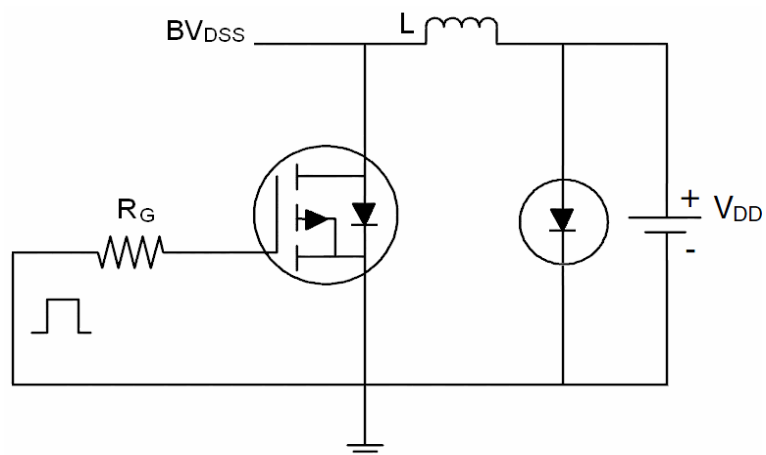
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=-250\mu A$	-40	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-40V, V_{GS}=0V$	-	-	-1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1.2	-1.9	-2.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=-10V, I_D=-20A$	-	7.5	10	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=-10V, I_D=-20A$	-	50	-	S
Dynamic Characteristics ^(Note 4)						
Input Capacitance	C_{iss}	$V_{DS}=-20V, V_{GS}=0V,$ $F=1.0\text{MHz}$	-	5380	-	PF
Output Capacitance	C_{oss}		-	570	-	PF
Reverse Transfer Capacitance	C_{rss}		-	500	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=-20V, R_L=2\Omega,$ $V_{GS}=-10V, R_G=1\Omega$	-	15	-	nS
Turn-on Rise Time	t_r		-	12	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	70	-	nS
Turn-Off Fall Time	t_f		-	18	-	nS
Total Gate Charge	Q_g	$V_{DS}=-20, I_D=-20A,$ $V_{GS}=-10V$	-	106	-	nC
Gate-Source Charge	Q_{gs}		-	22	-	nC
Gate-Drain Charge	Q_{gd}		-	27	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V_{SD}	$V_{GS}=0V, I_S=-70A$	-	-	-1.2	V
Diode Forward Current ^(Note 2)	I_S		-	-	-70	A
Reverse Recovery Time	t_{rr}	$T_J = 25^\circ\text{C}, I_F = -70A$ $di/dt = -100A/\mu s$ ^(Note 3)	-	53	-	nS
Reverse Recovery Charge	Q_{rr}		-	50	-	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

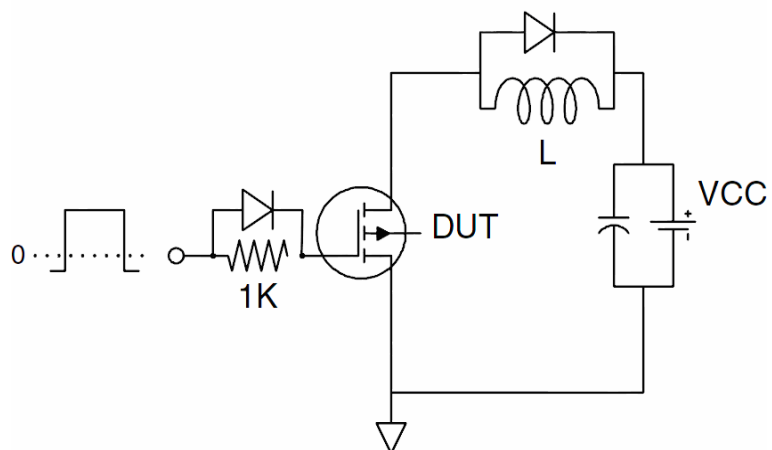
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. E_{AS} condition: $T_J=25^\circ\text{C}, V_{DD}=-20V, V_G=-10V, L=1\text{mH}, R_G=25\Omega, I_{AS}=45A$

Test Circuit

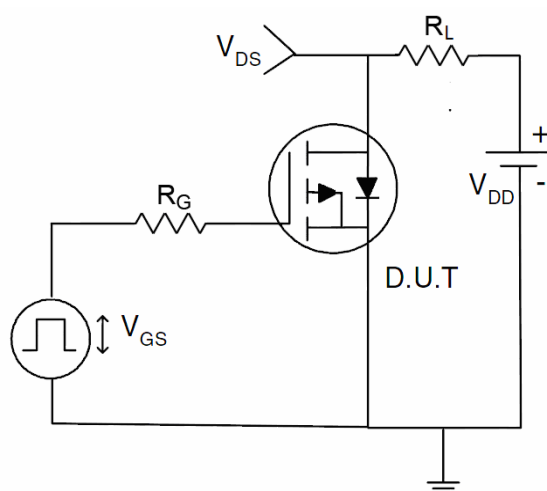
1) E_{AS} Test Circuit



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

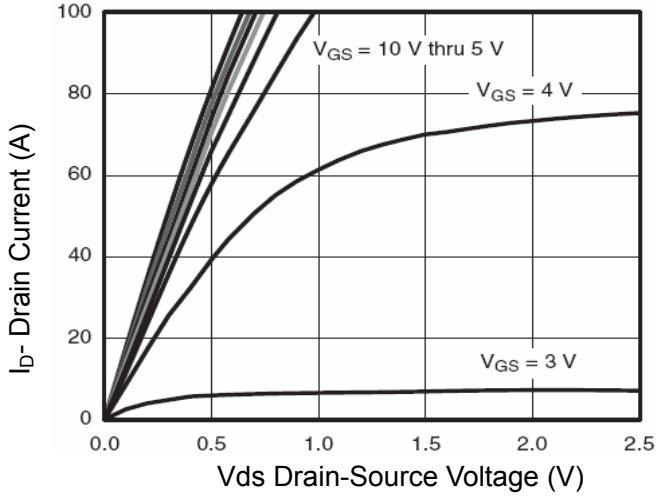


Figure 1 Output Characteristics

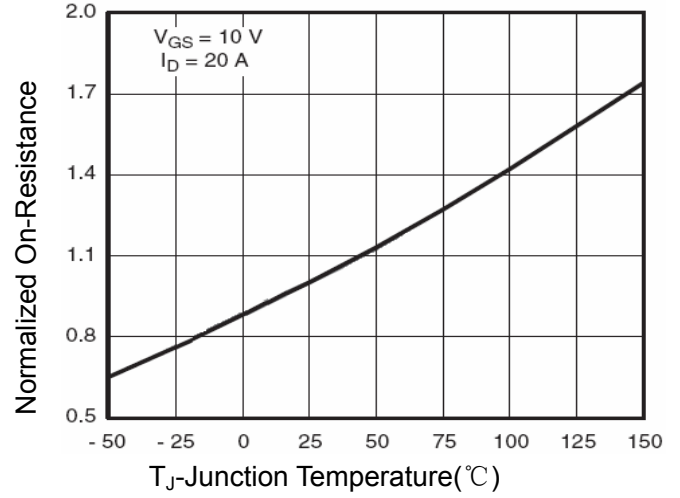


Figure 4 Rdson-Junction Temperature

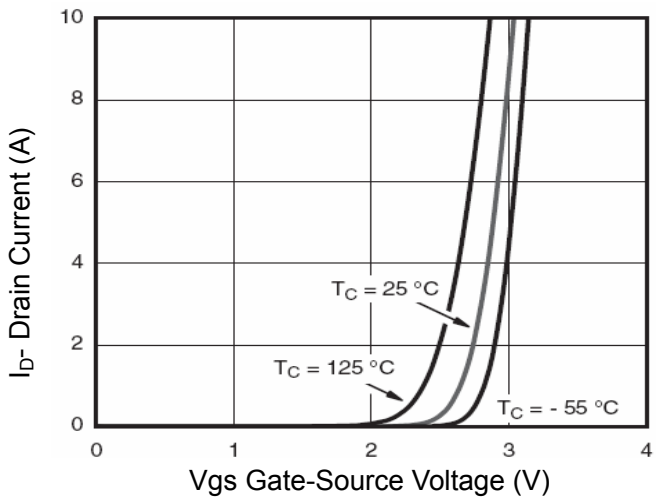


Figure 2 Transfer Characteristics

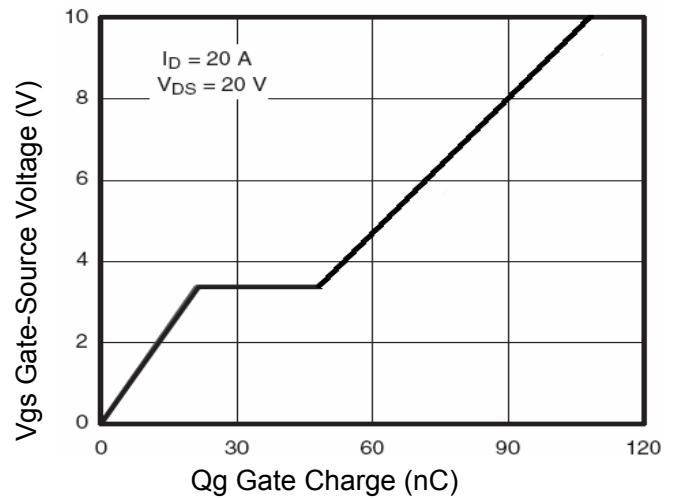


Figure 5 Gate Charge

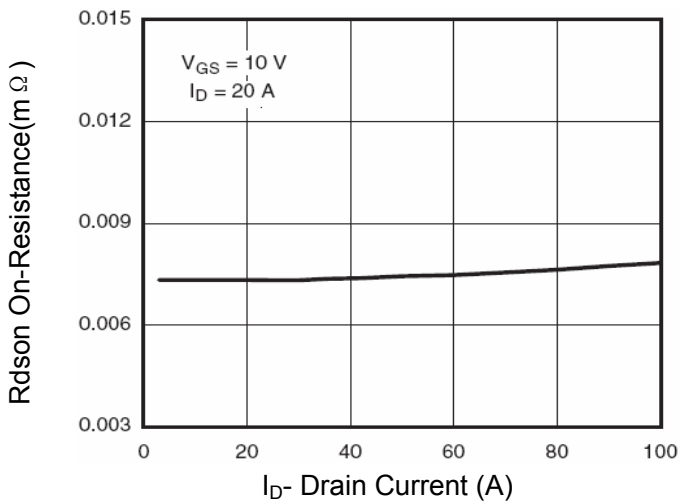


Figure 3 Rdson- Drain Current

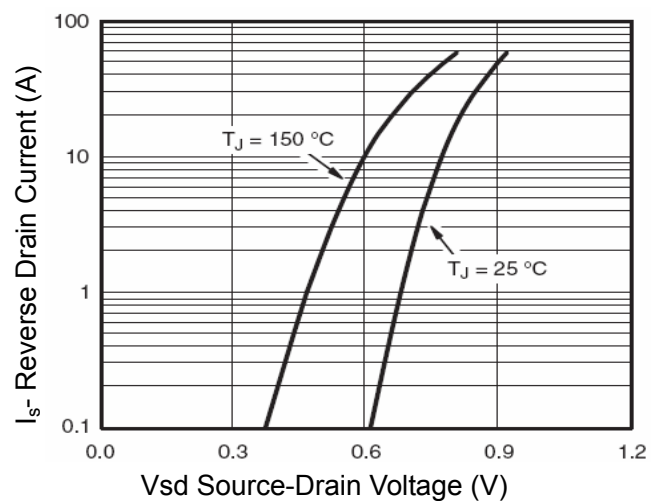


Figure 6 Source- Drain Diode Forward

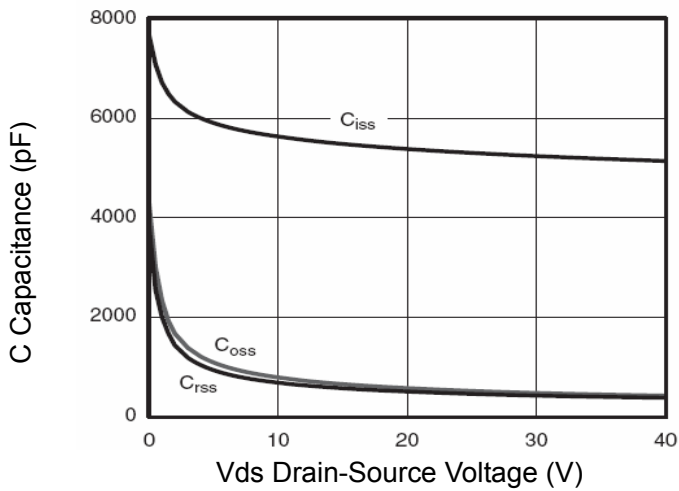


Figure 7 Capacitance vs Vds

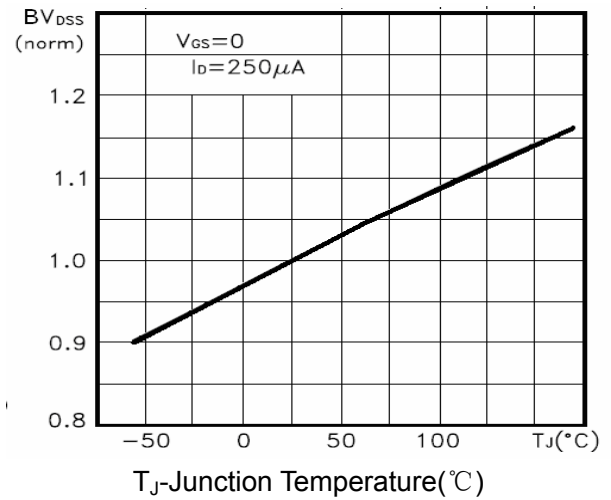


Figure 9 BV_{DSS} vs Junction Temperature

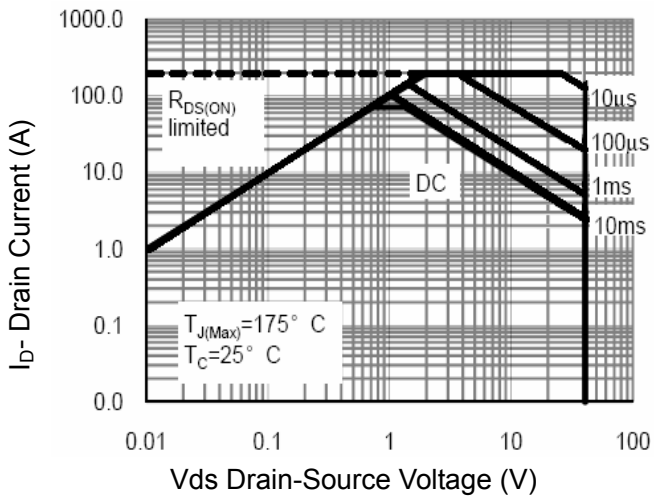


Figure 8 Safe Operation Area

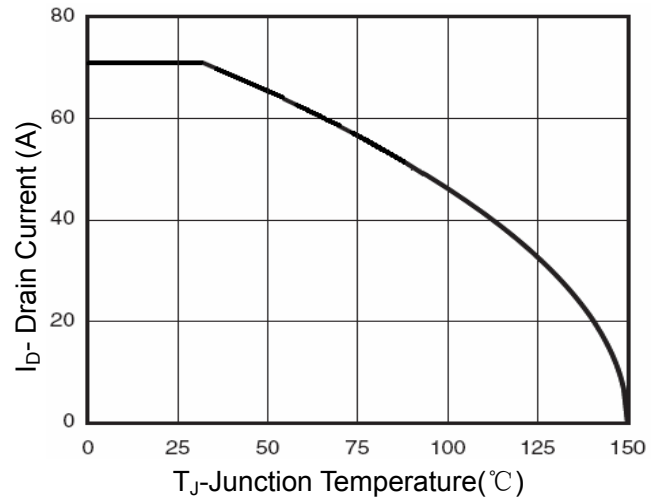


Figure 10 I_D Current Derating vs Junction Temperature

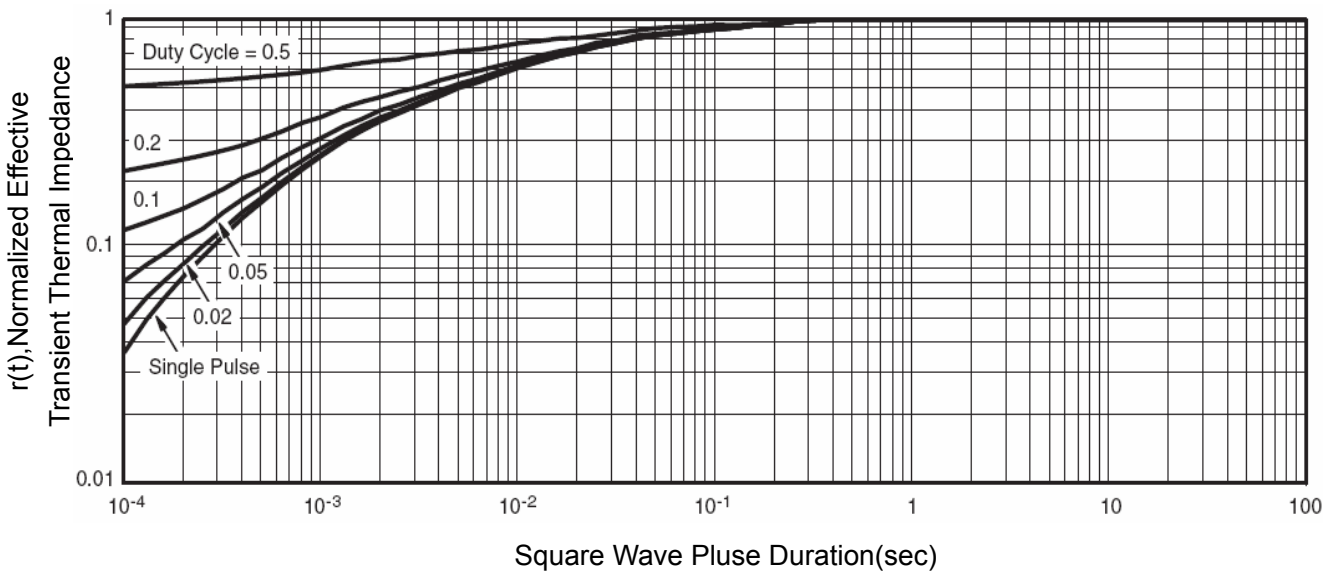
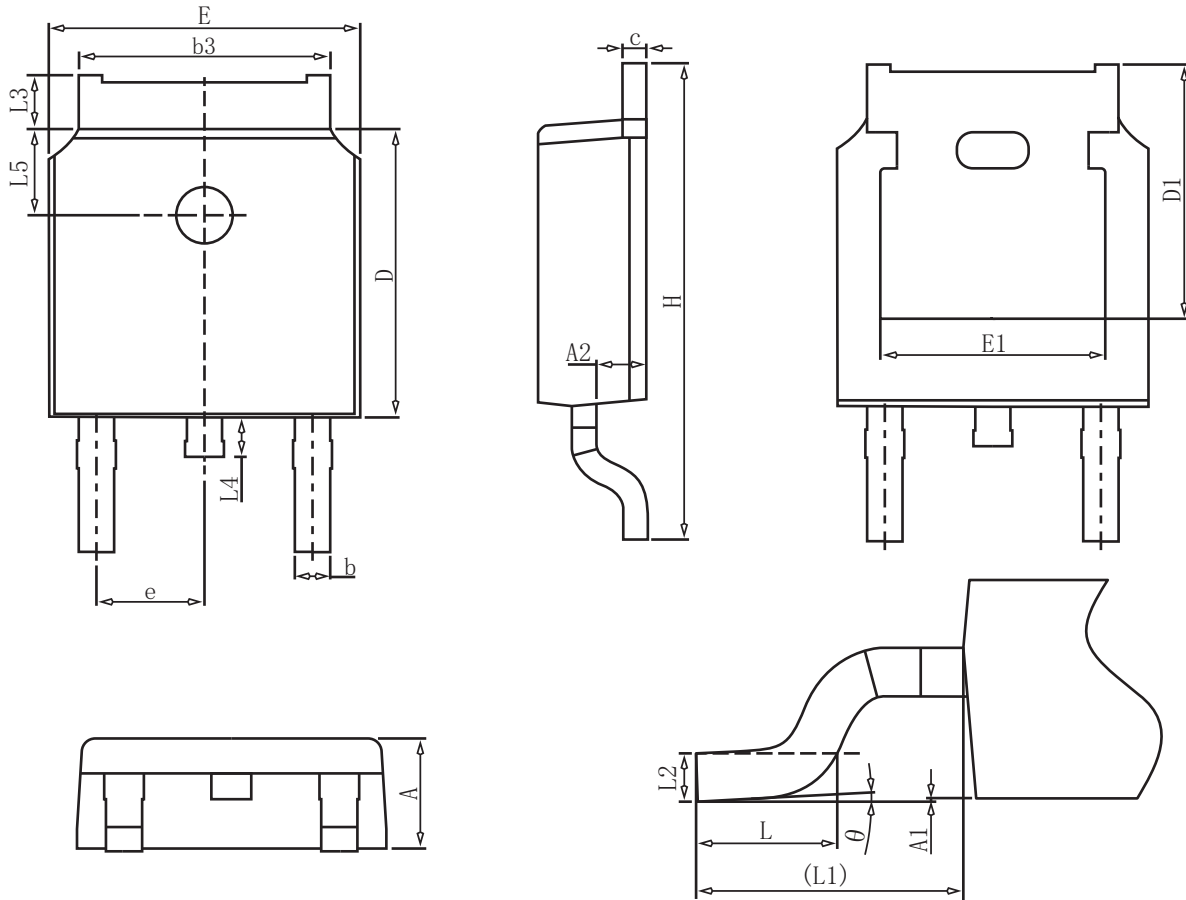


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-252 Package information



COMMON DIMENSIONS

SYMBOL	mm		
	MIN	NOM	MAX
A	2.20	2.30	2.40
A1	0.00	-	0.20
A2	0.97	1.07	1.17
b	0.68	0.78	0.90
b3	5.20	5.33	5.50
c	0.43	0.53	0.63
D	5.98	6.10	6.22
D1	5.30REF		
E	6.40	6.60	6.80
E1	4.63	-	-
e	2.286BSC		
H	9.40	10.10	10.50
L	1.38	1.50	1.75
L1	2.90REF		
L2	0.51BSC		
L3	0.88	-	1.28
L4	0.50	-	1.00
L5	1.65	1.80	1.95
θ	0°	-	8°