P-Channel Enhancement Mode Power MOSFET

Description

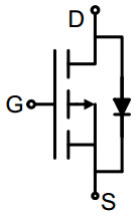
The G26P04D5 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge. It can be used in a wide variety of applications.

General Features

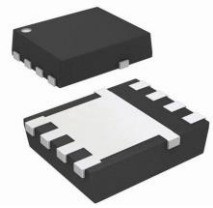
- V_{DS} -40 V
- I_D (at V_{GS} = -10V) -26A
- $R_{DS(ON)}$ (at V_{GS} = -10V) < 18mΩ
- $R_{DS(ON)}$ (at V_{GS} = -4.5V) < 22mΩ
- 100% Avalanche Tested
- RoHS Compliant

Application

- Power switch
- DC/DC converters



Schematic diagram



DFN5*6-8L

Device	Package	Marking	Packaging
G26P04D5	DFN5*6-8L	G26P04	5000pcs/Reel

Absolute Maximum Ratings T_C = 25ºC, unless otherwise noted

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	-40	V
Continuous Drain Current	I_D	-26	A
Pulsed Drain Current (note1)	I_{DM}	-91	A
Gate-Source Voltage	V_{GS}	±20	V
Power Dissipation	P_D	50	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 To 150	ºC

Thermal Resistance

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Ambient	R_{thJA}	50	ºC/W
Thermal Resistance, Junction-to-Case	R_{thJC}	2.5	ºC/W

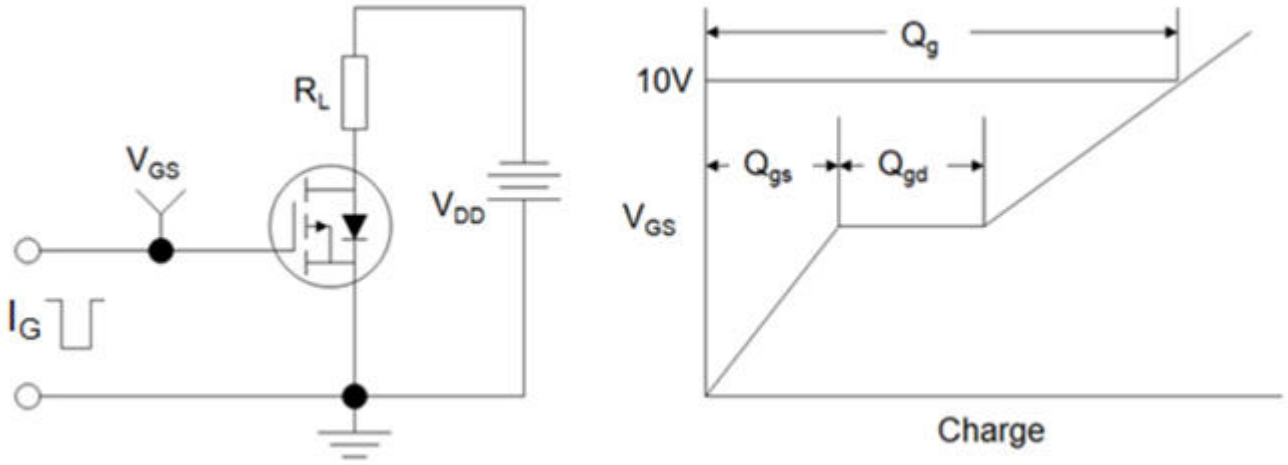
Specifications T_J = 25ºC, unless otherwise noted

Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Static Parameters						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = -250μA	-40	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -40V, V_{GS} = 0V	--	--	-1	uA
Gate-Source Leakage	I_{GSS}	V_{GS} = ±20V	--	--	±100	nA
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250μA	-1	-1.5	-2.5	V
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = -10V, I_D = - 12A	--	15	18	mΩ
		V_{GS} = -4.5V, I_D = - 12A	--	18	22	
Forward Transconductance	g_{FS}	V_{DS}=-5V,I_D=-12A	--	28	--	S
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = -20V, f = 1.0MHz	--	2479	--	pF
Output Capacitance	C_{oss}		--	274	--	
Reverse Transfer Capacitance	C_{rss}		--	204	--	
Total Gate Charge	Q_g	V_{DD} = -40V, I_D = -12A, V_{GS} = -10V	--	45	--	nC
Gate-Source Charge	Q_{gs}		--	6.1	--	
Gate-Drain Charge	Q_{gd}		--	10.1	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DS} = -20V, I_D = -1A, R_G = 6 Ω	--	9	--	ns
Turn-on Rise Time	t_r		--	7	--	
Turn-off Delay Time	$t_{d(off)}$		--	78	--	
Turn-off Fall Time	t_f		--	39	--	
Drain-Source Body Diode Characteristics						
Continuous Body Diode Current	I_S	T_C = 25ºC	--	--	-26	A
Body Diode Voltage	V_{SD}	T_J = 25ºC, I_F = Is, V_{GS} = 0V	--	--	-1.2	V

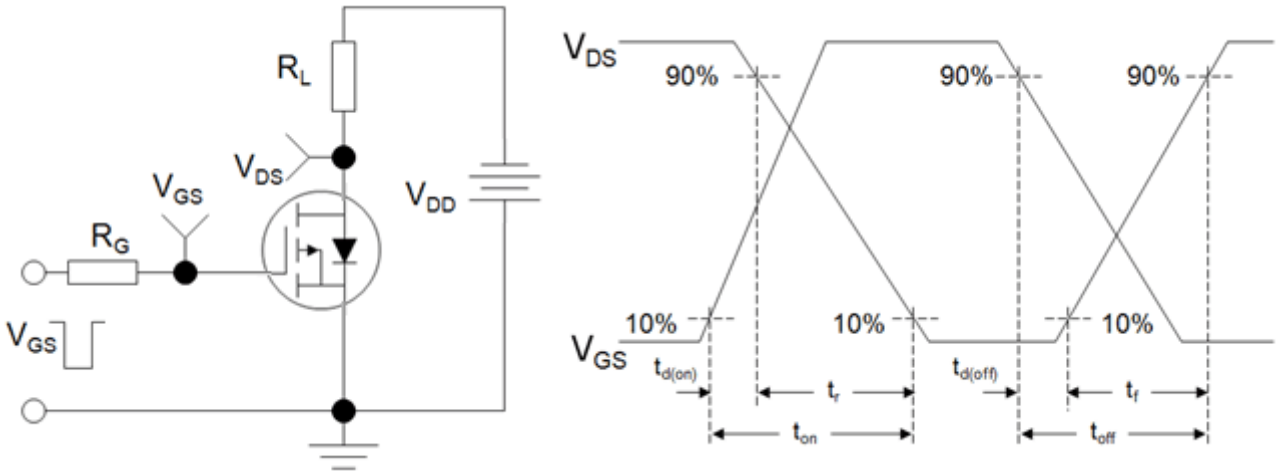
Notes

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. Identical low side and high side switch with identical R_G

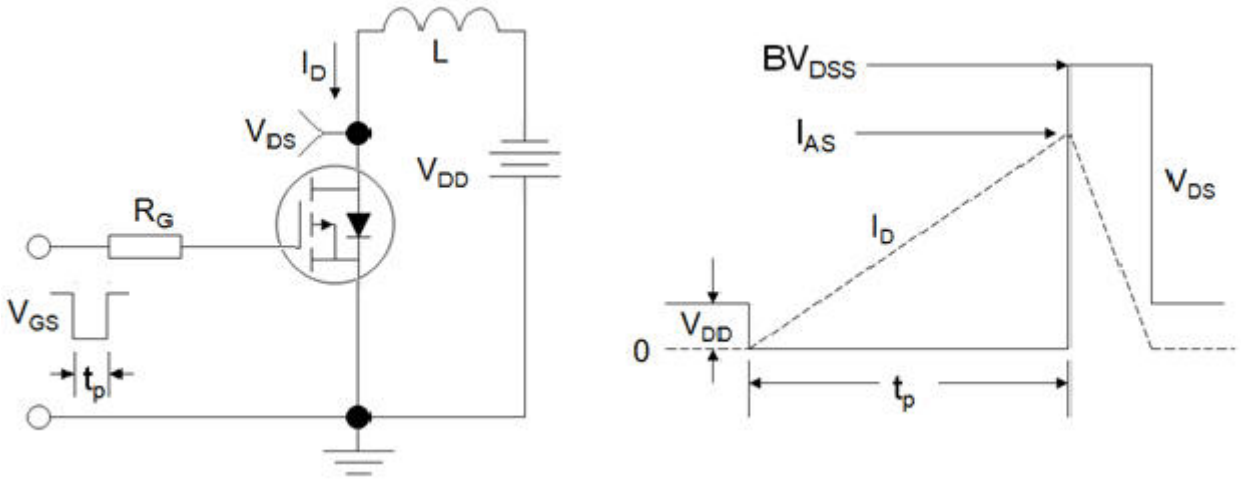
Gate Charge Test Circuit



Switch Time Test Circuit



EAS Test Circuit



Typical Characteristics T_J = 25ºC, unless otherwise noted

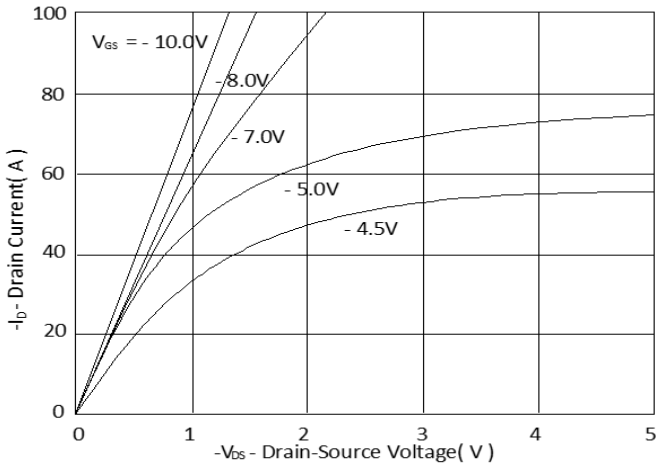


Fig.1 Typical Output Characteristics

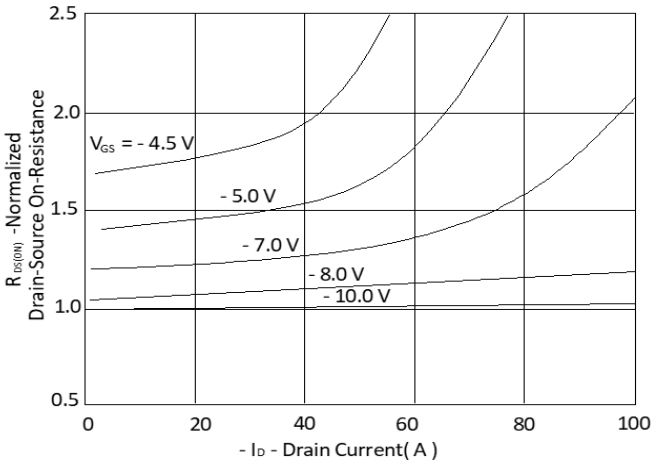


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

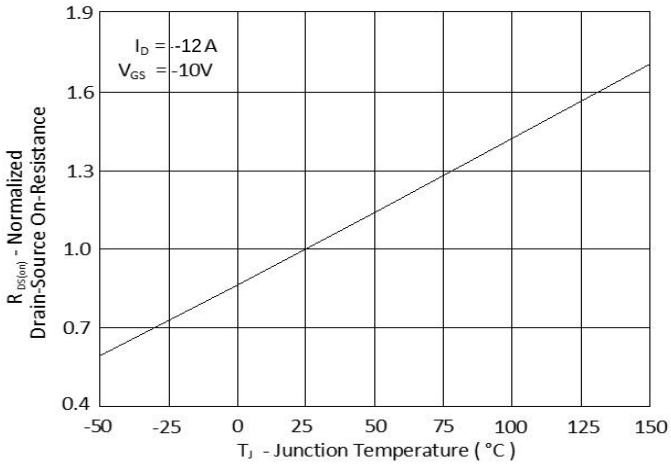


Fig.3 Normalized On-Resistance v.s. Junction Temperature

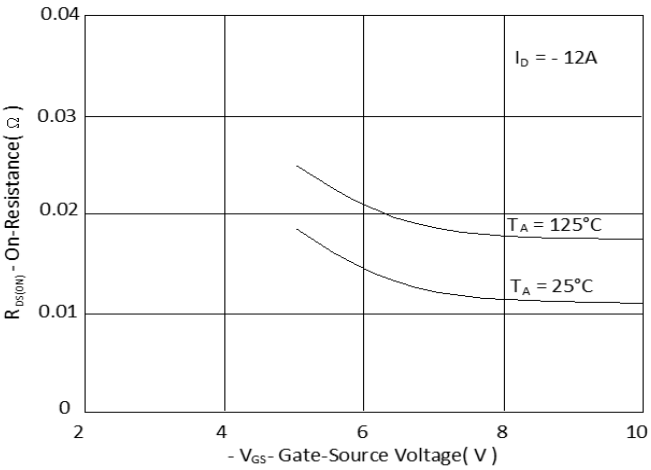


Fig.4 On-Resistance v.s. Gate Voltage

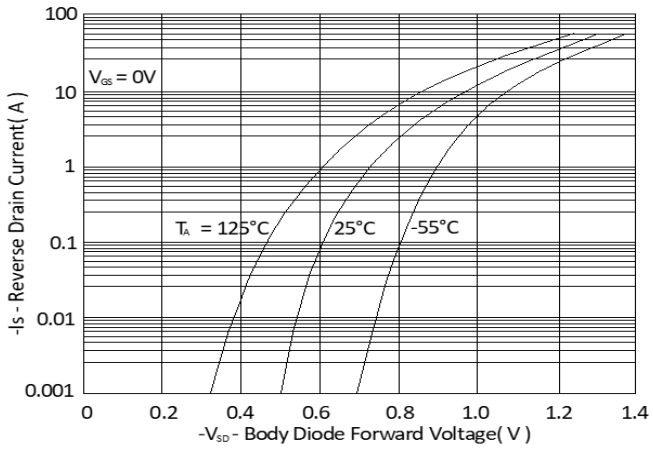


Fig.5 Forward Characteristic of Reverse Diode

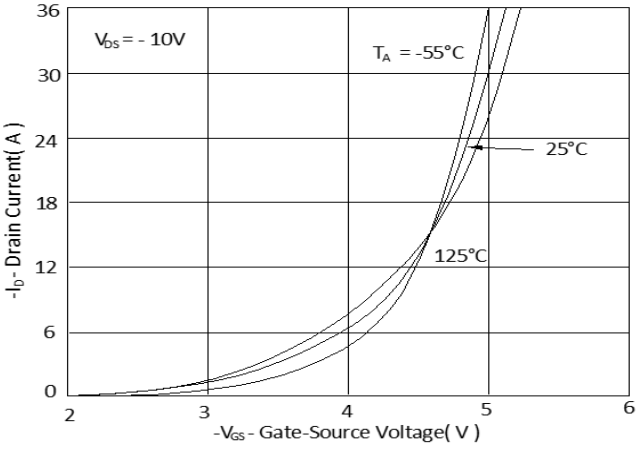


Fig.6 Transfer Characteristics

Typical Characteristics T_J = 25ºC, unless otherwise noted

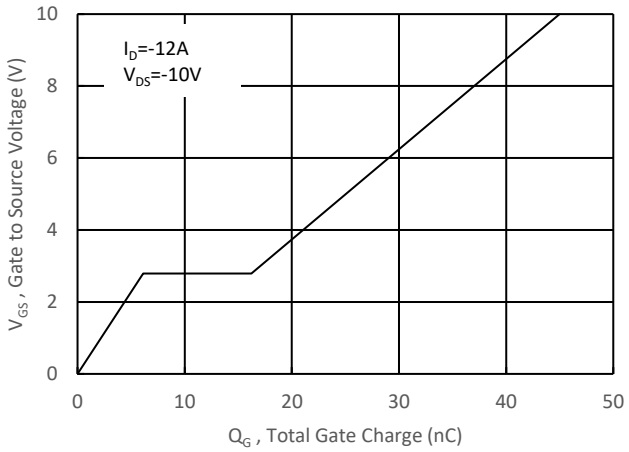


Fig.7 Gate Charge Characteristics

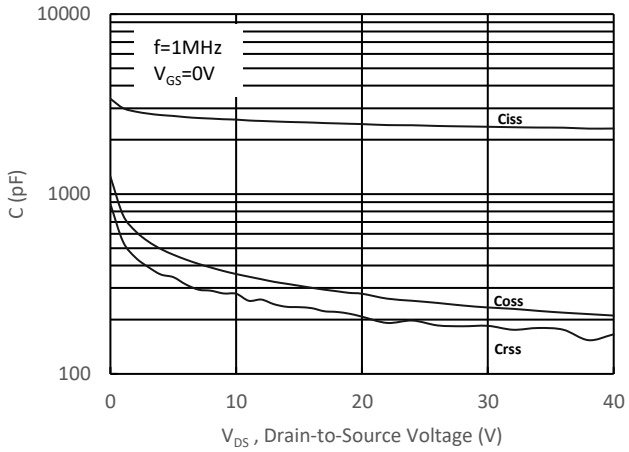


Fig.8 Typical Capacitance Characteristics

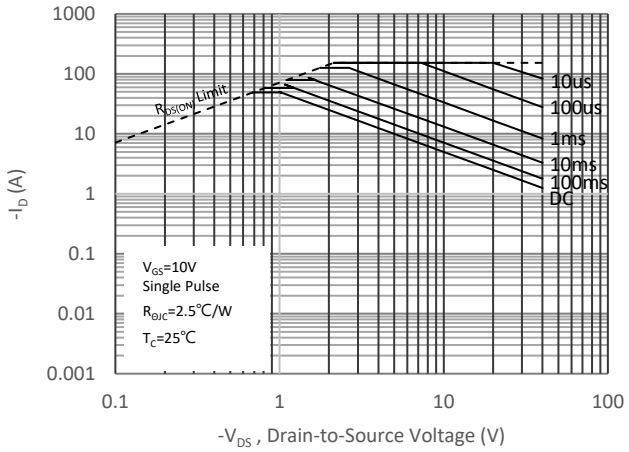


Fig 9. Maximum Safe Operating Area

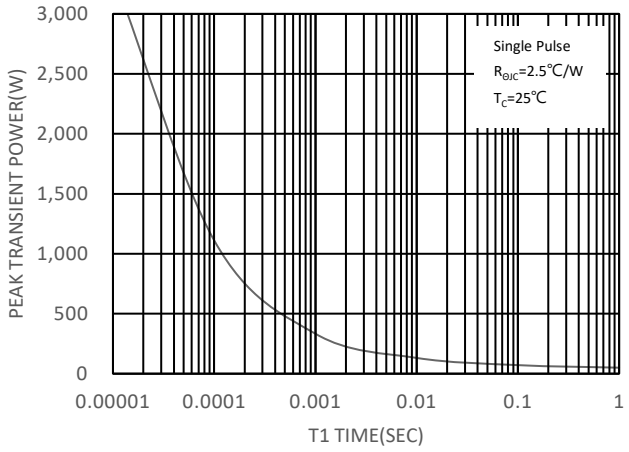


Fig 10. Single Pulse Maximum Power Dissipation

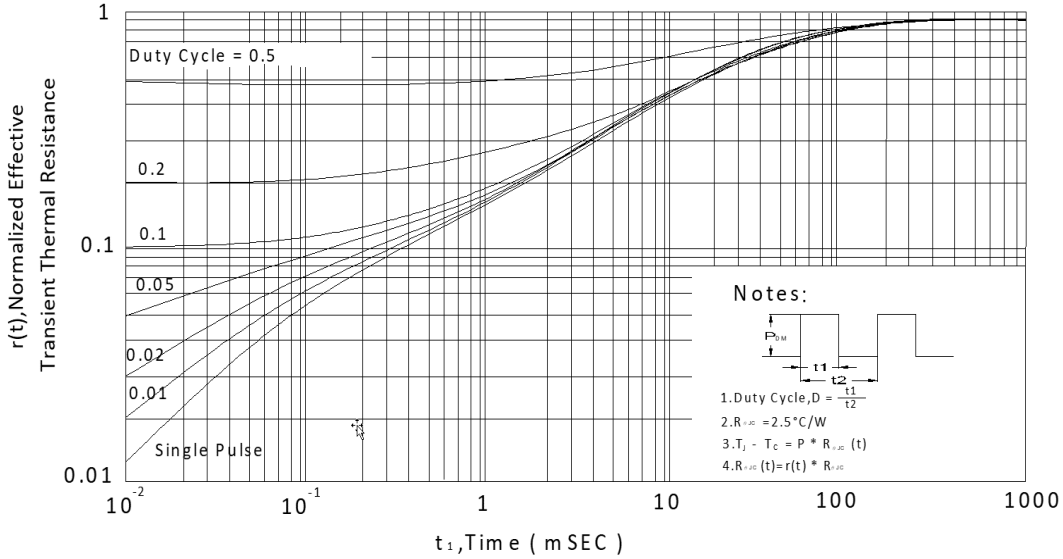
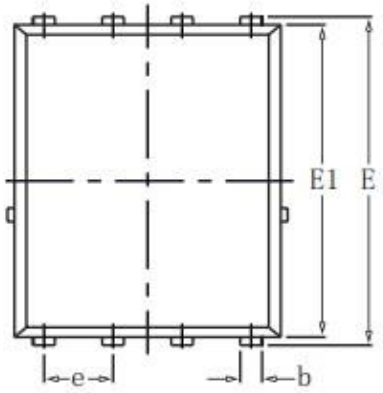
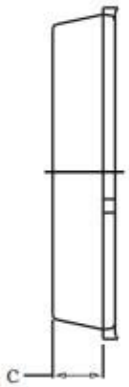
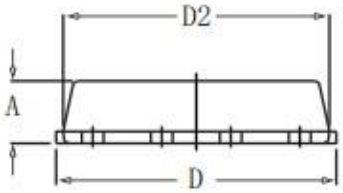


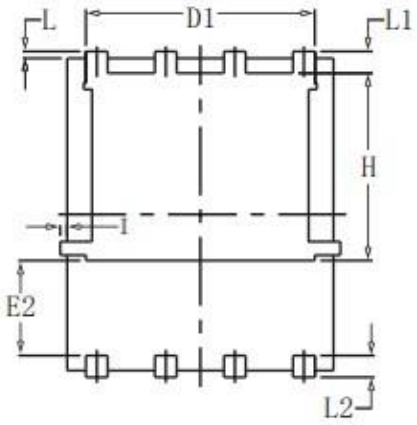
Fig 11. Effective Transient Thermal Impedance

DFN5*6-8L Package Information









SYMBOL	COMMON			
	MM		INCH	
	MIN	MAX	MIN	MAX
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.970	0.0324	0.0382
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.59	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	-	0.0630	-
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	-	0.18	-	0.0070