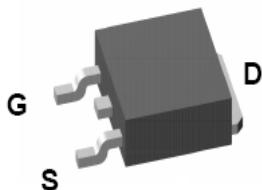


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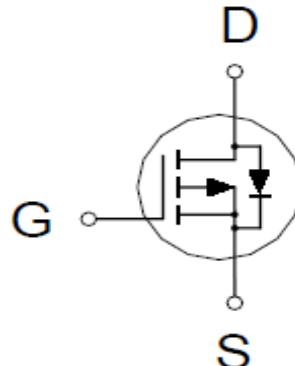
P-Channel Enhancement Mode MOSFET

PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
-40V	14mΩ @ $V_{GS} = -10V$	-51A



TO-252



1. GATE
2. DRAIN
3. SOURCE

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Drain-Source Voltage	V_{DS}	-40	V
Gate-Source Voltage	V_{GS}	± 25	V
Continuous Drain Current ²	I_D	-51	A
$T_C = 100^\circ C$	I_D	-40	
Pulsed Drain Current ¹	I_{DM}	-150	
Avalanche Current	I_{AS}	-38	
Avalanche Energy	E_{AS}	72.2	mJ
Power Dissipation	P_D	65	W
$T_C = 100^\circ C$	P_D	42	
Junction & Storage Temperature Range	T_j, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{0JC}		1.9	°C / W
Junction-to-Ambient	R_{0JA}		62.5	

¹Pulse width limited by maximum junction temperature.

²Package limitation current is -40A.

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ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}} = 0\text{V}, I_D = -250\mu\text{A}$	-40			V
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}} = V_{\text{GS}}, I_D = -250\mu\text{A}$	-1	-1.8	-3	
Gate-Body Leakage	I_{GSS}	$V_{\text{DS}} = 0\text{V}, V_{\text{GS}} = \pm 25\text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}} = -32\text{V}, V_{\text{GS}} = 0\text{V}$			-1	μA
		$V_{\text{DS}} = -30\text{V}, V_{\text{GS}} = 0\text{V}, T_J = 125^\circ\text{C}$			-10	
Drain-Source On-State Resistance ¹	$R_{\text{DS}(\text{ON})}$	$V_{\text{GS}} = -4.5\text{V}, I_D = -15\text{A}$		14	20	$\text{m}\Omega$
		$V_{\text{GS}} = -10\text{V}, I_D = -20\text{A}$		10	14	
Forward Transconductance ¹	g_{fs}	$V_{\text{DS}} = -5\text{V}, I_D = -20\text{A}$		50		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{\text{GS}} = 0\text{V}, V_{\text{DS}} = -20\text{V}, f = 1\text{MHz}$		2670		pF
Output Capacitance	C_{oss}			313		
Reverse Transfer Capacitance	C_{rss}			222		
Gate Resistance	R_g	$V_{\text{GS}} = 0\text{V}, V_{\text{DS}} = 0\text{V}, f = 1\text{MHz}$		4.5		Ω
Total Gate Charge ²	$Q_g(V_{\text{GS}} = -10\text{V})$	$V_{\text{DS}} = -20\text{V}, I_D = -20\text{A}$		58		nC
	$Q_g(V_{\text{GS}} = -4.5\text{V})$			29		
Gate-Source Charge ²	Q_{gs}			9		
Gate-Drain Charge ²	Q_{gd}			14		
Turn-On Delay Time ²	$t_{\text{d}(\text{on})}$	$V_{\text{DS}} = -20\text{V}, I_D \approx -20\text{A}, V_{\text{GS}} = -10\text{V}, R_{\text{GEN}} = 6\Omega$		29		nS
Rise Time ²	t_r			20		
Turn-Off Delay Time ²	$t_{\text{d}(\text{off})}$			90		
Fall Time ²	t_f			41		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_J = 25^\circ\text{C}$)						
Continuous Current ³	I_s				-50	A
Forward Voltage ¹	V_{SD}	$I_F = -20\text{A}, V_{\text{GS}} = 0\text{V}$			-1.3	V
Reverse Recovery Time	t_{rr}	$I_F = -20\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$		17		nS
Reverse Recovery Charge	Q_{rr}			6		nC

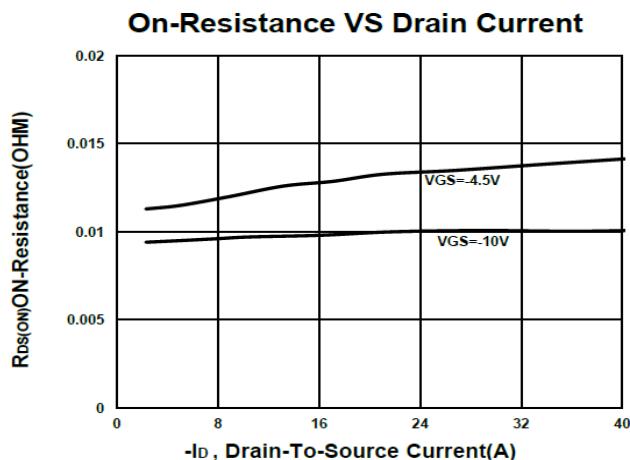
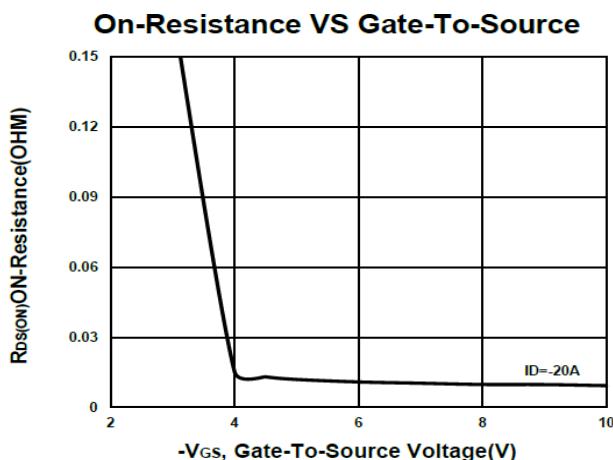
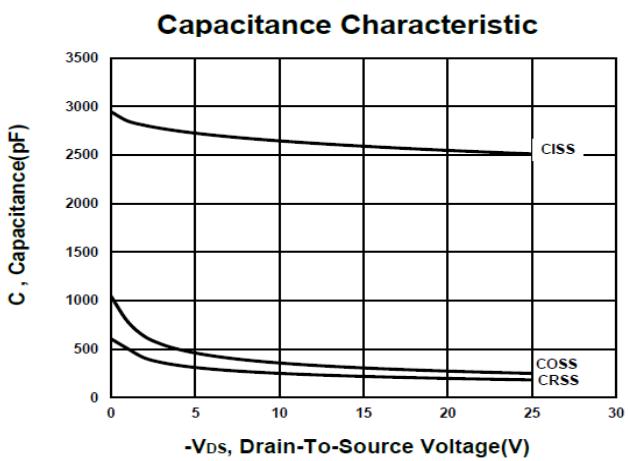
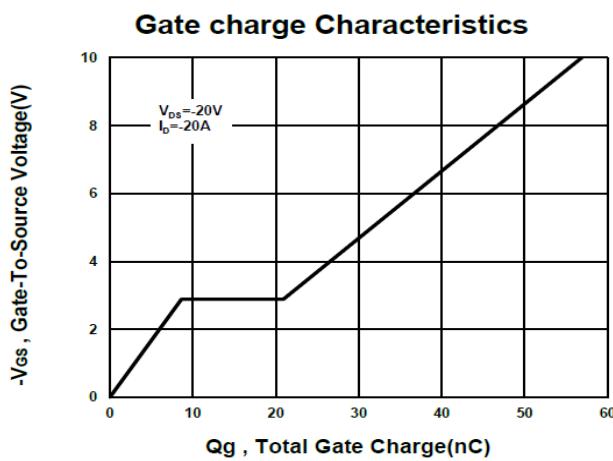
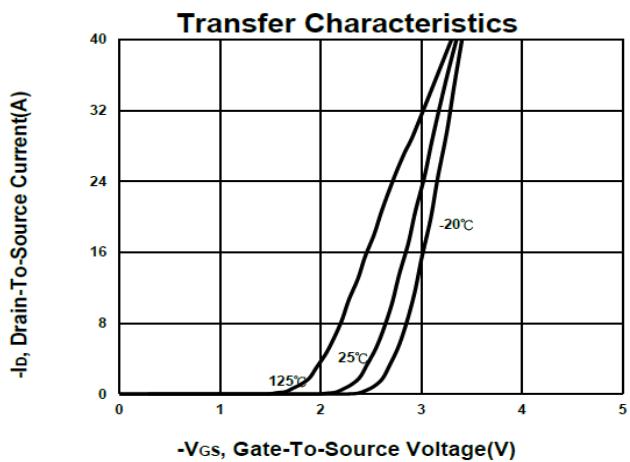
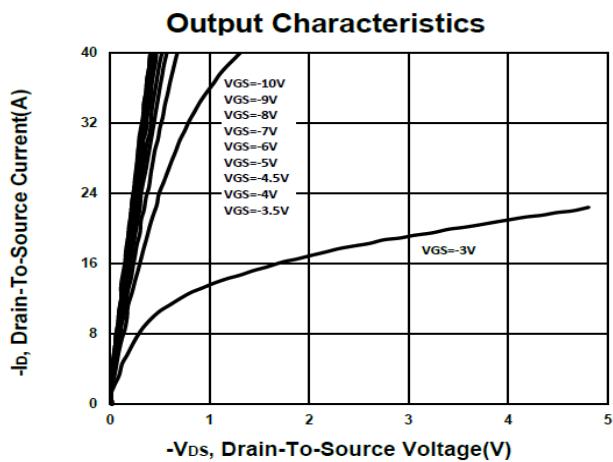
¹Pulse test : Pulse Width $\leq 300\text{ }\mu\text{sec}$, Duty Cycle $\leq 2\%$.

²Independent of operating temperature.

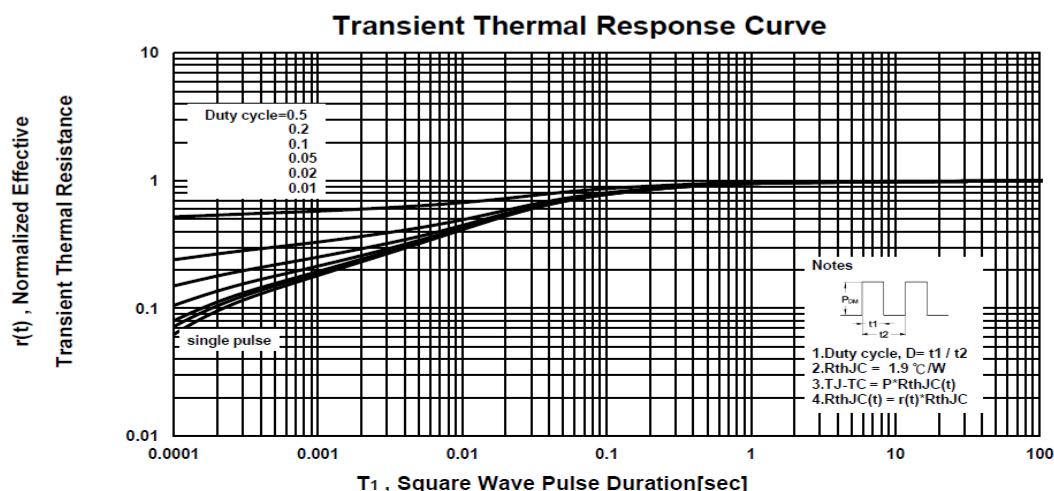
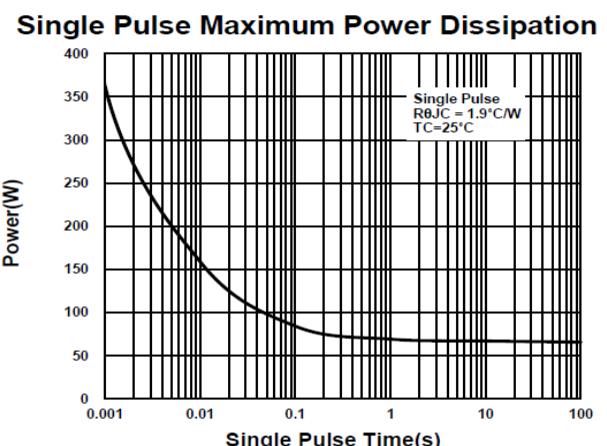
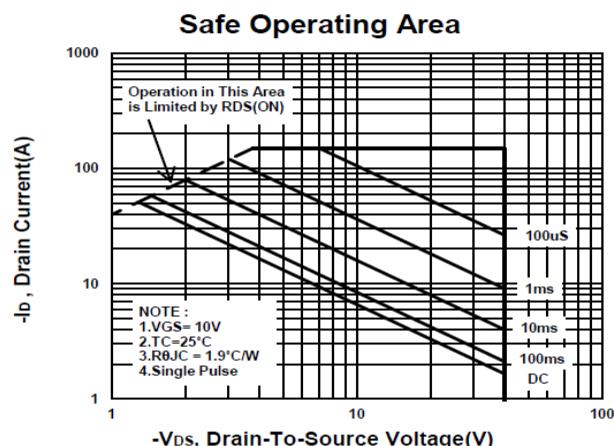
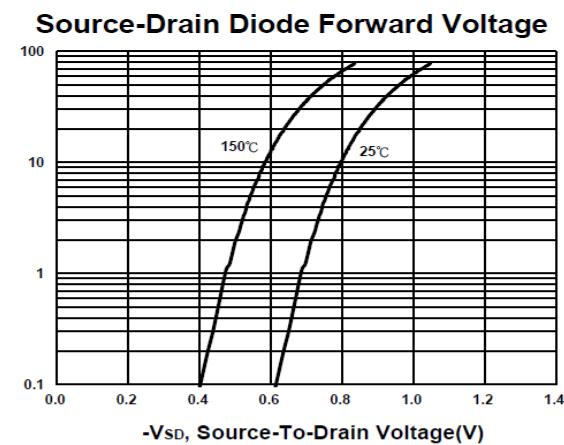
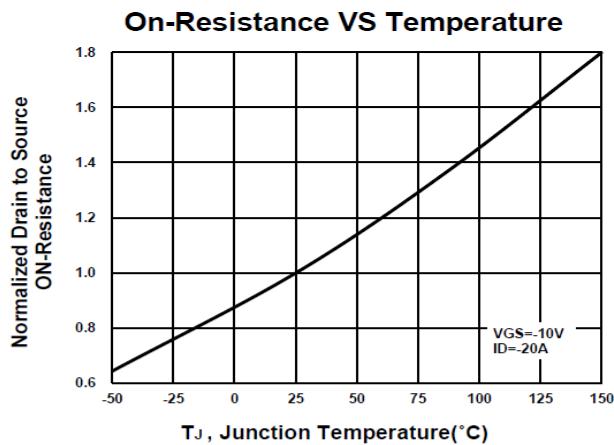
³Package limitation current is -40A.

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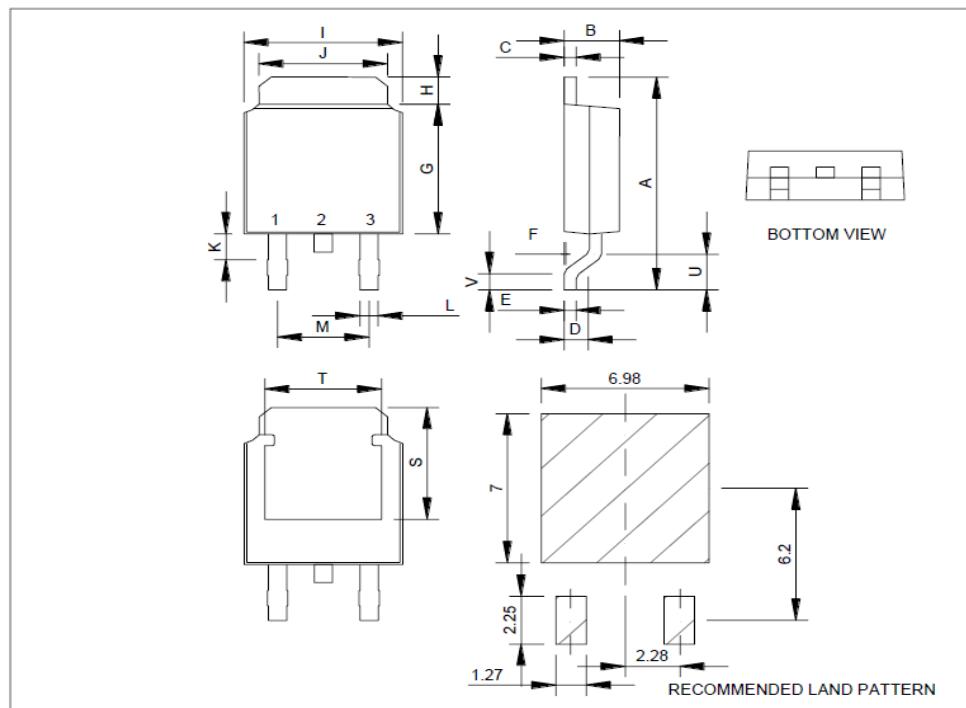


PD533BA P-Channel Enhancement Mode MOSFET

Package Dimension

TO-252 (DPAK) MECHANICAL DATA

Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	8.9	10	10.41	J	4.8		5.64
B	2.1	2.2	2.4	K	0.15		1.1
C	0.4	0.5	0.61	L	0.4	0.76	0.89
D	0.82	1.2	1.5	M	4.2	4.58	5
E	0.4	0.5	0.61	S	4.9	5.1	5.3
F	0		0.2	T	4.6	4.75	5.44
G	5.3	6.1	6.3	U	1.4		1.78
H	0.9		1.7	V	0.55	1.25	1.7
I	6.3	6.5	6.8				

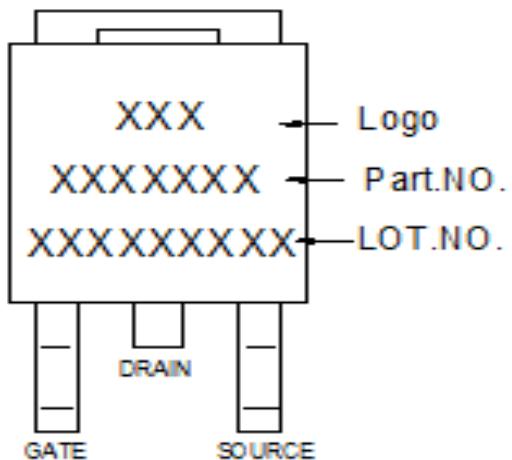


*因为各家封装模具不同而外观略有差异，不影响电性及Layout。

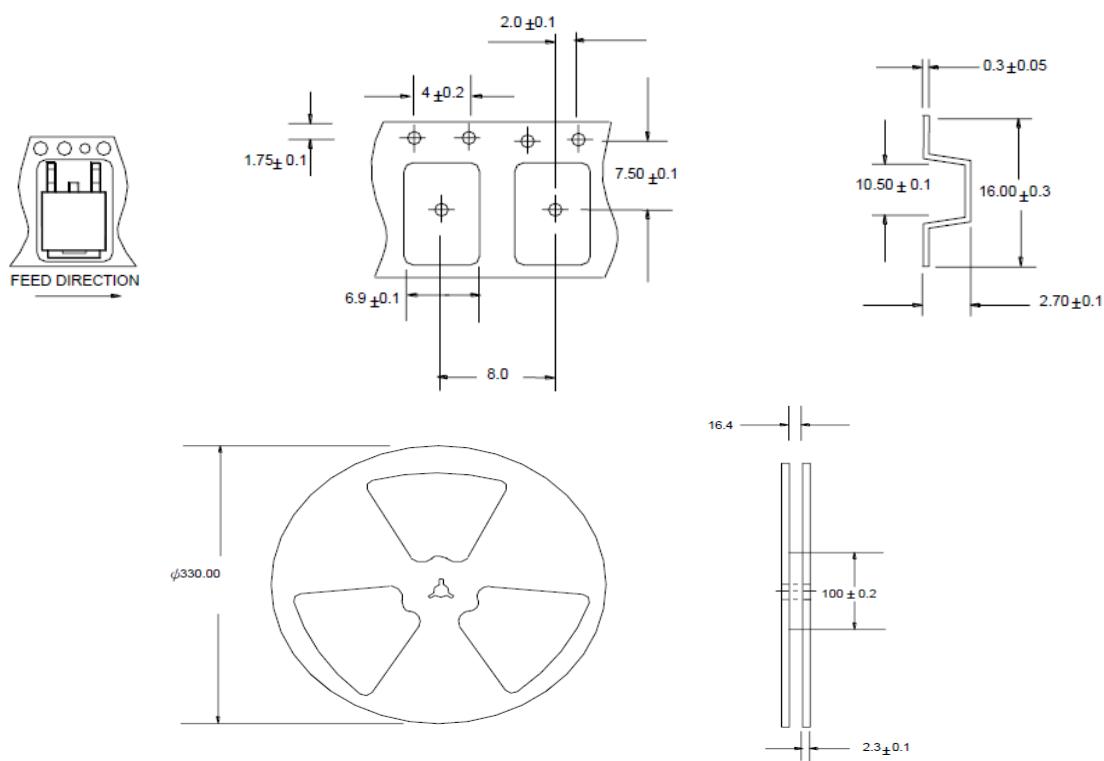
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P-Channel Enhancement Mode MOSFET

A. Marking Information



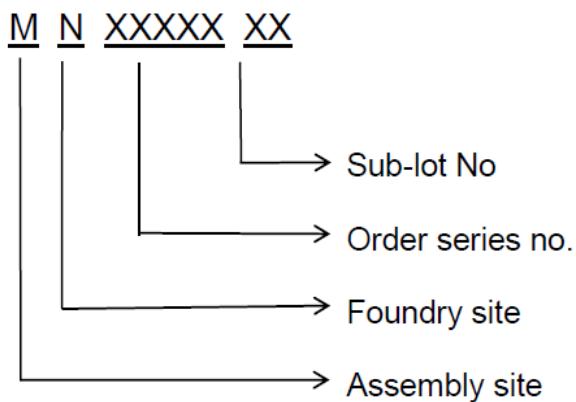
B. Tape&Reel Information: 2500pcs/Reel



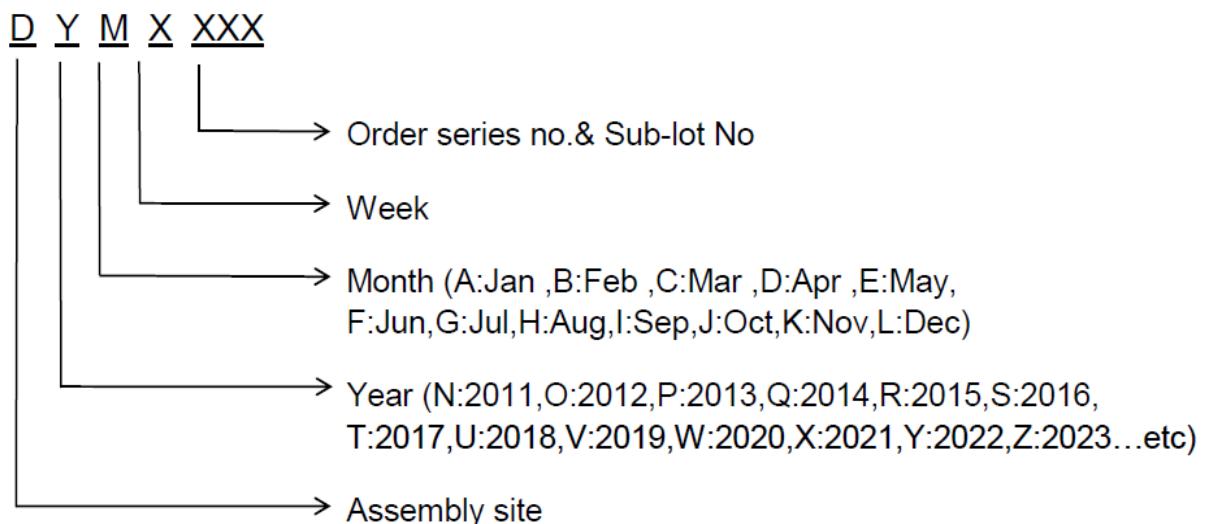
PD533BA **P-Channel Enhancement Mode MOSFET**

C. Lot No.&Date Code rule

1.Lot No.



2.Date Code



PD533BA P-Channel Enhancement Mode MOSFET

D.Label rule

标签内容(Label content)



1	Label Size	30 * 90 mm	
2	Font style	Times New Roman or Arial (或可区分英文“0”和数字“0”，“G”和“Q”的字型即可)	
3	U-NIKC	Height: 4 mm	
4	Package	Height: 2 mm	
5	Date	Height: 2 mm Shipping date: YYYY/MM/DD, ex. 2008/09/12	
6	Device	Height: 3 mm (Max: 16 Digit)	
7	Lot	Height: 3 mm (Max: 9 Digit) Sub lot	
8	D/C	Height: 3 mm (Max: 7 Digit)	
9	QTY	Height: 3 mm (Max: 6 Digit) Thousand mark is no needed	
10	RoHS label		long axis: 12 mm minor axis: 6 mm bottom color: White Font color: Black Font style: Arial
11	Halogen Free label		Diameter: 10 mm bottom color: Green Font color: Black Font style: Arial
12	Scan information	Device / Lot / D/C / QTY , Insert “/” between every parts. for example: P3055LDG/G12345601/GGG2301/2000 DPI (Dots per inch): Over 300 dpi Code : Code 128 Height: 6 mm at least	