NAU8822A
24-bit Stereo Audio CODEC with Speaker Driver

GENERAL DESCRIPTION

The NAU8822A is a low power, high quality CODEC for portable and general purpose audio applications. In addition to precision 24-bit stereo ADCs and DACs device integrates a broad range of additional functions to simplify implementation of complete audio system solutions. The NAU8822A includes drivers for speaker, headphone, and differential or stereo line outputs, and integrates preamps for stereo differential microphones, significantly reducing external component requirements. Also, a fractional PLL is available to accurately generate any audio sample rate for the CODEC using any commonly available system clock from 8MHz through 33MHz.

Advanced on-chip digital signal processing includes a 5-band equalizer, a 3-D audio enhancer, a mixed-signal automatic level control for the microphone or line input through the ADC, and a digital limiter/dynamic-range-compressor (DRC) function for the playback path. Additional digital filtering options are available in the ADC path, to simplify implementation of specific application requirements such as “wind noise reduction” and speech band enhancement. The digital audio input/output interface can operate as either a master or a slave.

The NAU8822A operates with analog supply voltages from 2.5V to 3.6V, while the digital core can operate at 1.7V to conserve power. The loudspeaker BTL output pair and two auxiliary line outputs can operate using a 5V supply to increase output power capability, enabling the NAU8822A to drive 1 Watt into an external speaker. Internal register controls enable flexible power saving modes by powering down sub-sections of the chip under software control.

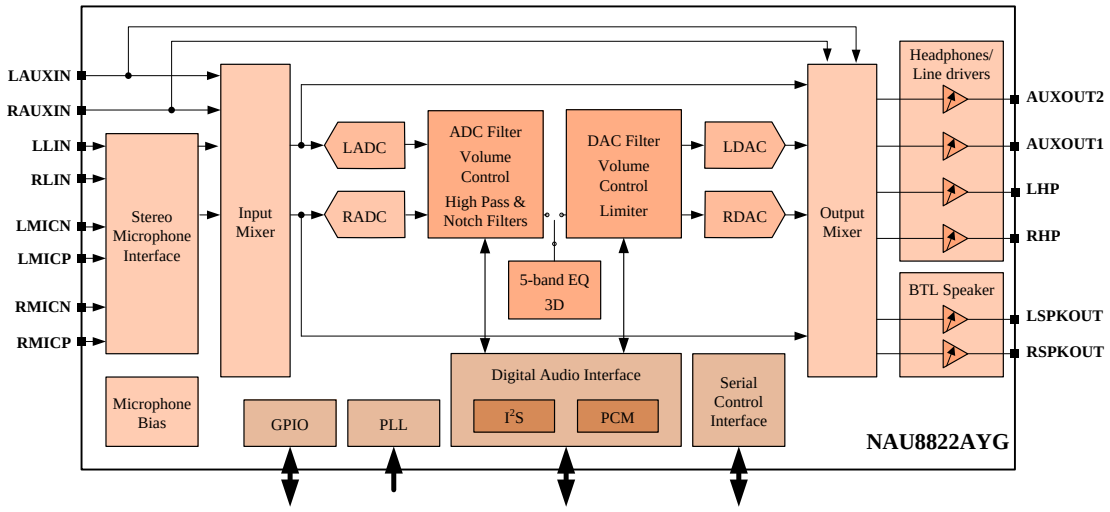
The NAU8822A is specified for operation from -40°C to +85°C. Automotive grade AEC-Q100 qualification & TS16949 compliant device is available upon request.

FEATURES

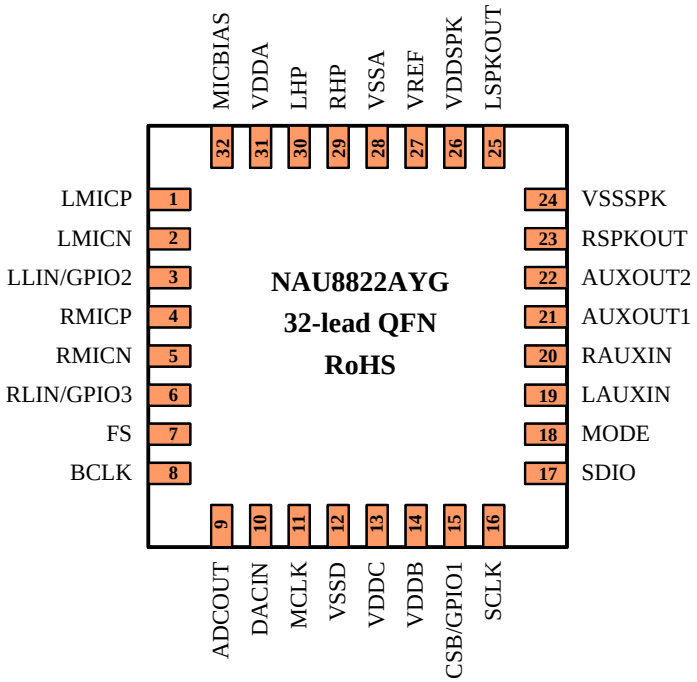
- DAC: 94dB SNR and -84dB THD (“A” weighted)
- ADC: 90dB SNR and -80dB THD (“A” weighted)
- Integrated BTL speaker driver: 1W into 8Ω
- Integrated head-phone driver: 40mW into 16Ω
- Integrated programmable microphone amplifier
- Integrated line input and line output
- On-chip PLL
- Integrated DSP with specific functions:
  - 5-band equalizer
  - 3-D audio enhancement
  - Input automatic level control (ALC/AGC)/limiter
  - Output dynamic-range-compressor/limiter
  - Notch filter and high pass filter
- Standard audio interfaces: PCM and I^2S
- Serial control interfaces with read/write capability
- Real-time readback of signal level and DSP status
- Supports any sample rate from 8kHz to 48kHz
- Industrial temperature range: –40°C to +85°C

APPLICATIONS

- Personal Media Players
- Smartphones
- Personal Navigation Devices
- Portable Game Players
- Camcorders
- Digital Still Cameras
- Portable TVs
- Stereo Bluetooth Headsets



Pinout



Part Number	Dimension	Package	Package Material
NAU8822AYG	5 x 5 mm	32-QFN	Pb-Free

Pin Descriptions

Pin #	Name	Type	Functionality
1	LMICP	Analog Input	Left MICP Input (common mode)
2	LMICN	Analog Input	Left MICN Input
3	LLIN/GPIO2	Analog Input / Digital I/O	Left Line Input / alternate Left MICP Input / GPIO2
4	RMICP	Analog Input	Right MICP Input (common mode)
5	RMICN	Analog Input	Right MICN Input
6	RLIN/GPIO3	Analog Input / Digital I/O	Right Line Input/ alternate Right MICP Input / Digital Output In 4-wire mode: Must be used for GPIO3
7	FS	Digital I/O	Digital Audio DAC and ADC Frame Sync
8	BCLK	Digital I/O	Digital Audio Bit Clock
9	ADCOUT	Digital Output	Digital Audio ADC Data Output
10	DACIN	Digital Input	Digital Audio DAC Data Input
11	MCLK	Digital Input	Master Clock Input
12	VSSD	Supply	Digital Ground
13	VDDC	Supply	Digital Core Supply
14	VDDB	Supply	Digital Buffer (Input/Output) Supply
15	CSB/GPIO1	Digital I/O	3-Wire MPU Chip Select or GPIO1 multifunction input/output
16	SCLK	Digital Input	3-Wire MPU Clock Input / 2-Wire MPU Clock Input
17	SDIO	Digital I/O	3-Wire MPU Data Input / 2-Wire MPU Data I/O
18	MODE	Digital Input	Control Interface Mode Selection Pin
19	LAUXIN	Analog Input	Left Auxiliary Input
20	RAUXIN	Analog Input	Right Auxiliary Input
21	AUXOUT1	Analog Output	Headphone Ground / Mono Mixed Output / Line Output
22	AUXOUT2	Analog Output	Headphone Ground / Line Output
23	RSPKOUT	Analog Output	BTL Speaker Positive Output or Right high current output
24	VSSSPK	Supply	Speaker Ground (ground pin for RSPKOUT, LSPKOUT, AUXOUT2 and AUXTOUT1 output drivers)
25	LSPKOUT	Analog Output	BTL Speaker Negative Output or Left high current output
26	VDDSPK	Supply	Speaker Supply (power supply pin for RSPKOUT, LSPKOUT, AUXOUT2 and AUXTOUT1 output drivers)
27	VREF	Reference	Decoupling for Midrail Reference Voltage
28	VSSA	Supply	Analog Ground
29	RHP	Analog Output	Headphone Positive Output / Line Output Right
30	LHP	Analog Output	Headphone Negative Output / Line Output Left
31	VDDA	Supply	Analog Power Supply
32	MICBIAS	Analog Output	Microphone Bias

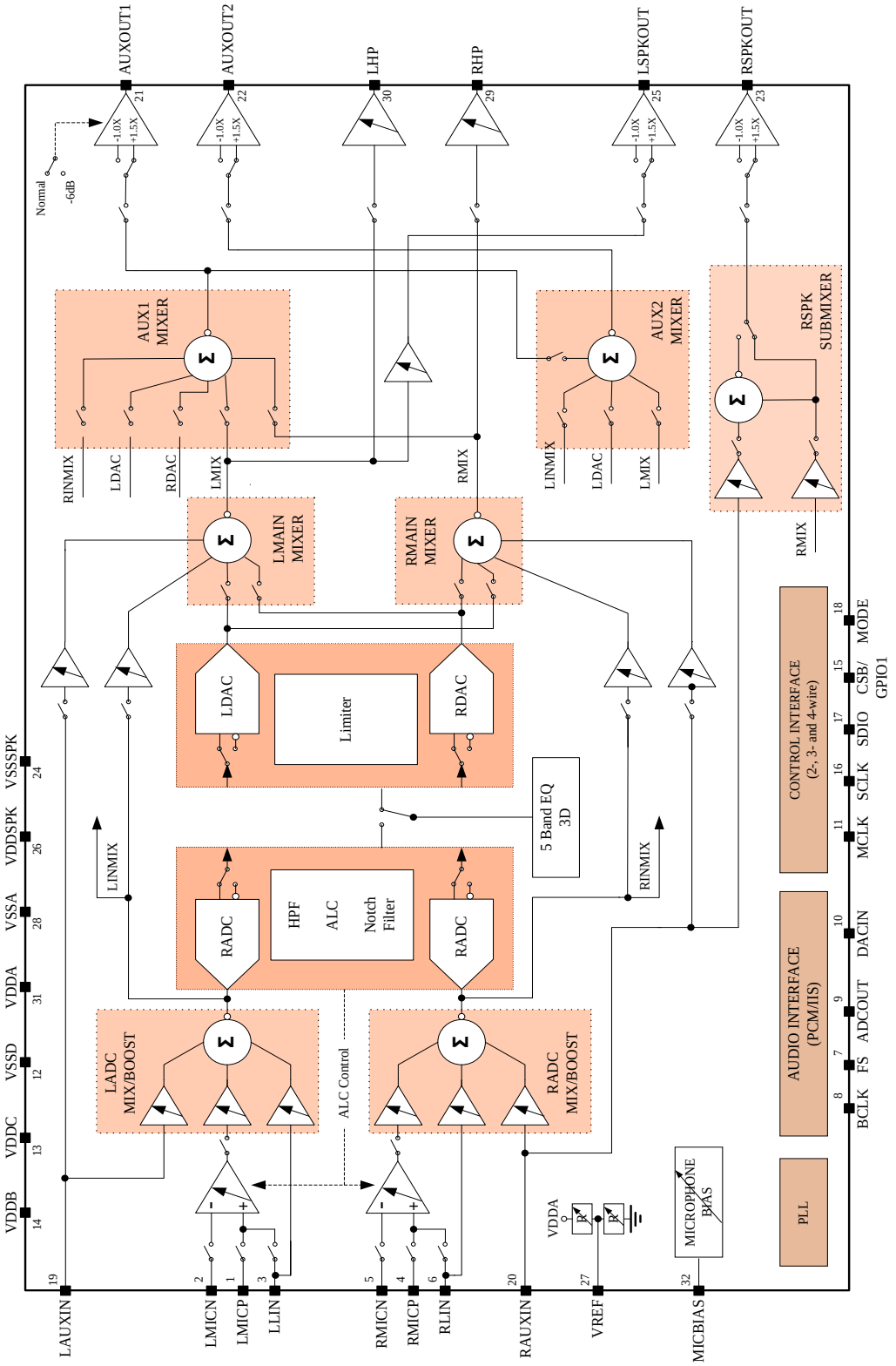


Figure 1: NAU8822ABlock Diagram

Electrical Characteristics

Conditions: VDDC = 1.8V, VDDA = VDDB = VDDSPK = 3.3V, MCLK = 12.88MHz, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data, 64X oversampling rate, unless otherwise stated.

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
Analog to Digital Converter (ADC)						
Full scale input signal [1]	V_{INFS}	PGABST = 0dB PGAGAIN = 0dB		1.0 0		Vrms dBV
Signal-to-noise ratio	SNR	Gain = 0dB, A-weighted	tbd	90		dB
Total harmonic distortion [2]	THD+N	Input = -3dB FS input		-80	tbd	dB
Channel separation		1kHz input signal		103		dB
Digital to Analog Converter (DAC) driving RHP / LHP with 10kΩ / 50pF load						
Full-scale output		Gain paths all at 0dB gain		VDDA / 3.3		V_{rms}
Signal-to-noise ratio	SNR	A-weighted	88	94		dB
Total harmonic distortion [2]	THD+N	R_L = 10kΩ; full-scale signal		-84	tbd	dB
Channel separation		1kHz input signal		96		dB
Output Mixers						
Maximum PGA gain into mixer				+6		dB
Minimum PGA gain into mixer				-15		dB
PGA gain step into mixer		Guaranteed monotonic		3		dB
Speaker Output (RSPKOUT / LSPKOUT with 8Ω bridge-tied-load)						
Full scale output [4]		SPKBST = 1		VCCSPK / 3.3		V_{rms}
		SPKBST = 0		(VCCSPK / 3.3) * 1.5		V_{rms}
Total harmonic distortion [2]	THD+N	P_o= 200mW, VDDSPK=3.3V		*63		dB
		P_o= 320mW, VDDSPK = 3.3V		-64		dB
		P_o= 860mW, VDDSPK = 5V		-60		dB
		P_o= 1000mW, VDDSPK = 5V		-36		dB
Signal-to-noise ratio	SNR	VDDSPK = 3.3V		91		dB
		VDDSPK=5V		90		dB
Power supply rejection ratio (50Hz - 22kHz)	PSRR	VDDSPK = 3.3V		81		dB
		VDDSPK = 5V (boost)		72		dB
Analog Outputs (RHP / LHP; RSPKOUT / LSPKOUT)						
Maximum programmable gain				+6		dB
Minimum programmable gain				-57		dB
Programmable gain step size		Guaranteed monotonic		1		dB
Mute attenuation		1kHz full scale signal		85		dB

Electrical Characteristics, cont'd.

Conditions: VDDC = 1.8V, VDDA = VDDB = VDDSPK = 3.3V, MCLK = 12.288MHz,
T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data, unless otherwise stated.

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
Headphone Output (RHP / LHP with 32Ω load)						
0dB full scale output voltage				AVDD / 3.3		V_{rms}
Signal-to-noise ratio	SNR	A-weighted		92		dB
Total harmonic distortion [2]	THD+N	R_L = 16Ω, P_o = 20mW, VDDA = 3.3V		80		dB
		R_L = 32Ω, P_o = 20mW, VDDA = 3.3V		85		dB
AUXOUT1 / AUXOUT2 with 10kΩ / 50pF load						
Full scale output		AUX1BST = 0 AUX2BST = 0		VDDSPK / 3.3		V_{rms}
		AUX1BST = 1 AUX2BST = 1		(VDDSPK / 3.3) * 1.5		V_{rms}
Signal-to-noise ratio	SNR			87		dB
Total harmonic distortion [2]	THD+N			-83		dB
Channel separation		1kHz signal		99		dB
Power supply rejection ratio (50Hz - 22kHz)	PSRR			53		dB
		VDDSPK = 5V (boost)		56		dB
Microphone Inputs (LMICP, LMICN, RMICP, RMICN, LLIN, RLIN) and Programmable Gain Amplifier (PGA)						
Full scale input signal [1]		PGABST = 0dB PGAGAIN = 0dB		1.0 0		Vrms dBV
Programmable gain			-12		35.25	dB
Programmable gain step size		Guaranteed Monotonic		0.75		dB
Mute Attenuation				120		dB
Input resistance		Inverting Input PGA Gain = 35.25dB PGA Gain = 0dB PGA Gain = -12dB **Non-inverting Input**		 1.6 47 75 94		 kΩ kΩ kΩ kΩ
Input capacitance				10		pF
PGA equivalent input noise		0 to 20kHz, Gain set to 35.25dB		120		μV
Input Boost Mixer						
Gain boost		Boost disabled Boost enabled		0 20		dB dB
Gain range LLIN / RLIN or LAUXIN / RAUXIN to boost/mixer			-12		6	dB
Gain step size to boost/mixer				3		dB
Auxiliary Analog Inputs (LAUXIN, RAUXIN)						
Full scale input signal [1]		Gain = 0dB		1.0 0		Vrms dBV
Input resistance		Aux direct-to-out path, only Input gain = +6.0dB Input gain = 0.0dB Input gain = -12dB		 20 40 159		 kΩ kΩ kΩ
Input capacitance				10		pF

Electrical Characteristics, cont'd.

Conditions: VDDC = 1.8V, VDDA = VDDB = VDDSPK = 3.3V, MCLK = 12.88MHz,
T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data, unless otherwise stated.

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
Automatic Level Control (ALC) & Limiter: ADC path only						
Target record level			-22.5		-1.5	dBFS
Programmable gain			-12		35.25	dB
Gain hold time [3]	t_{HOLD}	Doubles every gain step, with 16 steps total	0 / 2.67 / 5.33 / … / 43691			ms
Gain ramp-up (decay) [3]	t_{DCY}	ALC Mode ALC = 0	4 / 8 / 16 / … / 4096			ms
		Limiter Mode ALC = 1	1 / 2 / 4 / … / 1024			ms
Gain ramp-down (attack) [3]	t_{ATK}	ALC Mode ALC = 0	1 / 2 / 4 / … / 1024			ms
		Limiter Mode ALC = 1	0.25 / 0.5 / 1 / … / 128			ms
Mute Attenuation				120		dB
Microphone Bias						
Bias voltage	$V_{MICBIAS}$	See Figure 3	0.50, 0.60,0.65, 0.70, 0.75, 0.85, or 0.90			VDDA VDDA
Bias current source	$I_{MICBIAS}$			3		mA
Output noise voltage	V_n	1kHz to 20kHz		14		nV/√Hz
Digital Input/Output						
Input HIGH level	V_{IL}		0.7 * VDDC			V
Input LOW level	V_{IH}				0.3 * VDDC	V
Output HIGH level	V_{OH}	I_{Load} = 1mA	0.9 * VDDC			V
Output LOW level	V_{OL}	I_{Load} = -1mA			0.1 * VDDC	V
Input capacitance				10		pF

Notes

1. Full Scale is relative to the magnitude of VDDA and can be calculated as FS = VDDA/3.3.
2. Distortion is measured in the standard way as the combined quantity of distortion products plus noise. The signal level for distortion measurements is at 3dB below full scale, unless otherwise noted.
3. Time values scale proportionally with MCLK. Complete descriptions and definitions for these values are contained in the detailed descriptions of the ALC functionality.
4. With default register settings, SPKVDD should be 1.5xVDDA (but not exceeding maximum recommended operating voltage)to optimize available dynamic range in the AUXOUT1 and AUXOUT2 line output stages. OutputDC bias level is optimized for SPKVDD = 5.0Vdc (boost mode) and VDDA = 3.3Vdc.
5. Unused analog input pins should be left as no-connection.
6. Unused digital input pins should be tied to ground.

Absolute Maximum Ratings

Condition	Min	Max	Units
VDDB, VDDC, VDDA supply voltages	-0.3	+3.61	V
VDDSPK supply voltage (default register configuration)	-0.3	+5.80	V
VDDSPK supply voltage (optional low voltage configuration)	-0.3	+3.61	V
Core Digital Input Voltage range	VSSD – 0.3	VDDC + 0.30	V
Buffer Digital Input Voltage range	VSSD – 0.3	VDDB + 0.30	V
Analog Input Voltage range	VSSA – 0.3	VDDA + 0.30	V
Industrial operating temperature	-40	+85	°C
Storage temperature range	-65	+150	°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely influence product reliability and result in failures not covered by warranty.

Operating Conditions

Condition	Symbol	Min	Typical	Max	Units
Digital supply range (Core)	VDDC	1.65		3.60	V
Digital supply range (Buffer)	VDDB	1.65		3.60	V
Analog supply range	VDDA	2.50		3.60	V
Speaker supply (SPKBST=0)	VDDSPK	2.50		5.50	V
Speaker supply (SPKBST=1)	VDDSPK	2.50		5.50	V
Ground	VSSD VSSA VSSSPK		0		V

1. VDDA must be ≥ VDDC.
2. VDDB must be ≥ VDDC.

Table of Contents

1 General Description

The NAU8822A delivers reduced out-of-band noise energy, improved ALC and DSP signal processing, read-out capability of real-time signal level, readout of DSP status, and added controls for industry leading pop/click noise management. Additionally, handling of settings for 5-volt and 3-volt operation are simplified, and all registers unique to Nuvoton are moved to higher addresses. This makes the part a direct hardware and software drop-in replacement for common industry parts.

The NAU8822A is a stereo part with identical left and right channels that share common support elements. Additionally, the right channel auxiliary output path includes a dedicated submixer that supports mixing the right auxiliary input directly into the right speaker output driver. This enables the right speaker channel to output audio that is not present on any other output.

1.1.1 Analog Inputs

All inputs, except for the wide range programmable amplifier (PGA), have available analog input gain conditioning of -15dB through +6dB in 3dB steps. All inputs also have individual muting functions with excellent channel isolation and off-isolation from all outputs. All inputs are suitable for full quality, high bandwidth signals.

Each of the left-right stereo channels includes a low noise differential PGA amplifier, programmable for high-gain input. This may be used for a microphone level through line level source. Gain may be set from +35.25db through -12dB at the analog difference-amplifier type programmable amplifier input stage. A separate additional 20dB analog gain is available on this input path, between the PGA output and ADC mixer input. The output of the ADC mixer may be routed to the ADC and/or analog bypass to the analog output sections.

Each channel also has a line level input. This input may be routed to the input PGA, and/or directly to the ADC input mixer.

Each channel has a separate additional auxiliary input. This is a line level input which may be routed the ADC input mixer and/or directly to the analog output mixers.

1.1.2 Analog Outputs

There are six high current analog audio outputs. These are very flexible outputs that can be used individually or in stereo pairs for a wide range of end uses. However, these outputs are optimized for specific functions and are described in this section using the functional names that are applicable to those optimized functions.

Each output receives its signal source from built-in analog output mixers. These mixers enable a wide range of signal combinations, including muting of all sources. Additionally, each output has a programmable gain function, output mute function, and output disable function.

The RHP and LHP headphone outputs are optimized for driving a stereo pair of headphones, and are powered from the main analog voltage supply rail, VDDA. These outputs may be coupled using traditional DC blocking series capacitors. Alternatively, these may be configured in a no-capacitor DC coupled design using a virtual ground at ½ VDDA provided by an AUXOUT analog output operating in the non-boost output mode.

The AUXOUT1 and AUXOUT2 analog outputs are powered from the VDDSPK supply rail and VSSSPK ground return path. The supply rail may be the same as VDDA, or may be a separate voltage up to 5.5Vdc. This higher voltage enables these outputs to have an increased output voltage range and greater output power capability.

The RSPKOUT and LSPKOUT loudspeaker outputs are powered from the VDDSPK power supply rail and VSSGND ground return path. LSPKOUT receives its audio signal via an additional submixer. This submixer supports combining a traditional alert sound (from the RAUXIN input) with the right channel headphone output mixer signal. This submixer also provides the signal invert function that is necessary for the normal BTL (Bridge Tied Load) configuration used to drive a high power external loudspeaker. Alternatively, each loudspeaker output may be used individually as a separate high current analog output driver.

A programmable low-noise MICBIAS microphone bias supply output is included. This is suitable for both conventional electret (ECM) type microphone, and to power the newer MEMS all-silicon type microphones.

1.1.3 ADC, DAC, and Digital Signal Processing

Each left and right channel has an independent high quality ADC and DAC associated with it. These are high performance, 24-bit delta-sigma converters that are suitable for a very wide range of applications.

The ADC and DAC functions are each individually supported by powerful analog mixing and routing. The ADC output may be routed to the digital output path and/or to the input of the DAC in a digital pass-through mode. The ADC and DAC blocks are also supported by advanced digital signal processing subsystems that enable a very wide range of programmable signal conditioning and signal optimizing functions. All digital processing is with 24-bit precision, as to minimize processing artifacts and maximize the audio dynamic range supported by the NAU8822A.

The ADCs are supported by a wide range, mixed-mode Automatic Level Control (ALC), a high pass filter, and a notch filter. All of these features are optional and highly programmable. The high pass filter function is intended for DC-blocking or low frequency noise reduction, such as to reduce unwanted ambient noise or "wind noise" on a microphone input. The notch filter may be programmed to greatly reduce a specific frequency band or frequency, such as a 50Hz, 60Hz, or 217Hz unwanted noise.

The DACs are supported by a programmable limiter/DRC (Dynamic Range Compressor). This is useful to optimize the output level for various applications and for use with small loudspeakers. This is an optional feature that may be programmed to limit the maximum output level and/or boost an output level that is too small.

Digital signal processing is also provided for a 3D Audio Enhancement function, and for a 5-Band Equalizer. These features are optional, and are programmable over wide ranges. This pair ofdigital processing features may be applied jointly to either the ADC audio path or to the DAC audio path, but not to both paths simultaneously.

1.1.4 Realtime Signal Level Readout and DSP Status

In addition to general read-back ability of all its registers, the NAU8822A includes powerful capacities to readback signal related DSP information not possible with almost any other CODEC. In conjunction with the ALC, the software by means of the readback function can determine the realtime signal level at the inputs, as well as the realtime actual gain setting being used by the ALC. Additionally, other signal related information can also be determined, such as the Noise Gate on/off status and Automute/Softmute function status. These greatly enhance both the ability to optimize software and to enhance dynamic end product functionality.

1.1.5 Digital Interfaces

Command and control of the device is accomplished using a 2-wire/3-wire/4-wire serial control interface. This is a simple, but highly flexible interface that is compatible with many commonly used command and control serial data protocols and host drivers.

Digital audio input/output data streams are transferred to and from the device separately from command and control. The digital audio data interface supports either I2S or PCM audio data protocols, and is compatible with commonly used industry standard devices that follow either of these two serial data formats.

1.1.6 Clock Requirements

The clocking signals required for the audio signal processing, audio data I/O, and control logic may be provided externally, or by optional operation of a built-in PLL (Phase Locked Loop).

The PLL is provided as a low cost, zero external component count optional method to generate required clocks in almost any system. The PLL is a fractional-N divider type design, which enables generating accurate desired audio sample rates derived from a very wide range of commonly available system clocks.

The frequency of the system clock provided as the PLL reference frequency may be any stable frequency in the range between 8MHz and 33MHz. Because the fractional-N multiplication factor is a very high precision 24-bit value, any desired sample rate supported by the NAU8822A can be generated with very high accuracy, typically limited by the accuracy of the external reference frequency. Reference clocks and sample rates outside of these ranges are also possible, but may involve performance tradeoffs and increased design verification.

2 Power Supply

This device has been designed to operate reliably using a wide range of power supply conditions and power-on/power-off sequences. There are no special requirements for the sequence or rate at which the various power supply pins change. Any supply can rise or fall at any time without harm to the device. However, pops and clicks may result from some sequences. Optimum handling of hardware and software power-on and power-off sequencing is described in more detail in the Applications section of this document.

2.1.1 Power-On Reset

The NAU8822A does not have an external reset pin. The device reset function is automatically generated internally when power supplies are too low for reliable operation. The internal reset is generated any time that either VDDA or VDDC is lower than is required for reliable maintenance of internal logic conditions. The reset threshold voltage for VDDA and VDDC is approximately 0.5Vdc. If both VDDA and VDDC are being reduced at the same time, the threshold voltage may be slightly lower. Note that these are much lower voltages than are required for normal operation of the chip. These values are mentioned here as general guidance as to overall system design.

If either VDDA or VDDC is below its respective threshold voltage, an internal reset condition is asserted. During this time, all registers and controls are set to the hardware determined initial conditions. Software access during this time will be ignored, and any expected actions from software activity will be invalid.

When both VDDA and VDDC reach a value above their respective thresholds, an internal reset pulse is generated which extends the reset condition for an additional time. The duration of this extended reset time is approximately 50 microseconds, but not longer than 100 microseconds. The reset condition remains asserted during this time. If either VDDA or VDDC at any time becomes lower than its respective threshold voltage, a new reset condition will result. The reset condition will continue until both VDDA and VDDC again higher than their respective thresholds. After VDDA and VDDC are again both greater than their respective threshold voltage, a new reset pulse will be generated, which again will extend the reset condition for not longer than an additional 100 microseconds.

2.1.2 Power Related Software Considerations

There is no direct way for software to determine that the device is actively held in a reset condition. If there is a possibility that software could be accessing the device sooner than 100 microseconds after the VDDA and VDDC supplies are valid, the reset condition can be determined indirectly. This is accomplished by writing a value to any register other than register 0x00, with that value being different than the power-on reset initial values. The optimum choice of register for this purpose may be dependent on the system design, and it is recommended the system engineer choose the register and register test bit for this purpose. After writing the value, software will then read back the same register. When the register test bit reads back as the new value, instead of the power-on reset initial value, software can reliably determine that the reset condition has ended.

Although it is not required, it is strongly recommended that a Software Reset command should be issued after power-on and after the power-on reset condition is ended. This will help insure reliable operation under every power sequencing condition that could occur.

If there is any possibility that VDDA or VDDC could be unreliable during system operation, software may be designed to monitor whether a power-on reset condition has happened. This can be accomplished by writing a test bit to a register that is different from the power-on initial conditions. This test bit should be a bit that is never used for any other reason, and does not affect desired operation in any way. Then, software at any time can read this bit to determine if a power-on reset condition has occurred. If this bit ever reads back other than the test value, then software can reliably know that a power-on reset event has occurred. Software can subsequently re-initialize the device and the system as required by the system design.

2.1.3 Software Reset

All chip registers can be reset to power-on default conditions by writing any value to register 0, using any of the control modes. Writing valid data to any other register disables the reset, but all registers need to have the correct operating data written. See the applications section on powering NAU8822A up for information on avoiding pops and clicks after a software reset.

3 Input Path Detailed Descriptions

The NAU8822Aprovides multiple inputs to acquire and process audio signals from microphones or other sources with high fidelity and flexibility. There are left and right input paths, each with three input pins, which can be used to capture signals from single-ended, differential or dual-differential microphones. These input channels each include a programmable gain amplifier (PGA). The outputs of the PGAs, plus two additional auxiliary inputs, are then connected to the input boost/mix stages for maximum flexibility handling various signal sources.

All inputs are maintained at a DC bias at approximately ½ of the AVDD supply voltage. Connections to these inputs should be AC-coupled by means of DC blocking capacitors suitable for the device application.

Differential microphone input (MICN & MICP pins) and Programmable Gain Amplifier

The NAU8822A features a low-noise, high common mode rejection ratio (CMRR), differential microphone input pair, MICP and MICN, which are connected to a PGA gain stage. The differential input structure is essential in noisy digital systems where amplification of low-amplitude analog signals is necessary such as in portable digital media devices and cell phones. Differential inputs very useful to reduce ground noise in systems in which there are ground voltage differences between different chips and other components. When properly implemented, the differential input architecture offers an improved power-supply rejection ratio (PSRR) and higher ground noise immunity.

3.1 Programmable Gain Amplifier (PGA)

Each PGA supports three possible inputs, MICP, MICN, and LIN. These are the microphone differential pair and a separate line level input. The PGA has a gain range of -12dB through +35.25dB in evenly spaced decibel increments of 0.75dB. Operation of the PGA is subject to control by the following registers:

R2 Power management controls for the left and right PGA
R2 Power management controls for ADC Mix/Boost (must be “on” for any PGA path to function)
R7 Zero crossing timeout control
R32 Automatic Level Control (ALC) for the left and right PGA
R44 Input selection options for the left and right PGA
R45 Volume (gain), mute, update bit, and zero crossing control for the left PGA
R46 Volume (gain), mute, update bit, and zero crossing control for the right PGA

Important: The R45 and R46 update bits are write-only bits. The primary intended purpose of the update bit is to enable simultaneous changes to both the left and right PGA volume values, even though these values must be written sequentially. When there is a write operation to either R45 or R46 volume settings, but the update bit is not set (value = 0), the new volume setting is stored as pending for the future, but does not go into effect. When there is a write operation to either R45 or R46 and the update bit is set (value = 1), then the new value in the register being written is immediately put into effect, and any pending value in the other PGA volume register is put into effect at the same time.

Note: If the ALC automatic level control is enabled, the function of the ALC is to automatically adjust the R45 or R46 volume setting. If ALC is enabled for the left or right, or both channels, then software should avoid changing the volume setting for the affected channel or channels. The reason for this is to avoid unexpected volume changes caused by competition between the ALC and the direct software control of the volume setting.

Zero-Crossing controls are implemented to suppress clicking sounds that may occur when volume setting changes take place while an audio input signal is active. When the zero crossing function is enabled (logic = 1), any volume change for the affected channel will not take place until the audio input signal passes through the zero point in its peak-to-peak swing. This prevents any instantaneous voltage change to the audio signal caused by volume setting changes. If the zero crossing function is disabled (logic = 0), volume changes take place instantly on condition of the Update Bit, but without regard to the instantaneous voltage level of the affected audio input signal.

The R7 zero crossing timeout control is an additional feature to limit the amount of time that a volume change to the PGA is delayed pending a zero crossing event. If the input signal is such that there are no zero crossing events, and the timeout control is enabled (level = 1), any new volume setting to either PGA will automatically be put into effect after between 2.5 and 3.5 periods of the Slow Timer Clock (see description under “Miscellaneous Functions”).

3.1.1 Zero Crossing Example

This drawing shows in a graphical form the problem and benefits of using the zero crossing feature. There is a major audible improvement as a result of using the zero crossing feature.

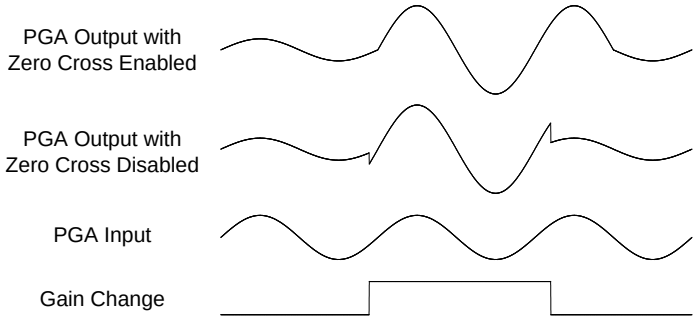


Figure 2: Zero Crossing Gain Update Operation

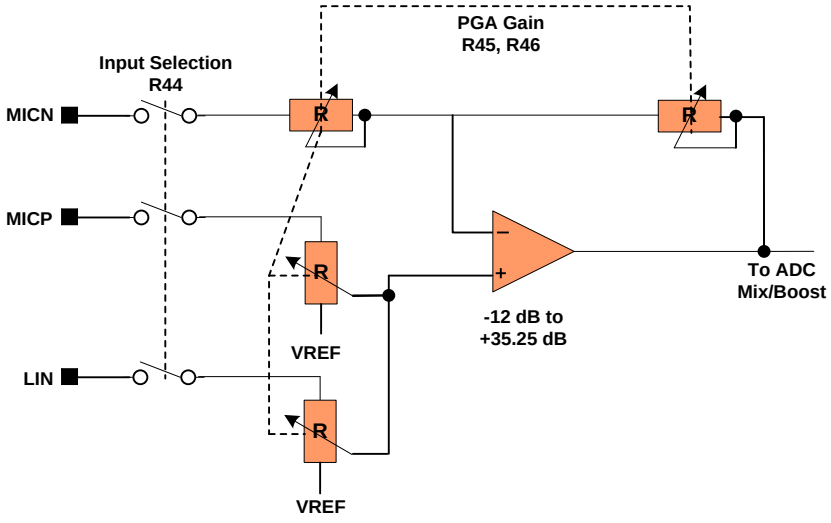


Figure 3: PGA Input Structure Simplified Schematic

3.2 Positive Microphone Input (MICP)

The positive (non-inverting) microphone input (MICP) can be used separately, or as part of a differential input configuration. This input pin connects to the positive (non-inverting) terminal of the PGA amplifier under control of register R44. When the R44 associated control bit is set (logic = 1), a switch connects MICP to the PGA input. When the associated control bit is not set (logic = 0), the MICP pin is connected to a resistor of approximately 30kΩ which is tied to VREF. The purpose of the tie to VREF is to reduce any pop or click sound by keeping the DC level of the MICP pin close to VREF at all times.

Note: If the MICP signal is not used differentially with MICN, the PGA gain values will be valid only if the MICN pin is terminated to a low impedance signal point. This termination should normally be an AC coupled path to signal ground.

This input impedance is constant regardless of the gain value. The nominal input impedance for this input is given by the following table. Impedance for specific gain values not listed in this table can be estimated through interpolation between listed values.

Nominal Input Impedance	Gain (dB)	Impedance (kΩ)
LMICP & RMICP to non-inverting PGA input or LLIN & RLIN to non-inverting PGA input	-12	94
	-9	94
	-6	94
	-3	94
	0	94
	3	94
	6	94
	9	94
	12	94
	18	94
	30	94
	35.25	94

Table 1: Microphone and Line Non-Inverting Input Impedances

3.3 Negative Microphone Input (MICN)

The negative(inverting) microphone input (MICN) can be used separately, or as part of a differential input configuration. This input pin connects to the negative (inverting) terminal of the PGA amplifier under control of register R44. When the R44 associated control bit is set (logic = 1), a switch connects MICP to the PGA input. When the associated control bit is not set (logic = 0), the MICN pin is connected to a resistor of approximately 30kΩ which is tied to VREF. The purpose of the tie to VREF is to reduce any pop or click sound by keeping the DC level of the MICN pin close to VREF at all times.

It is important for a system designer to know that the MICN input impedance varies as a function of the selected PGA gain. This is normal and expected for a difference amplifier type topology. The nominal resistive impedance values for this input over the possible gain range are given by the following table. Impedance for specific gain values not listed in this table can be estimated through interpolation between listed values.

Nominal Input Impedance	Gain (dB)	Impedance (kΩ)
LMICN or RMICN to inverting PGA input	-12	75
	-9	69
	-6	63
	-3	55
	0	47
	3	39
	6	31
	9	25
	12	19
	18	11
	30	2.9
	35.25	1.6

Table 2: Microphone Inverting Input Impedances

System designers should also note that at the highest gain values, the input impedance is relatively low. For most inputs, the best strategy if higher gain values are needed is to use the input PGA in combination with the +20dB gain boost available on the PGA Mix/Boost stage that immediately follows the PGA output. A good guideline is to use the PGA gain for up to around 20dB of gain. If more gain than this is required and the lower input impedance of the PGA at high gains is a problem, a combination of the PGA and boost stage should be used. In this type of

combined gain configuration, it is preferred to have at least 6dB gain at the PGA input stage to benefit from the PGA low noise characteristics.

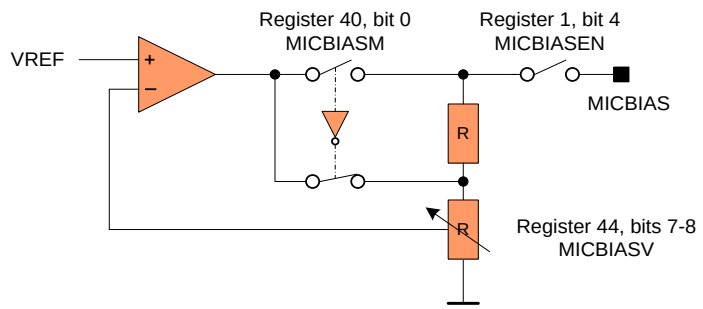
3.4 Microphone biasing

The MICBIAS pin provides a low-noise microphone DC bias voltage as may be required for operation of an external microphone. This built-in feature can typically provide up to 3mA of microphone bias current. This DC bias voltage is suitable for powering either traditional ECM (electret) type microphones, or for MEMS types microphones with an independent power supply pin.

Seven different bias voltages are available for optimum system performance, depending on the specific application. The microphone bias pin normally requires an external filtering capacitor as shown on the schematic in the Application section. The microphone bias function is controlled by the following registers:

R1 Power control for MICBIAS feature (enabled when bit 4 = 1)
R58 Optional low-noise mode and different bias voltage levels (enabled when bit 0 = 1)
R44 Primary MICBIAS voltage selection

The low-noise feature results in greatly reduced noise in the external MICBIAS voltage by placing a resistor of approximately 200-ohms in series with the output pin. This creates a low pass filter in conjunction with the external MICBIAS filter capacitor, but without any additional external components. The low noise feature is enabled when the mode control bit 0 in register R58 is set (level = 1)



Register 44, Bits 7-8	Register 58, Bit 0	Microphone Bias Voltage
00	0	0.90 * VDDA
01	0	0.65 * VDDA
10	0	0.75 * VDDA
11	0	0.50 * VDDA
00	1	0.85 * VDDA
01	1	0.60 * VDDA
10	1	0.70 * VDDA
11	1	0.50 * VDDA

Figure 4: Microphone Bias Generator

3.5 Line/Aux Input Impedance and Variable Gain Stage Topology

Except for the input PGAs, other variable gain stages are implemented similarly to the simplified schematic shown here. The gain value changes affect input impedance in the ranges detailed in the description of each type of input path. If a path is in the "not selected" condition, then the input impedance will be in a high impedance condition. If an external input pin is not used anywhere in the system, it will be coupled to a DC tie-off of approximately 30kΩ coupled to VREF. The unused input/output tie-off function is explained in more detail in the Application Information section of this document.

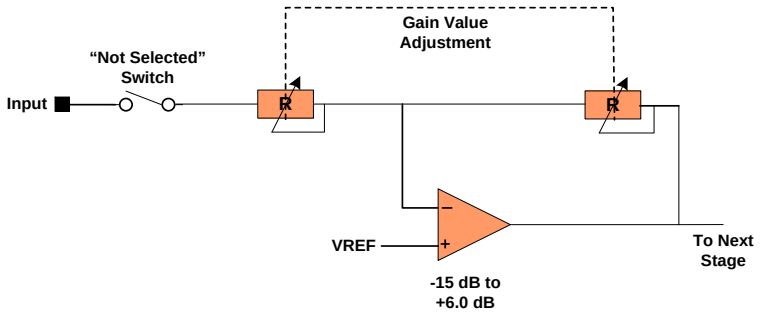


Figure 5: Variable Gain Stage Simplified Schematic

The input impedance presented to these inputs depends on the input routing choices and gain values. If an input is routed to more than one internal input node, then the effective input impedance will be the parallel combination of the impedance of the multiple nodes that are used. The impedance looking into the PGA non-inverting input is constant as listed in the section discussing the microphone input PGAs. The nominal resistive input impedances looking into the ADC Mix/Boost input inputs are listed in the following table:

Inputs	Gain (dB)	Impedance (kΩ)
LAUXIN & RAUXIN to L/RADC MIX/BOOST amp or LLIN & RLIN to L/RADC MIX/BOOST amp	Not Selected	High-Z
	-12	159
	-9	113
	-6	80
	-3	57
	0	40
	3	28
	6	20

Table 3: MIX/BOOST Amp Impedances

The nominal resistive input impedances presented to signal pins that are directly routed to an output mixer are listed in the following table. If an input is connected to other active nodes, then this value is in parallel with the resistive input impedance of any such other node.

Inputs	Gain (dB)	Impedance (kΩ)
LAUXIN & RAUXIN to bypass amp Or RAUXIN to RSPK SUBMIXER amp	-15	225
	-12	159
	-9	113
	-6	80
	-3	57
	0	40
	3	28
	6	20

Table 4:Bypass Amp and RSPK SUBMIXER Input Impedances

3.6 Left and Right Line Inputs (LLIN and RLIN)

A third possible input to the left or right PGA is an optionalassociated LIN left or right line level input. These inputs may be routed to the PGA non-inverting input, and/or connect directly to the ADC Mixer/Boost stage. If routed to the PGA, this signal is processed as an alternate pin for the MICPsignal. LIN may be received differentially in relation to the MICN pin and has available the same gain range as for MICP. As in the operational case of using theMICP input, the MICN input must have a low impedance path to signal ground, so that the gain values chosen in the PGA are valid.

Note: It not recommended that both the LIN line input path to the PGA and the MICP path to the PGA be enabled at the same time. This will cause the differential gain to be unbalanced, and result in poor common mode rejection. Also, this will result in the LIN and MICP signals being connected together through internal chip resistors.

The line input pins, may alternatively be configured to operate as a GPIO (General Purpose Input/Output) logic input pin. This intended purpose is static logic voltage level sensing to determine if a headset is present or not as part of a physical detection of a possible external headset. Only one GPIO pin at any one time can be assigned for this purpose.

Registers that affect operation of the LLIN and RLIN inputs are:

R2 ADC Mix/Boost power control (must be “on” for any LIN path to function)
R9 GPIO selection for headset detect function
R44 PGA input selection control bits
If selected, all other PGA control registers (see PGA description)
R47 Left line input ADC Mix/Boost volume and mute (bits 4, 5, and 6)
R48 Right line input ADC Mix/Boost volume and mute (bits 4, 5, and 6)

3.7 Auxiliary inputs (LAUXIN, RAUXIN)

The left and right channels each have an additional input that is separate from the programmable amplifier stage. These are the left and right auxiliary inputs, LAUXIN and RAUXIN. These inputs may be routed to either or both the associated ADC Mix/Boost stage, or the associated LCH MIX or RCH MIX output mixer.

The RAUXIN input may additionally be routed to the Right Speaker Submixer in the analog output section. This path enables a sound to be output from the LSPKOUT speaker output, but without being audible anywhere else in the system. One purpose of this path is to support a traditional “beep” sound, such as from a microprocessor toggle bit. This is a historical application scenario which is now uncommon.

The auxiliary inputs are affected by the following registers:

ADC Mix/Boost if used (see ADC Mix/Boost section)
LCH MIXER or RCH MIXER if used (see output mixer section)
BEEP MIXER if used (see Beep Mixer section)
Note: no power control registers affect only the auxiliary inputs

The input impedance presented to these inputs depends on the input routing choices and gain values. If an input is routed to more than one internal input node, then the effective input impedance will be the parallel combination of the impedance of the multiple nodes that are used. The input impedances presented to these inputs are the same as those listed for the LLIN and RLIN inputs.

3.8 ADC Mix/Boost Stage

The left and right channels each have an independent ADC Mix/Boost stage. Most analog input signals must pass through the ADC Mix/Boost stage before use anywhere else in this device. The only analog inputs that can completely bypass the ADC Mix/Boost stage are the LAUXIN and RAUXIN auxiliary inputs.

The ADC mixer stage has three inputs, AUX, LIN, and PGA. The AUX input is for the associated auxiliary input, and the LIN is for the associated line input. The PGA input is an internal connection to the associated programmable gain amplifier servicing the microphone and line inputs.

All three inputs to the ADC Mix/Boost stage can be independently muted, and all three inputs have independent gain controls. The AUX and LIN inputs have an available gain range of -12dB through +6dB in 3dB steps. The PGA input path has a choice of 0dB or 20dB of gain in addition to the gain in the PGA.

Registers that affect the ADC Mix/Boot stage are:

R2 Power control for left and right channels
R45 mute function for left channel PGA (bit 6 = 0 = muted condition)
R46 mute function for right channel PGA (bit 6 = 0 = muted condition)
R47 gain and mute control for left channel AUX and LIN
R48 gain and mute control for right channel AUX and LIN

3.9 Input Limiter / Automatic Level Control (ALC)

The input section of the NAU8822A is supported by additional combined digital and analog functionality which implement an Automatic Level Control (ALC) function. This can be very useful to automatically manage the analog input gain to optimize the signal level at the output of the programmable amplifier. The ALC can automatically amplify input signals that are too small, or decrease the amplitude if the signals are too loud. This system also helps to prevent clipping (overdrive) at the input of the ADC while maximizing the full dynamic range of the ADC.

The ALC may be operated in the normal mode just described, on in a special limiter mode of operation. The limiter mode is a faster mode of operation, the primary purpose of which is to limit too-loud signals. The limiter mode of operation is described after this section which provides details on the normal mode of operation.

The functional block architecture for the ALC is shown below. The ALC monitors the output of the ADC, measured after the digital decimator. The ADC output is fed into a peak detector, which updates the measured peak value whenever the absolute value of the input signal is higher than the current measured peak. The measured peak gradually decays to zero unless a new peak is detected, allowing for an accurate measurement of the signal envelope. The peak value is used by a logic algorithm to determine whether the PGA input gain should be increased, decreased, or remain the same.

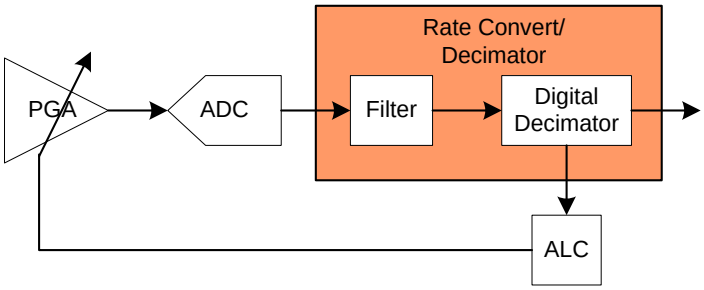


Figure 6: ALC Block Diagram

3.9.1 Normal Mode Example Operation

Immediately following is a simple example of the ALC operation. In the steady state at the beginning of the example time sequence, the PGA gain is at a steady value which results in the desired output level from the ADC. When the input signal suddenly becomes louder, the ALC reduces volume at a register determined rate and step size. This continues until the output level of the ADC is again at the desired target level. When the input signal suddenly becomes quiet, the ALC increases volume at a register determined rate and step size. When the output level from the ADC again reaches the target level, and now the input remains at a constant level, the ALC remains in a steady state.

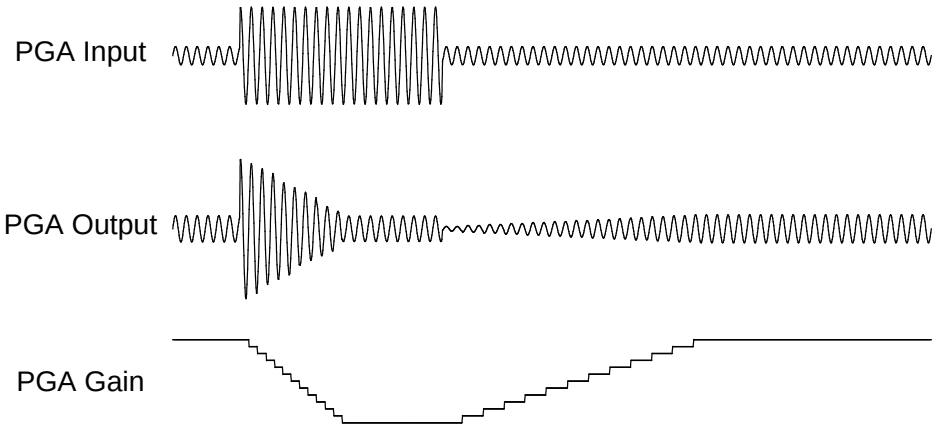


Figure 7: ALC Normal Mode Operation

3.9.2 ALC Parameter Definitions

Automatic level and volume control features are complex and have difficult to understand traditional names for many features and controls. This section defines some terms so that the explanations of this subsystem are more clear.

ALC Maximum Gain: Register 32 (ALCMXGAIN) This sets the maximum allowed gain in the PGA during normal mode ALC operation. In the Limiter mode of ALC operation, the ALCMXGAIN value is not used. In the Limiter mode, the maximum gain allowed for the PGA is set equal to the pre-existing PGA gain value that was in effect at the moment in time that the Limiter mode is enabled.

ALC Minimum Gain: Register 32 (ALCMNGAIN) This sets the minimum allowed gain in the PGA during all modes of ALC operation. This is useful to keep the AGC operating range close to the desired range for a given application scenario.

ALC Target Value: Register 33 (ALCSL) Determines the value used by the ALC logic decisions comparing this fixed value with the output of the ADC. This value is expressed as a fraction of Full Scale (FS) output from the ADC. Depending on the logic conditions, the output value used in the comparison may be either the instantaneous value of the ADC, or otherwise a time weighted average of the ADC peak output level.

ALC Attack Time: Register 34 (ALCATK)Attack time refers to how quickly a system responds to an increasing volume level that is greater than some defined threshold. Typically, attack time is much faster than decay time. In the NAU8822A, when the absolute value of the ADC output exceeds the ALC Target Value, the PGA gain will be reduced at a step size and rate determined by this parameter. When the peak ADC output is at least 1.5dB lower than the ALC Target Value, the stepped gain reduction will halt.

ALC Decay Time: Register 34 (ALCDCY) Decay time refers to how quickly a system responds to a decreasing volume level. Typically, decay time is much slower than attack time. When the ADC output level is below the ALC Target value by at least 1.5dB, the PGA gain will increase at a rate determined by this parameter. The decay time constant is determined by the setting in register 34, bits 4 to 7 (ALCDCY), which sets the delay between increases in gain. In Limiter mode, the time constants are faster than in ALC mode. (See Detailed Register Map.)

ALC Hold Time Register 33 (ALCHLD) Hold time refers to a duration of time when no action is taken. This is typically to avoid undesirable sounds that can happen when an ALC responds too quickly to a changing input signal. The use and amount of hold time is very application specific. In the NAU8822A, the hold time value is the duration of time that the ADC output peak value must be less than the target value before there is an actual gain increase.

3.10 ALCPeak Limiter Function

To reduce clipping and other bad audio effects, all ALC modes include a peak limiter function. This implements an emergency PGA gain reduction when the ADC output level exceeds a built-in maximum value. When the ADC output exceeds 87.5% of full scale, the ALC block ramps down the PGA gain at the maximum ALC Attack Time rate, regardless of the mode and attack rate settings, until the ADC output level has been reduced below the emergency limit threshold. This limits ADC clipping if there is a sudden increase in the input signal level.

3.10.1 ALC Normal Mode Example Using ALC Hold Time Feature

Input signals with different characteristics (e.g., voice vs. music) may require different settings for this parameter for optimum performance. Increasing the ALC hold time prevents the ALC from reacting too quickly to brief periods of silence such as those that may appear in music recordings; having a shorter hold time, may be useful in voice applications where a faster reaction time helps to adjust the volume setting for speakers with different volumes. The waveform below shows the operation of the ALCHLD parameter.

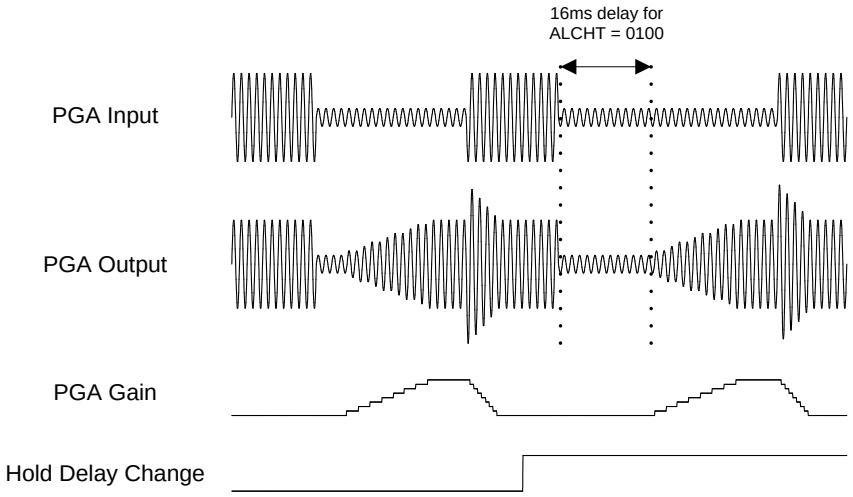


Figure 8: ALC Hold Delay Change

3.11 Noise Gate (Normal Mode Only)

A noise gate threshold prevents ALC amplification of noise when there is no input signal, or no signal above an expected background noise level. The noise gate is enabled by setting register 35, bit 3 (NGEN), HIGH, and the threshold level is set in register 35, bits 0 to 2 (NGTH). This does not remove noise from the signal; when there is no signal or a very quiet signal (pause) composed mostly of noise, the ALC holds the gain constant instead of amplifying the signal towards the target threshold. The NAU8822A accomplishes this by comparing the input signal level against the noise gate threshold. The noise gate only operates in conjunction with the ALC and only in Normal mode. The noise gate is asserted when:

Equation 1: (Signal at ADC – PGA gain – MIC Boost gain) < NGTH (Noise Gate Threshold Level)

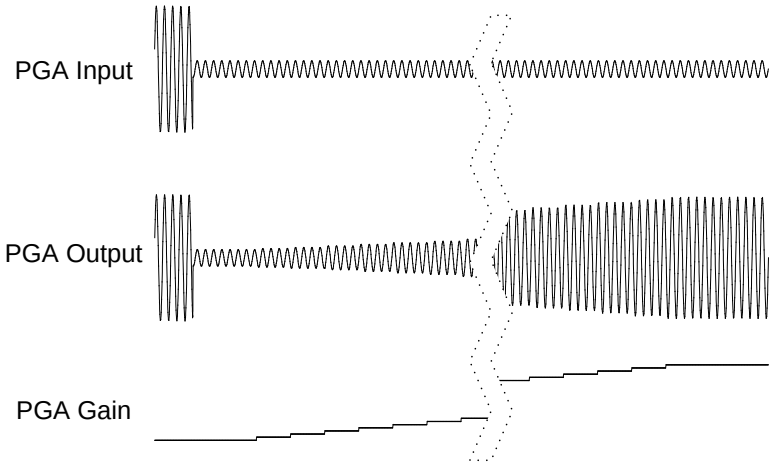


Figure 9: ALC Operation Without Noise Gate

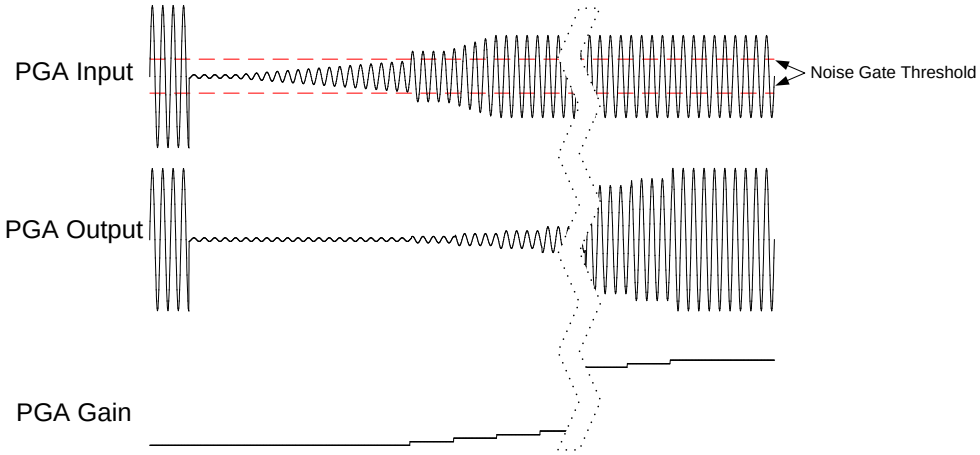
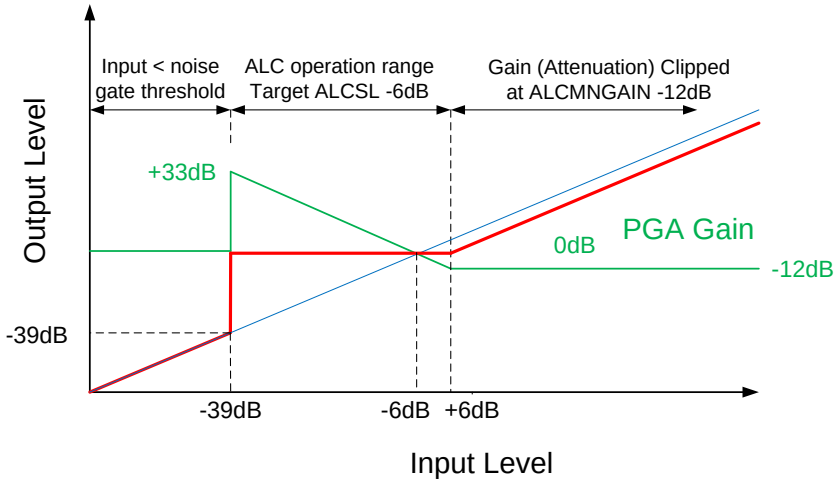


Figure 10: Noise Gate Operation

3.12 ALC Example with ALC Min/Max Limits and Noise Gate Operation

The drawing below shows the effects of ALC operation over the full scale signal range. The drawing is color coded to be more clear as follows:

Blue Original Input signal (linear line from zero to maximum)
Green PGA gain value over time (inverse to signal in target range)
Red Output signal (held to a constant value in target range)



Register	Bits	Name	Value	Description
32	7-8	ALCSEL	11	ALC enabled both channels
32	3-5	ALCMAXGAIN	111	Max ALC gain @ 35.25dB
32	0-2	ALCMINGAIN	000	Min ALC gain @ -12dB
33	0-3	ALCLVL	1011	Target ALC gain @ -6dBFS
35	3	NGEN	1	Noise gate enabled
35	0-2	NGTH	000	Noise gate @ -39dB

Figure 11: ALC Response Envelope

3.12.1 ALC Register Map Overview

ALC can be enabled for either or both the left and right ADC channels. All ALC functions and mode settings are common to the left and right channels. When either the right or left PGA is disabled, the respective PGA will remain at the most recent gain value as set by the ALC. Registers that control the ALC features and functions are:

R32 Enable left/right ALC functions; set maximum gain, minimum gain
R33 ALC hold time, ALC target signal level
R34 ALC limiter mode selection, attack parameters, decay parameters
R35 Enable noise gate, noise gate parameters
R70 Selection of signal level averaging options and ALC table options
R70 Realtime readout of left channel gain value in use by ALC (same as left in stereo operation)
R71 Realtime readout of right channel gain value in use by ALC (same as right in stereo operation)
R76 Realtime readout of input signal level from averagingpeak-to-peak input signal detector
R77 Realtime readout of input signal level from averaging input signal peak detector

The following table shows some of the ALC parameter values and their ranges. The complete list of settings and values is included in the Detailed Register Map.

Parameter	Register	Bits	Name	Default Setting	Value	Programmable Range
Minimum Gain of PGA	32	0-2	ALCMINGAIN	000	-12dB	Range: -12dB to +30dB @ 6dB increments
Maximum Gain of PGA	32	3-5	ALCMAXGAIN	111	35.25dB	Range: -6.75dB to +35.25dB @ 6dB increments
ALC Function	32	7-8	ALCEN	00	Disabled	00 = Disable 01 = Enable right channel 10 = Enable left channel 11 = Enable both channels
ALC Target Level	33	0-3	ALCLVL	1011	-6dBFS	Range: -22.5dB to -1.5dBFS @ 1.5dB increments
ALC Hold Time	33	4-7	ALCHLD	0000	0ms	Range: 0ms to 1024ms at 1010 and above (timesare for 0.75dB steps, and double with every step)
ALC Attack time	34	0-3	ALCATK	0010	500µs	ALCM=0 - Range: 125µs to 128ms ALCM=1 - Range: 31µs to 32ms (timesare for 0.75dB steps, and double with every step)
ALC Decay Time	34	4-7	ALCDCY	0011	4ms	ALCM = 0 - Range: 500µs to 512ms ALCM = 1 - Range: 125µs to 128ms (timesare for 0.75dB steps, and double with every step)
Limiter Function	34	8	ALCMODE	0	Disabled	0 = ALC mode 1 = Limiter mode

Table 5: Registers associated with ALC and Limiter Control

3.13 Limiter Mode

When register 34, bit 8, is HIGH and ALC is enabled in register 32, bits 7-8 (ALCEN), the ALC block operates in limiter mode. In this mode, the PGA gain is constrained to be less than or equal to the PGA gain setting when the limiter mode is enabled. In addition, attack and decay times are faster in limiter mode than in normal mode as indicated by the different lookup tables for these parameters for limiter mode. The following waveform illustrates the behavior of the ALC in limiter mode in response to changes in various ALC parameters.

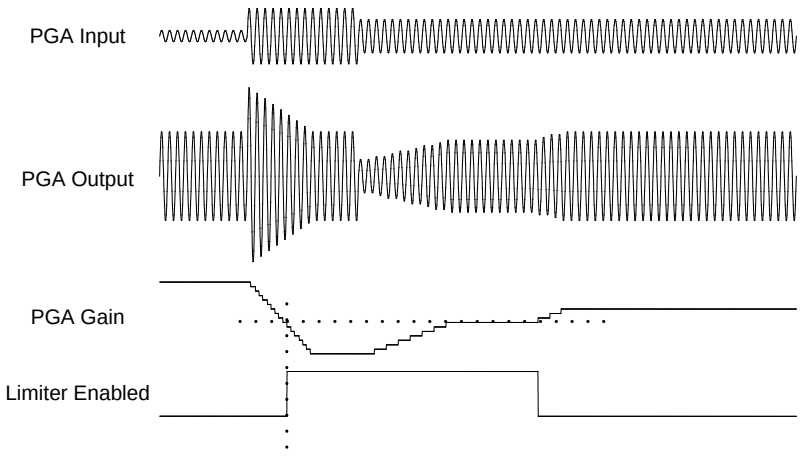
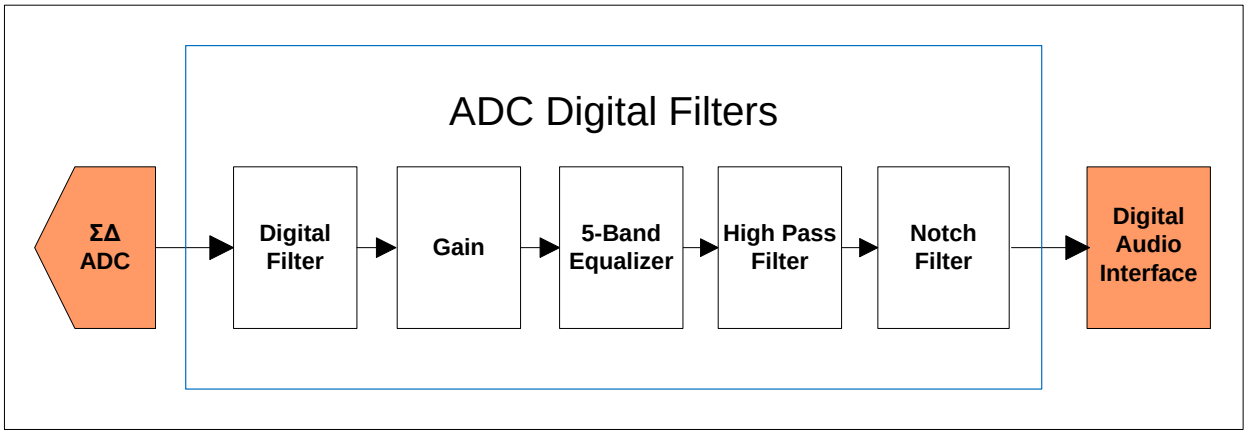


Figure 12: ALC Limiter Mode Operation

4 ADC Digital Block



The ADC digital block performs 24-bit analog-to-digital conversion and signal processing, making available a high quality audio sample stream the audio path digital interface.This block consists of a sigma-delta modulator, digital decimator/ filter, 5-band graphic equalizer, 3D effects, high pass filter, and a notch filter. The equalizer and 3D audio function block is a single resource that may be used by either the ADC or DAC, but not both at the same time. The ADC coding scheme is in twos complement format and the full-scale input level is proportional to VDDA. With a 3.3V supply voltage, the full-scale level is $1.0V_{RMS}$.

Registers that affect the ADC operation are:

R2 Power management enable/disable left/right ADC
R5 Digital passthrough of ADC output data into DAC input
R7 Sample rate indication bits (affect filter frequency scaling)
R14 Oversampling, polarity inversion, and filter controls for left/right ADC
R14 ADC high pass filter Audio Mode or Application Mode selection
R15 Left channel ADC digital volume control and update bit function
R16 Right channel ADC digital volume control and update bit function

4.1 Sampling / Oversampling Rate, Polarity Control, Digital Passthrough

The audio sample rate of the ADC is determined entirely by the IMCLK internal Master Clock frequency, which is 128 times the base audio sample rate. A technique known as oversampling is used to improve noise and distortion performance of the ADC, but this does not affect the final audio sample rate. The default oversampling rate of the ADC is 64X (64 times the audio sample rate), but this can be changed to 128X for greatly improved audio performance. The higher rate increases power consumption by only approximately three milliwatts per channel, so for most applications, the improved quality is a good choice. There is almost zero increased power to also run the DACs at 128X oversampling, and the best overall quality will be achieved when both the DACs and ADCs are operated at the same oversampling rate.

The polarity of either ADC output signal can be changed independently on either ADC logic output as a feature sometimes useful in management of the audio phase. This feature can help minimize any audio processing that may be otherwise required as the data are passed to other stages in the system.

Digital audio passthrough allows the output of the ADCs to be directly sent to the DACs as the input signal to the DAC for DAC output. In this mode of operation, the output data from the ADCs are still available on the ADCOUT logic pin. However, any external input signal for the DAC will be ignored. The passthrough function is useful for many test and application purposes, and the DAC output may be utilized in any way that is normally supported for the DAC analog output signals.

4.2 ADC Digital Volume Control and Update Bit Functionality

The effective output audio volume of each ADC can be changed using the digital volume control feature. This processes the output of the ADC to scale the output by the amount indicated in the volume register setting. Included is a "digital mute" value which will completely mute the signal output of the ADC. The digital volume setting can range from 0dB through -127dB in 0.5dB steps.

Important: The R15 and R16 update bits are write-only bits. The primary intended purpose of the update bit is to enable simultaneous changes to both the left and right ADC volume values, even though these values must be written sequentially. When there is a write operation to either R15 or R16 volume settings, but the update bit is not set (value = 0), the new volume setting is stored as pending for the future, but does not go into effect. When there is a write operation to either R15 or R16 and the update bit is set (value = 1), then the new value in the register being written is immediately put into effect, and any pending value in the other ADC volume register is put into effect at the same time.

4.3 ADC Programmable HighPass Filter

Each ADC is optionally supported by a high pass filter in the digital output path. Filter operation and settings are always the same for both left and right channels. The high pass filter has two different operating modes. In the audio mode, the filter is a simple first order DC blocking filter, with a cut-off frequency of 3.7Hz. In the application specific mode, the filter is a second order audio frequency filter, with a programmable cut-off frequency. The cutoff frequency of the high pass filter is scaled depending on the sampling frequency indicated to the system by the setting in Register 7.

Registers that affect operation of the programmable high pass filter are:

R7 Sample rate indication to the system (affects filter coefficient internal scaling)
R14 High-pass enable/disable, operating mode, and cut-off frequency

The following table provides the exact cutoff frequencies with different sample rates as indicated to the system by means of Register 7. The table shows the assumed actual numerical sample rates as determined by the system clocks. Detailed response curves are provided in the Appendix section of this document.

Register 14, bits 4 to 6 (HPF)	Sample Rate in kHz (FS)								
	R7(SMPLR) = 101or 100			R7(SMPLR) = 011 or 010			R7(SMPLR) = 001 or 000		
	8	11.025	12	16	22.05	24	32	44.1	48
000	82	113	122	82	113	122	82	113	122
001	102	141	153	102	141	153	102	141	153
010	131	180	156	131	180	156	131	180	156
011	163	225	245	163	225	245	163	225	245
100	204	281	306	204	281	306	204	281	306
101	261	360	392	261	360	392	261	360	392
110	327	450	490	327	450	490	327	450	490
111	408	563	612	408	563	612	408	563	612

Table 6: High Pass Filter Cut-off Frequencies in Hz (with HPFAM register 14, bit 7 = 1)

4.4 Programmable Notch Filter

Each ADC is optionally supported by a notch filter in the digital output path. Filter operation and settings are always the same for both left and right channels. A notch filter is useful to a very narrow band of audio frequencies in a stop band around a given center frequency. The notch filter is enabled by setting register 27, bit 7 (NFCEN), to 1. The center frequency is programmed by setting registers 27, 28, 29, and 30, bits 0 to 6 (NFA0[13:7], NFA0[6:0], NFA1[13:7], NFA1[6:0]), with two's compliment coefficient values calculated using table __.

Registers that affect operation of the notch filter are:

R27 Notch filter enable/disable
R27 Notch filter a0 coefficient high order bits and update bit
R28 Notch filter a0 coefficient low order bits and update bit
R29 Notch filter a1 coefficient high order bits and update bit
R30 Notch filter a1 coefficient low order bits and update bit

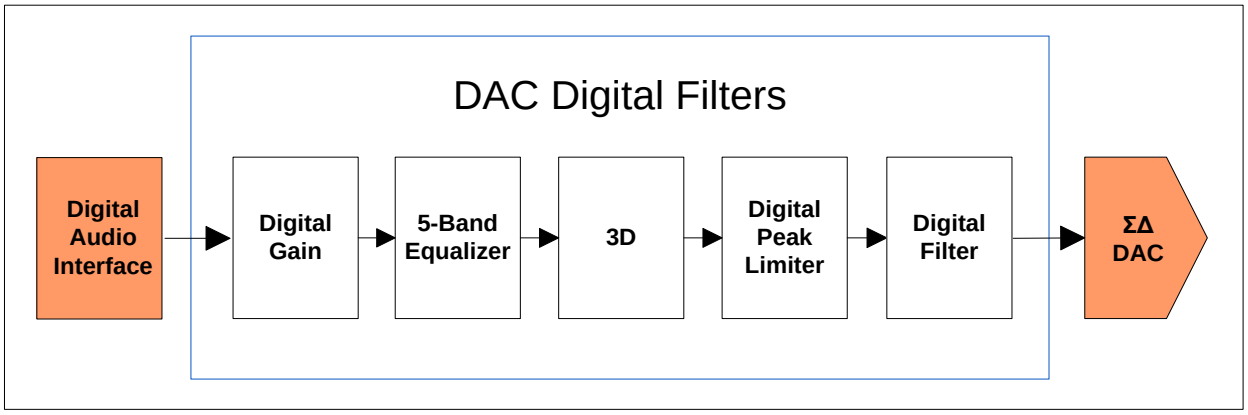
Important: The register update bits are write-only bits. The update bit function is important so that all filter coefficients actively being used are changed simultaneously, even though these register values must be written sequentially. When there is a write operation to any of the filter coefficient settings, but the update bit is not set (value = 0), the value is stored as pending for the future, but does not go into effect. When there is a write operation to any coefficient register, and the update bit is set (value = 1), then the new value in the register being written is immediately put into effect, and any pending coefficient value is put into effect at the same time.

Coefficient values are in the form of 2's-complement integer values, and must be calculated based upon the desired filter properties. The mathematical operations for calculating these coefficients aredetailed in the following table.

A_0	A_1	Notation	Register Value (DEC)
$\frac{1-\tan\left(\frac{2\ \pi\ f_b}{2\ f_s}\right)}{1+\tan\left(\frac{2\ \pi\ f_b}{2\ f_s}\right)}$	$-\left(1+A_0\right)\ x\ \cos\left(\frac{2\ \pi\ f_c}{f_s}\right)$	f_c = center frequency (Hz) f_b = -3dB bandwidth (Hz) f_s = sample frequency (Hz)	NFCA0 = $-A_0 \times 2^{13}$ NFCA1 = $-A_1 \times 2^{12}$ Note: Values are rounded to the nearest whole number and converted to 2's complement

Table 7: Equations to calculate notch filter coefficients

5 DAC Digital Block



The DAC digital block uses 24-bit signal processing to generate analog audio with a 16-bit digital sample stream input. This block consists of a sigma-delta modulator, digital decimator/filter, and optional 5-band graphic equalizer/3D effects block, and a dynamic range compressor/limiter. The DAC coding scheme is in twos complement format and the full-scale output level is proportional to VDDA. With a 3.3V supply voltage, the full-scale output level is $1.0V_{RMS}$.

Registers that affect the DAC operation are:

R3 Power management enable/disable left/right DAC
R5 Digital passthrough of ADC output data into DAC input
R7 Sample rate indication bits (affect filter frequency scaling)
R10 Softmute, Automute, oversampling options, polarity controls for left/right DAC
R11 Left channel DAC digital volume value; update bit feature
R12 Right channel DAC digital volume value; update bit feature

5.1 DAC Soft Mute

Both DACs are initialized with the SoftMute function disabled, which is a shared single control bit. Softmute automatically ramps the DAC digital volume down to zero volume when enabled, and automatically ramps the DAC digital volume up to the register specified volume level for each DAC when disabled. This feature provides a tool that is useful for using the DACs without introducing pop and click sounds.

5.2 DAC AutoMute

The analog output of both DACs can be automatically muted in a no signal condition. Both DACs share a single control bit for this function. When automute is enabled, the analog output of the DAC will be muted any time there are 1024 consecutive audio sample values with a zero value. If at any time there is a non-zero sample value, the DAC will be un-muted, and the 1024 count will be reinitialized to zero.

5.3 DAC Sampling / Oversampling Rate, Polarity Control, Digital Passthrough

The sampling rate of the DAC is determined entirely by the frequency of its input clock and the oversampling rate setting. The oversampling rate of the DAC can be changed to 128X for improved audio performance at slightly higher power consumption. Because the additional supply current is only 1mA, in most applications the 128X oversampling is preferred for maximum audio performance.

The polarity of either DAC output signal can be changed independently on either DAC analog output as a feature sometimes useful in management of the audio phase. This feature can help minimize any audio processing that may be otherwise required as the data are passed to other stages in the system. Digital audio passthrough allows the output of the ADCs to be directly sent to the DACs as the input signal to the DAC for DAC output. In this mode of operation, the external digital audio signal for the DAC will be ignored. The

passthrough function is useful for many test and application purposes, and the DAC output may be utilized in any way that is normally supported for the DAC analog output signals.

5.4 DAC Digital Volume Control and Update Bit Functionality

The effective output audio volume of each DAC can be changed using the digital volume control feature. This processes the output of the DAC to scale the output by the amount indicated in the volume register setting. Included is a "digital mute" value which will completely mute the signal output of the DAC. The digital volume setting can range from 0dB through -127dB in 0.5dB steps.

Important: The R11 and R12 update bits are write-only bits. The primary intended purpose of the update bit is to enable simultaneous changes to both the left and right DAC volume values, even though these values must be written sequentially. When there is a write operation to either R11 or R12 volume settings, but the update bit is not set (value = 0), the new volume setting is stored as pending for the future, but does not go into effect. When there is a write operation to either R11 or R12 and the update bit is set (value = 1), then the new value in the register being written is immediately put into effect, and any pending value in the other DAC volume register is put into effect at the same time.

5.5 DACAutomaticOutputPeak Limiter / Volume Boost

Both DACs are supported by a digital output volume limiter/boost feature which can be useful to keep output levels within a desired range without any host/processor intervention. Settings are shared by both DAC channels.

Registers that manage the peak limiter and volume boost functionality are:

R24 Limiter enable/disable, limiter attack rate, boost decay rate
R25 Limiter upper limit, limiter boost value

The operation of the peak limiter is shown in the following figure. The upper signal graphs show the time varying level of the input and output signals, and the lower graph shows the gain characteristic of the limiter. When the signal level exceeds the limiter threshold value by 0.5dB or greater, the DAC digital signal level will be attenuated at a rate set by the limiter attack rate value. When the input signal level is less than the boost lower limit by 0.5dB or greater, the DAC digital volume will be increased at a rate set by the boost decay rate value. The default boost gain value is limited not to exceed 0dB (zero attenuation).

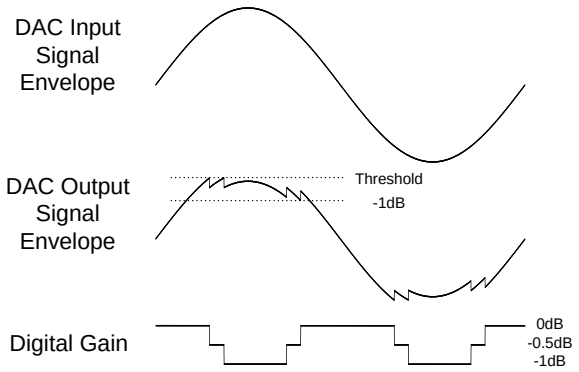


Figure 13: DAC Digital Limiter Control

The limiter may optionally be set to automatically boost the DAC digital signal level when the signal is more than 0.5dB below the limiter threshold. This can be useful in applications in which it is desirable to compress the signal dynamic range. This is accomplished by setting the limiter boost register bits to a value greater than zero. If the limiter is disabled, this boost value will be applied to the DAC digital output signal separate from other gain affecting values.

5.6 5-Band Equalizer

The NAU8822A includes a 5-band graphic equalizer with low distortion, low noise, and wide dynamic range. The equalizer is applied to both left and right channels. The equalizer is grouped with the 3D Stereo Enhancement signal processing function. Both functions may be assigned to support either the ADC path, or the DAC path, but not both paths simultaneously.

Registers that affect operation of the 5-Band Equalizer are:

R18 Assign equalizer to DAC path or to ADC path (default = ADC path)
R18 Band 1 gain control and cut-off frequency
R19 Band 2 gain control, center cut-off frequency, and bandwidth
R20 Band 3 gain control, center cut-off frequency, and bandwidth
R21 Band 4 gain control, center cut-off frequency, and bandwidth
R22 Band 5 gain control and cut-off frequency

Each of the five equalizer bands is independently adjustable for maximum system flexibility, and each offers up to 12dB of boost and 12dB of cut with 1dB resolution. The high and the low bands are shelving filters (high-pass and low-pass, respectively), and the middle three bands are peaking filters. Details of the register value settings are described below. Response curve examples are provided in the Appendix of this document.

Register Value	Equalizer Band				
	1 (HighPass) Register 18 Bits 5 & 6 EQ1CF	2 (BandPass) Register 19 Bits 5 & 6 EQ2CF	3 (BandPass) Register 20 Bits 5 & 6 EQ3CF	4 (BandPass) Register 21 Bits 5 & 6 EQ4CF	5 (LowPass) Register 22 Bits 5 & 6 EQ5CF
00	80Hz	230Hz	650Hz	1.8kHz	5.3kHz
01	105Hz	300Hz	850Hz	2.4kHz	6.9kHz
10	135Hz	385Hz	1.1kHz	3.2kHz	9.0kHz
11	175Hz	500Hz	1.4kHz	4.1kHz	11.7kHz

Table 8: Equalizer Center/Cutoff Frequencies

Register Value		Gain	Registers
Binary	Hex		
00000	00h	+12db	Bits 0 to 4 in registers 18 (EQ1GC) 19 (EQ2GC) 20 (EQ3GC) 21 (EQ4GC) 22 (EQ5GC)
00001	01h	+11dB	
00010	02h	+10dB	
- - -	- -	Increments 1dB per step	
01100	0Ch	0dB	
01101	17h	-11dB	
- - -	- -	Increments 1dB per step	
11000	18h	-12dB	
11001 to 11111	19h to 1Fh	Reserved	

Table 9: Equalizer Gains

5.7 3D Stereo Enhancement

NAU8822A includes digital circuitry to provide flexible 3D enhancement to increase the perceived separation between the right and left channels, and has multiple options for optimum acoustic performance. The equalizer is grouped with the 3D Stereo Enhancement signal processing function. Both functions may be assigned to support either the ADC path, or the DAC path, but not both paths simultaneously.

Registers that affect operation of 3D Stereo Enhancement are:

R18 Assign equalizer to DAC path or to ADC path (default = ADC path)
R41 3D Audio depth enhancement setting

The amount of 3D enhancement applied can be programmed from the default 0% (no 3D effect) to 100% in register 41, bits 0 to 3 (DEPTH3D), as shown in Table __. Note: 3D enhancement uses increased gain to achieve its effect, so that the source signal may need to be attenuated by up to 6dB to avoid clipping.

Register 41 Bits 0 to 3 3DDEPTH	3D Effect
0000	0%
0001	6.7%dB
0010	13.4%dB
- - -	Increments 6.67% for each binary step in the input word
1110	93.3%
1111	100%

Table 10: 3D Enhancement Depth

5.8 Companding

Companding is used in digital communication systems to optimize signal-to-noise ratios with reduced data bit rates, using non-linear algorithms. NAU8822A supports the two main telecommunications companding standards on both the transmit and the receive sides: A-law and µ-law. The A-law algorithm is primarily used in European communication systems and the µ-law algorithm is primarily used by North America, Japan, and Australia. . Companding converts 13 bits (µ-law) or 12 bits (A-law) to 8 bits using non-linear quantization. The companded signal is an 8bit word containing sign (1-bit), exponent (3-bits) and mantissa (4-bits)

Following are the data compression equations set in the ITU-T G.711 standard and implemented in the NAU8822A:

5.9 µ-law

$F(x) = \ln(1 + \mu|x|) / \ln(1 + \mu)$ $-1 \le x \le 1$
with µ=255 for the U.S. and Japan

5.10 A-law

$F(x) = A|x| / (1 + \ln A)$ for $x \le 1/A$
$F(x) = (1 + \ln A|x|) / (1 + \ln A)$ for $1/A \le x \le 1$
with A=87.6 for Europe

The register affecting companding operation is:

R5 Enable 8-bit mode, enable DAC companding, enable ADC companding

The companded signal is an 8-bit word consisting of a sign bit, three bits for the exponent, and four bits for the mantissa. When companding is enabled, the PCM interface must be set to an 8-bit word length. When in 8-bit mode, the Register 4 word length control (WLEN) is ignored.

Companding Mode	Register 5			
	Bit 4	Bit3	Bit 2	Bit 1
No Companding (default)	0	0	0	0
ADC				
A-law			1	1
μ-law			1	0
DAC				
A-law	1	1		
μ-law	1	0		

Table 11: Companding Control

5.11 8-bit Word Length

Writing a 1 to register 5, bit 5 (CMB8), will cause the PCM interface to use 8-bit word length for data transfer, overriding the word length configuration setting in WLEN (register 4, bits 5 and 6.).

6 Analog Outputs

The NAU8822A features six different analog outputs. These are highly flexible and may be used individually or in pairs for many purposes. However, they are grouped in pairs and named for their most commonly used stereo application end uses. The following sections detail key features and functions of each type of output. Included is a description of the associated output mixers. These mixers are separate internal functional blocks that are important toward understanding all aspects of the analog output section.

Important: For analog outputs depopping purpose, when powering up speakers, headphone, AUXOUTs, certain delays are generated after enabling sequence. However, the delays are created by MCLK and sample rate register. For correct operation, sending I2S signal no earlier than 250ms after speaker or headphone enabled and MCLK appearing.

6.1 Main Mixers (LMAIN MIX and RMAIN MIX)

Each left and right channel is supported by an independent main mixer. This mixer combines signals from a various available signal sources internal to the device. Each mixer may also be selectively enabled/disabled as part of the power management features. The outputs of these mixers are the only signal source for the headphone outputs, and the primary signal source for the loudspeaker outputs.

Each mixer can accept either or both the left and right digital to analog (DAC) outputs. Normally, the left and right DAC is mixed into the associated left and right main output mix. This additional capability to mix opposite DAC channels enables switching the left and right DAC outputs to the opposite channel, or mixing together the left and right DAC signals – all without any processor or host intervention and processing overhead.

Each mixer also can also combine signals directly from the respective left or right AUX input, and from the output of the respective ADC Mix/Boost stage output. Each of these paths may be muted, or have an applied selectable gain between -15dB and +6dB in 3dB steps.

Registers that affect operation of the Main Mixers are:

R3 Power control for the left and right main mixer
R49 left and right DAC cross-mixing source selection options
R50 left DAC to left main mixer source selection option
R51 right DAC to right main mixer source selection option

R50 left AUX and ADC Mix/Boost source select, and gain settings
R51 right AUX and ADC Mix/Boost source select, and gain settings

6.2 Auxiliary Mixers (AUX1 MIXER and AUX2 MIXER)

Each auxiliary analog output channel is supported by an independent mixer dedicated to the auxiliary output function. This mixer combines signals from a various available signal sources internal to the device. Each mixer may also be selectively enabled/disabled as part of the power management features.

Unlike the main mixers, the auxiliary mixers are not identical and combine different signal sets internal to the device. These mixers in conjunction with the auxiliary outputs greatly increase the overall capabilities and flexibility of the NAU8822A.

The AUX1 mixer combines together any or all of the following:

Left Main Mixer output
Right Main Mixer output
Left DAC output
Right DAC output
Right ADC Mix/Boost stage output
The AUX2 mixer combines together any or all of the following:
Left Main Mixer output
Left DAC output
Left ADC Mix/Boost stage output
Inverted output from AUX1 mixer stage

Registers that affect operation of the Auxiliary Mixers are:

R1 Power control for the left and right auxiliary mixer
R56 Signal source selection for the AUX2 mixer
R57 Signal source selection for the AUX1 mixer

6.3 Right Speaker Submixer

The right speaker submixer serves two important functions. One is to optionally invert the output from the Right Main Mixer as an optional signal source for the right channel loudspeaker output driver. This inversion is normal and necessary in typical applications using the loudspeaker drivers.

The other function of the right speaker submixer is to mix the RAUXIN input signal directly into the right channel speaker output driver. This enables the RAUXIN signal to be output on the right loudspeaker channel, but not be mixed to any other output. The traditional purpose of this path is to support an old-style beep sound, such as traditionally generated by a microprocessor output toggle bit. On the NAU8822A, this traditional function is supported by a full quality signal path that may be used for any purpose. The volume for this path has a selectable gain from -15dB through +6dB in 3dB step increments.

There is no separate power management control feature for the Right Speaker Submixer. The register that affects the Right Speaker Submixer is:

R43 Input mute controls, volume for RAUXIN path

6.4 Headphone Outputs (LHP and RHP)

These are high quality, high current output drivers intended for driving low impedance loads such as headphones, but also suitable for a wide range of audio output applications. The only signal source for each of these outputs is from the associated left and right Main Mixer. Power for this section is provided from the VDDA pin. Each driver may be selectively enabled/disabled as part of the power management features.

Each output can be individually muted, or controlled over a gain range of -57dB through +6dB in 3dB steps. Gain changes for the two headphone outputs can be coordinated through use of an update bit feature as part of the register controls. Additionally, clicks that could result from gain changes can be suppressed using an optional zero crossing feature.

Registers that affect the headphone outputs are:

R2 Power management control for the left and right headphone amplifier
R52 Volume, mute, update, and zero crossing controls for left headphone driver
R53 Volume, mute, update, and zero crossing controls for right headphone driver

Important: The R52 and R53 update bits are write-only bits. The primary intended purpose of the update bit is to enable simultaneous changes to both the left and right headphone output volume values, even though these two register values must be written sequentially. When there is a write operation to either R52 or R53 volume settings, but the update bit is not set (value = 0), the new volume setting is stored as pending for the future, but does not go into effect. When there is a write operation to either R52 or R53 and the update bit is set (value = 1), then the new value in the register being written is immediately put into effect, and any pending value in the other headphone output volume register is put into effect at the same time.

Zero-Crossing controls are implemented to suppress clicking sounds that may occur when volume setting changes take place while an audio input signal is active. When the zero crossing function is enabled (logic = 1), any volume change for the affected channel will not take place until the audio input signal passes through the zero point in its peak-to-peak swing. This prevents any instantaneous voltage change to the audio signal caused by volume setting changes. If the zero crossing function is disabled (logic = 0), volume changes take place instantly on condition of the Update Bit, but without regard to the instantaneous voltage level of the affected audio input signal.

6.5 Speaker Outputs

These are high current outputs suitable for driving low impedance loads, such as an 8-ohm loudspeaker. Both outputs may be used separately for a wide range of applications, however, the intended application is to use both outputs together in a BTL (Bridge-Tied-Load, and also, Balanced-Transformer-Less) configuration. In most applications, this configuration requires an additional signal inversion, which is a feature supported in the right speaker submixer block.

This inversion is normal and necessary when the two speaker outputs are used together in a BTL (Bridge-Tied-Load, and also, Balanced-Transformer-Less) configuration. In this physical configuration, the RSPKOUT signal is connected to one pole of the loudspeaker, and the LSPKOUT signal is connected to the other pole of the loudspeaker. Mathematically, this creates within the loudspeaker a signal equal to (Left-Right). The desired mathematical operation for a stereo signal is to drive the speaker with (Left+Right). This is accomplished by implementing an additional inversion to the right channel signal. For most applications, best performance will be achieved when care is taken to insure that all gain and filter settings in both the left and right channel paths to the loudspeaker drivers are identical.

Power for the loudspeaker outputs is supplied via the VDDSPK pin, and ground is independently provided as the VSSPK pin. This power option enables an operating voltage as high as 5Vdc and helps in a system design to prevent high current outputs from creating noise on other supply voltage rails or system grounds. VSSPK must be connected at some point in the system to VSSA, but provision of the VSSPK as a separate high current ground pin facilitates managing the flow of current to prevent “ground bounce” and other ground noise related problems.

Each loudspeaker output may be selectively enabled/disabled as part of the power management features. Registers that affect the loudspeaker outputs are:

R3 Power management control of LSPKOUT and RSPKOUT driver outputs
R47/R48 Driver distortion mode control
R49 Disable boost control for speaker outputs for VDDSPK 3.3V or lower
R54 Volume (gain), mute, update bit, and zero crossing control for left speaker driver
R55 Volume (gain), mute, update bit, and zero crossing control for right speaker driver

Important: The R49 boost control option is set in the power-on reset condition for high voltage operation of VDDSPK. If VDDSPK is greater than 3.6Vdc, the R49 boost control bits should be remain at the power-on default settings. This insures reliable operation of the part, proper DC biasing, and optimum scaling of the signal to enable the output to achieve full scale output when VDDSPK is greater than VDDA. In the boost mode, the gain of the output stage is increased by a factor of 1.5 times the normal gain value.

Important: The R54 and R55 update bits are write-only bits. The primary intended purpose of the update bit is to enable simultaneous changes to both the left and right headphone output volume values, even though these two register values must be written sequentially. When there is a write operation to either R54 or R55 volume settings, but the

update bit is not set (value = 0), the new volume setting is stored as pending for the future, but does not go into effect. When there is a write operation to either R54 or R55 and the update bit is set (value = 1), then the new value in the register being written is immediately put into effect, and any pending value in the other headphone output volume register is put into effect at the same time.

Zero-Crossing controls are implemented to suppress clicking sounds that may occur when volume setting changes take place while an audio input signal is active. When the zero crossing function is enabled (logic = 1), any volume change for the affected channel will not take place until the audio input signal passes through the zero point in its peak-to-peak swing. This prevents any instantaneous voltage change to the audio signal caused by volume setting changes. If the zero crossing function is disabled (logic = 0), volume changes take place instantly on condition of the Update Bit, but without regard to the instantaneous voltage level of the affected audio input signal.

The loudspeaker drivers may optionally be operated in an ultralow distortion mode. This mode may require additional external passive components to insure stable operation in some system configurations. No external components are required in normal mode speaker driver operation. Distortion performance in normal operation is excellent, and already suitable for almost every application.

6.6 Auxiliary Outputs

These are high current outputs suitable for driving low impedance loads such as headphones or line level loads. Power for these outputs is supplied via the VDDSPK pin, and ground is also independently provided as the VSSPK pin. This power option enables an operating voltage as high as 5Vdc and helps in a system design to prevent high current outputs from creating noise on other supply voltage rails or system grounds. VSSPK must be connected at some point in the system to VSSA, but provision of the VSSPK as a separate high current ground pinfacilitates managing the flow of current to prevent “ground bounce” and other ground noise related problems.

Each auxiliary output driver may be selectively enabled/disabled as part of the power management features.Registers that affect the auxiliary outputs are:

R3 Power management control of AUXOUT1 and AUXOUT2 outputs
R49 Disable boost control for AUXOUT1 and AUXOUT2 for VDDSPK 3.3Vdc or lower
R56 Mute, gain control, and input selection controls for AUXOUT2
R57 Mute, gain control, and input selection controls for AUXOUT1

Important: The R49 boost control option is set in the power-on reset condition for high voltage operation of VDDSPK. If VDDSPK is greater than 3.6Vdc, the R49 boost control bits should be remain at the power-on default settings. This insures reliable operation of the part, proper DC biasing, and optimum scaling of the signal to enable the output to achieve full scale output when VDDSPK is greater than VDDA. In the boost mode, the gain of the output stage is increased by a factor of 1.5 times the normal gain value.

An optional alternative function for these outputs is to provide a virtual ground for an external headphone device. This is for eliminating output capacitors for the headphone amplifier circuit in applications where this type of design is appropriate. In this type of application, the AUXOUT output is typically operated in the muted condition. In the muted condition, and with the output configured in the non-boost mode (also requiring that VDDSPK < 3.61Vdc), the AUXOUT output DC level will remain at the internal VREF level. This the same internal DC level as used by the headphone outputs. Because these DC levels are nominally the same, DC current flowing through the headphone in this mode of operation is minimized. Depending on the application, one or both of the auxiliary outputs may be used in this fashion.

7 Miscellaneous Functions

7.1 Slow Timer Clock

An internal Slow Timer Clock is supplied to automatically control features that happen over a relatively periods of time, or time-spans. This enables the NAU8822A to implement long time-span features without any host/processor management or intervention.

Two features are supported by the Slow Timer Clock. These arean optional automatic time out for the zero-crossing holdoff of PGA volume changes, and timing for debouncing of the mechanical jack detection feature. If either feature is required, the Slow Timer Clock must be enabled.

The Slow Timer Clock is initialized in the disabled state. The Slow Timer Clock is controlled by only the following register:

R7 Sample rate indication select, and Slow Timer Clock enable

The Slow Timer Clock rate is derived from MCLK using an integer divider that is compensated for the sample rate as indicated by the R7 sample rate register. If the sample rate register value precisely matches the actual sample rate, then the internal Slow Timer Clock rate will be a constant value of 128ms. If the actual sample rate is, for example, 44.1kHz and the sample rate selected in R7 is 48kHz, the rate of the Slow Timer Clock will be approximately 10% slower in direct proportion of the actual vs. indicated sample rate. This scale of difference should not be important in relation to the dedicated end uses of the Slow Timer Clock.

7.2 General Purpose Inputs and Outputs (GPIO1, GPIO2, GPIO3) and Jack Detection

Three pins are provided in the NAU8822A that may be used for limited logic input/output functions. GPIO1 has multiple possible functions, and may be either a logic input or logic output. GPIO2 and GPIO3 may be either line level analog inputs, or logic inputs dedicated to the purpose of jack detection. GPIO2 and GPIO3 do not have any logic output capability or function. Only one GPIO can be selected for jack detection.

If a GPIO is selected for the jack detection feature, the Slow Timer Clock must be enabled. The jack detection function is automatically “debounced” such that momentary changes to the logic value of this input pin are ignored. The Slow Timer Clock is necessary for the debouncing feature.

Registers that control the GPIO functionality are:

R8 GPIO functional selection options
R9 Jack Detection feature input selection and functional options

If a GPIO is selected for the jack detection function, the required Slow Timer Clock determines the duration of the time windows for the input logic debouncing function. Because the logic level changes happen asynchronously to the Slow Timer Clock, there is inherently some variability in the timing for the jack detection function. A continuous and persistent logic change on the GPIO pin used for jack detection will result in a valid internal output signal within 2.5 to 3.5 periods of the Slow Timer Clock. Any logic change of shorter duration will be ignored.

The threshold voltage for a jack detection logic-low level is no higher than 1.0Vdc. The threshold voltage for a jack detection logic-high level is no lower than 1.7Vdc. These levels will be reduced as the VDDC core logic voltage pin is reduced below 1.9Vdc.

If the RLIN or LLIN input pin is used for the GPIO function, the analog signal path should be configured to be disconnected from its respective PGA input. This will not cause harm to the device, but could cause unwanted noise introduced through the PGA path.

7.3 Automated Features Linked to Jack Detection

Some functionality can be automatically controlled by the jack detection logic. This feature can be used to enable the internal analog amplifier bias voltage generator, and/or enable analog output drivers automatically as a result of detecting a logic change at a GPIO pin assigned to the purpose of jack detection. This eliminates any requirement for the host/processor to perform these functions.

The internal analog amplifier bias generator creates the VREF voltage reference and bias voltage used by the analog amplifiers. The ability to control it is a power management feature. This is implemented as a logical “OR” function of either the debounced internal jack detection signal, or the ABIASEN control bit in Register 1. The bias generator will be powered if either of these control signals is enabled (value = 1).

Power management control of four different outputs is also optionally and selectively subject to control linked with the jack detection signal. The four outputs that can be controlled this way are the headphone driver signal pair, loudspeaker driver signal pair, AUXOUT1, and AUXOUT2. Register settings determine which outputs may be

enabled, and whether they are enabled by a logic 1 or logic 0 value. Output control is a logical "AND" operation of the jack detection controls, and of the register control bits that normally control the outputs. Both controls must be in the "ON" condition for a given output to be enabled.

Registers that affect these functions are:

R9 GPIO pin selection for jack detect function, jack detection enable, VREF jack enable
R13 bit mapped selection of which outputs are to be enabled when jack detect is in a logic 1 state
R13 bit mapped selection of which outputs are to be enabled when jack detect is in a logic 0 state

8 Clock Selection and Generation

The NAU8822A has two basic clock modes that support the ADC and DAC data converters. It can accept external clocks in the slave mode, or in the master mode, it can generate the required clocks from an external reference frequency using an internal PLL (Phase Locked Loop). The internal PLL is a fractional type scaling PLL, and therefore, a very wide range of external reference frequencies can be used to create accurate audio sample rates.

Separate from this ADC and DAC clock subsystem, audio data are clocked to and from the NAU8822A by means of the control logic described in the Digital Audio Interfaces section. The audio bit rate and audio sample rate for this data flow are managed by the Frame Sync (FS) and Bit Clock (BCLK) pins in the Digital Audio Interface.

It is important to understand that the sampling rate for the ADC and DAC data converters is not determined by the Digital Audio Interface, and instead, this rates derived exclusively from the Internal Master Clock (IMCLK). Itis therefore a requirement that the Digital Audio Interface and data converters be operated synchronously, and that the FS, BCLK, and IMCLK signals are all derived from a common reference frequency. If these three clocks signals are not synchronous, audio quality will be reduced.

The IMCLK is always exactly 256 times the sampling rate of the data converters. Also note that IMCLK should not exceed 12.288MHz under any condition.

IMCLK is output from the Master Clock Prescaler. The prescaler reduces by an integer division factor the input frequency input clock. The source of this input frequency clock is either the external MCLK pin, or the output from the internal PLL Block.

Registers that are used to manage and control the clock subsystem are:

R1 Power management, enable control for PLL (default = disabled)
R6 Master/slave mode, clock scaling, clock selection
R7 Sample rate indication (scales DSP coefficients and timing – does NOT affect actual sample rate
R8 MUX control and division factor for PLL output on GPIO1
R36 PLL Prescaler, Integer portion of PLL frequency multiplier
R37 Highest order bits of 24-bit fraction of PLL frequency multiplier
R38 Middle order bits of 24-bit fraction of PLL frequency multiplier
R39 Lowest order bits of 24-bit fraction of PLL frequency multiplier

In Master Mode, the IMCLK signal is used to generate FS and BCLK signals that are driven onto the FS and BCLK pins and input to the Digital Audio Interface. FS is always IMCLK/256 and the duty cycle of FS is automatically adjusted to be correct for the mode selected in the Digital Audio Interface. The frequency of BCLK may optionally be divided to optimize the bit clock rate for the application scenario.

In Slave Mode, there is no connection between IMCLK and the FS and BCLK pins. In this mode, FS and BLCK are strictly input pins, and it is the responsibility of the system designer to insure that FS, BCLK, and IMCLK are synchronous and scaled appropriately for the application.

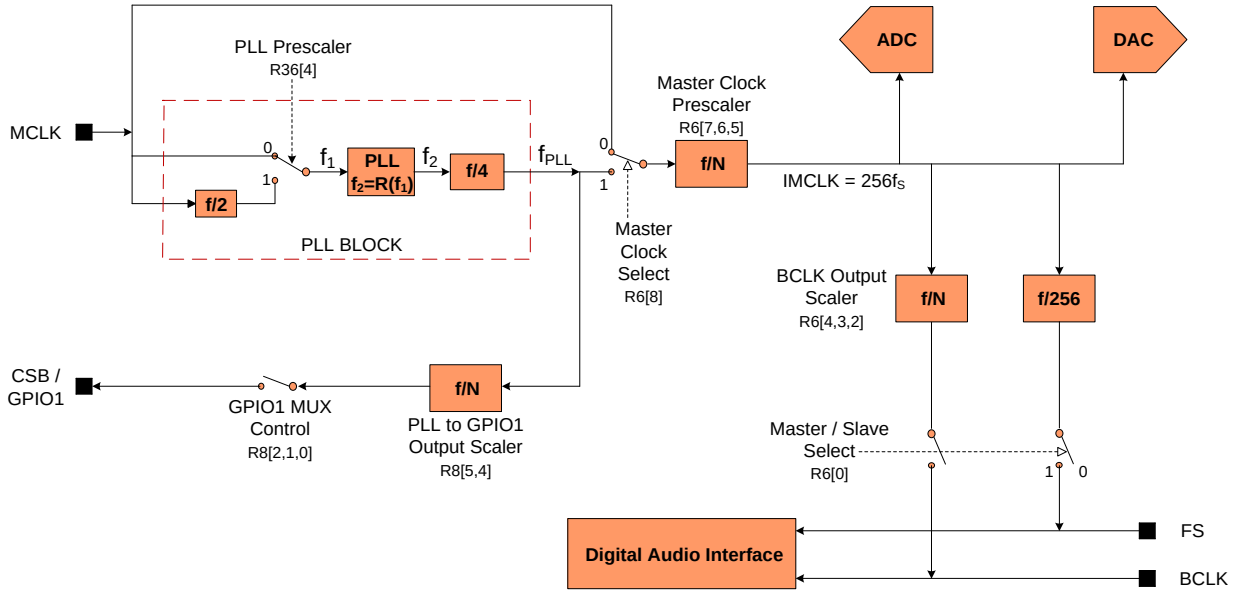


Figure 14: PLL and Clock Select Circuit

8.1 Phase Locked Loop (PLL) General Description

The PLL may be optionally used to multiply an external input clock reference frequency by a high resolution fractional number. To enable the use of the widest possible range of external reference clocks, the PLL block includes an optional divide-by-two prescaler for the input clock, a fixed divide-by-four scaler on the PLL output, and an additional programmable integer divider that is the Master Clock Prescaler.

The high resolution fraction for the PLL is the ratio of the desired PLL oscillator frequency (f_2), and the reference frequency at the PLL input (f_1). This can be represented as $R = f_2/f_1$, with R in the form of a decimal number: xy.abcdefgh. To program the NAU8822A, this value is separated into an integer portion ("xy"), and a fractional portion, "abcdefgh". The fractional portion of the multiplier is a value that when represented as a 24-bit binary number (stored in three 9-bit registers on the NAU8822A), very closely matches the exact desired multiplier factor.

To keep the PLL within its optimal operating range, the integer portion of the decimal number ("xy"), must be any of the following decimal values: 6, 7, 8, 9, 10, 11, or 12. The input and output dividers outside of the PLL are often helpful to scale frequencies as needed to keep the "xy" value within the required range. Also, the optimum PLL oscillator frequency is in the range between 90MHz and 100MHz, and thus, it is best to keep f_2 within this range.

In summary, for any given design, choose:

- IMCLK = desired Master Clock = (256)*(desired codec sample rate)
- f_2 = (4)*(P)(IMCLK) or (2)*(P)(IMCLK) when PLL49MOUT bit R72[2] = 1
  where P is the Master Clock Prescale integer value; optimal f_2: 90MHz< f_2 <100MHz
- f_1 = (MCLK)/(D), where D is the PLL Prescale factor of 1, or 2, and MCLK is the frequency at the MCLK pin
  note: The integer values for D and P are chosen to keep the PLL in its optimal operating range. It may be best to assign initial values of 1 to both D and P, and then by inspection, determine if they should be a different value.
- $R = f_2/f_1$ = xy.abcdefgh decimal value, which is the fractional frequency multiplication factor for the PLL
- N = xy truncated integer portion of the R value, and limited to decimal value 6, 7, 8, 9, 10, 11, or 12
- $K = (2^{24})*(0.abcdefgh)$, rounded to the nearest whole integer value, then converted to a binary 24-bit value
- R36 is set with the whole number integer portion, N, of the multiplier
- R37, R38, R39 are set collectively with the 24-bit binary fractional portion, K, of the multiplier
- R36 PLL Prescaler set as necessary
- R6 Master Clock Prescaler and BCLK Output Scaler set as necessary. The BCLK should be limited per described by BCLK Timing Chart, therefore BCLKSEL setting must adhere to Timing Chart.

8.1.1 Phase Locked Loop (PLL) Design Example

In an example application, a desired sample rate for the DAC is known to be 48.000kHz. Therefore, it is also known that the IMCLK rate will be 256fs, or 12.288MHz. Because there is a fixed divide-by-four scaler on the PLL output, then the desired PLL oscillator output frequency will be 49.152MHz.

In this example system design, there is already an available 12.000MHz clock from the USB subsystem. To reduce system cost, this clock will also be used for audio. Therefore, to use the 12MHz clock for audio, the desired fractional multiplier ratio would be R = 49.152/12.000 = 4.096. This value, however, does not meet the requirement that the "xy" whole number portion of the multiplier be in the inclusive range between 6 and 12. To meet the requirement, the Master Clock Prescaler can be set for an additional divide-by-two factor. This now makes the PLL required oscillator frequency 98.304 MHz, and the improved multiplier value is now R = 98.304/12.000 = 8.192.

To complete this portion of the design example, the integer portion of the multiplier is truncated to the value, 8. The fractional portion is multiplied by 2^{24}, as to create the needed 24-bit binary fractional value. The calculation for this is: $(2^{24})(0.192) = 3221225.472$. It is best to round this value to the nearest whole value of 3221225, or hexadecimal 0x3126E9. Thus, the values to be programmed to set the PLL multiplier whole number integer and fraction are:

```
R36  0xnm8   ; integer portion of fraction,(nm represents other settings in R36)
R37  0x00C   ; highest order 6-bits of 24-bit fraction
R38  0x093   ; middle 9-bits of 24-bit fraction
R39  0x0E9   ; lowest order 9-bits of 24-bit fraction
```

Below are additional examples of results for this calculation applied to commonly available clock frequencies and desired IMCLK 256fs sample rates.

MCLK (MHz)	Desired 256fs IMCLK rate (MHz)	PLL oscillator f_2 (MHz)	PLL Prescaler divider	Master Clock divider	Fractional Multiplier $R = f_2/f_1$	Integer Portion N (Hex)	Fractional Portion K (Hex)
12.0	11.28960	90.3168	1	2	7.526400	7	86C226
12.0	12.28800	98.3040	1	2	8.192000	8	3126E9
14.4	11.28960	90.3168	1	2	6.272000	6	45A1CA
14.4	12.28800	98.3040	1	2	6.826667	6	D3A06D
19.2	11.28960	90.3168	2	2	9.408000	9	6872B0
19.2	12.28800	98.3040	2	2	10.240000	A	3D70A3
19.8	11.28960	90.3168	2	2	9.122909	9	1F76F8
19.8	12.28800	98.3040	2	2	9.929697	9	EE009E
24.0	11.28960	90.3168	2	2	7.526400	7	86C226
24.0	12.28800	98.3040	2	2	8.192000	8	3126E9
26.0	11.28960	90.3168	2	2	6.947446	6	F28BD4
26.0	12.28800	98.3040	2	2	7.561846	7	8FD526

Table 12: PLL Frequency Examples

Make sure that PLL is not turned on (R1[4]=0) before R36, R37, R38, and R39 are programmed accordingly to ensure that IMCLK is not greater than 12.288MHz.

8.2 CSB/GPIO1 as PLL output

CSB/GPIO1 is a multi-function pin that may be used for a variety of purposes. If not required for some other purpose, this pin may be configured to output the clock frequency from the PLL subsystem. This is the same frequency that is available from the PLL subsystem as the input to the Master Clock Prescaler. This frequency may be optionally divided by an additional integer factor of 2, 3, or 4, before being output on GPIO1.

9 Control Interfaces

9.1 Selection of Control Mode

The NAU8822A features include a serial control bus that provides access to all of the device control registers. This bus may be configured either as a 2-wire interface that is interoperable with industry standard implementations of the I2C serial bus, or as a 3-wire/4-wire bus compatible with commonly used industry implementations of the SPI (Serial Peripheral Interface) bus.

Mode selection is accomplished by means of combination of the MODE control logic pin, and the SPIEN control bit in Register 7 or Register 73. The following table shows the three functionally different modes that are supported.

MODE Pin	SPIEN bit R7[8]	SPIEN bit R73[8]	Description
0	0	0	2-Wire Interface, Read/Write operation
1	X "don't care"	0	SPI Interface 3-Wire Write-only operation
X "don't care"	X "don't care"	1	SPI Interface 4-Wire Read operation SPI Interface 4-Wire Write operation

Table 13: Control Interface Selection

The timing in all three bus configurations is fully static. This results in good compatibility with standard bus interfaces, and also, with software simulated buses. A software simulated bus can be very simple and low cost, such as by utilizing general purpose I/O pins on the host controller and software "bit banging" techniques to create the required timing.

9.2 2-Wire-Serial Control Mode (I^2C Style Interface)

The 2-wire bus is a bidirectional serial bus protocol. This protocol defines any device that sends data onto the bus as a transmitter (or master), and the receiving device as the receiver (or slave). The NAU8822A can function only as a slave device when in the 2-wire interface configuration.

9.3 2-Wire Protocol Convention

All 2-Wire interface operations must begin with a START condition, which is a HIGH-to-LOW transition of SDIO while SCLK is HIGH. All 2-Wire interface operations are terminated by a STOP condition, which is a LOW to HIGH transition of SDIO while SCLK is HIGH. A STOP condition at the end of a read or write operation places the device in a standby mode.

An acknowledge (ACK), is a software convention is used to indicate a successful data transfer. To allow for the ACK response, the transmitting device releases the SDIO bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDIO line LOW to acknowledge the reception of the eight bits of data.

Following a START condition, the master must output a device address byte. This consists of a 7-bit device address, and the LSB of the device address byte is the R/W (Read/Write) control bit. When R/W=1, this indicates the master is initiating a read operation from the slave device, and when R/W=0, the master is initiating a write operation to the slave device. If the device address matches the address of the slave device, the slave will output an ACK during the period when the master allows for the ACK signal.

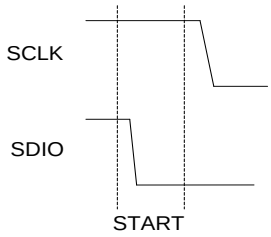


Figure 15: Valid START Condition

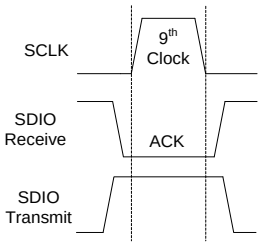


Figure 16: Valid Acknowledge

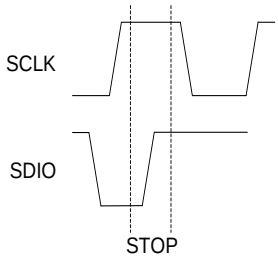


Figure 17: Valid STOP Condition

0	0	1	1	0	1	0	R/W	Device Address Byte
A7	A6	A5	A4	A3	A2	A1	A0	Control Address Byte
D7	D6	D5	D4	D3	D2	D1	D0	Data Byte

Figure 18: Slave Address Byte, Control Address Byte, and Data Byte

9.4 2-Wire Write Operation

A Write operation consists of a two-byte instruction followed by one or more Data Bytes. A Write operation requires a START condition, followed by a valid device address byte with R/W=0, a valid control address byte, data byte(s), and a STOP condition.

The NAU8822A is permanently programmed with "0011010" as the Device Address. If the Device Address matches this value, the NAU8822A will respond with the expected ACK signaling as it accepts the data being transmitted into it.

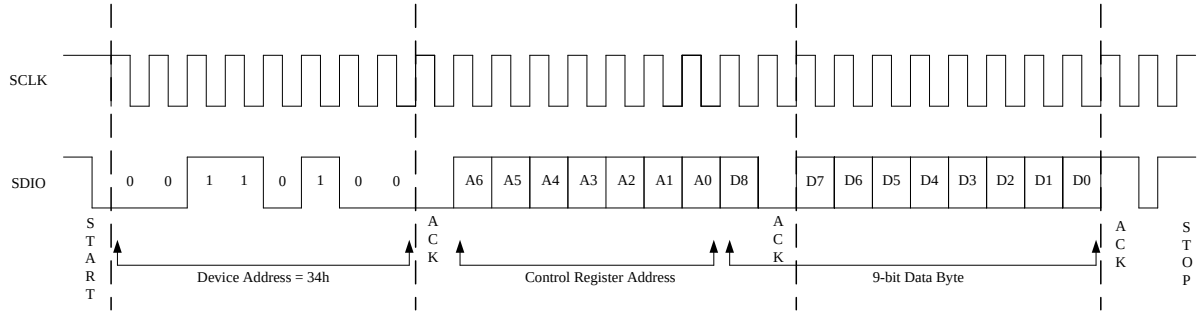


Figure 19: Byte Write Sequence

9.5 2-Wire Read Operation

A Read operation consists of a three-byte Write instruction followed by a Read instruction of one or more data bytes. The bus master initiates the operation issuing the following sequence: a START condition, device address byte with the R/W bit set to "0", and a Control Register Address byte. This indicates to the slave device which of its control registers is to be accessed.

The NAU8822A is permanently programmed with "0011010" as its device address. If the device address matches this value, the NAU8822A will respond with the expected ACK signaling as it accepts the Control Register Address

being transmitted into it. After this, the master transmits a second START condition, and a second instantiation of the same device address, but now with R/W=1.

After again recognizing its device address, the NAU8822A transmits an ACK, followed by a two byte value containing the nine bits of data from the selected control register inside the NAU8822A. Unused bits in the byte containing the MSB information from the NAU8822A are output by the NAU8822A as zeros.

During this phase, the master generates the ACK signaling with each byte transferred from the NAU8822A. If there is no STOP signal from the master, the NAU8822A will internally auto-increment the target Control Register Address and then output the two data bytes for this next register in the sequence.

This process will continue as long as the master continues to issue ACK signaling. If the Control Register Address being indexed inside the NAU8822A reaches the value 0x7F (hexadecimal) and the value for this register is output, the index will roll over to 0x00. The data bytes will continue to be output until the master terminates the read operation by issuing a STOP condition.

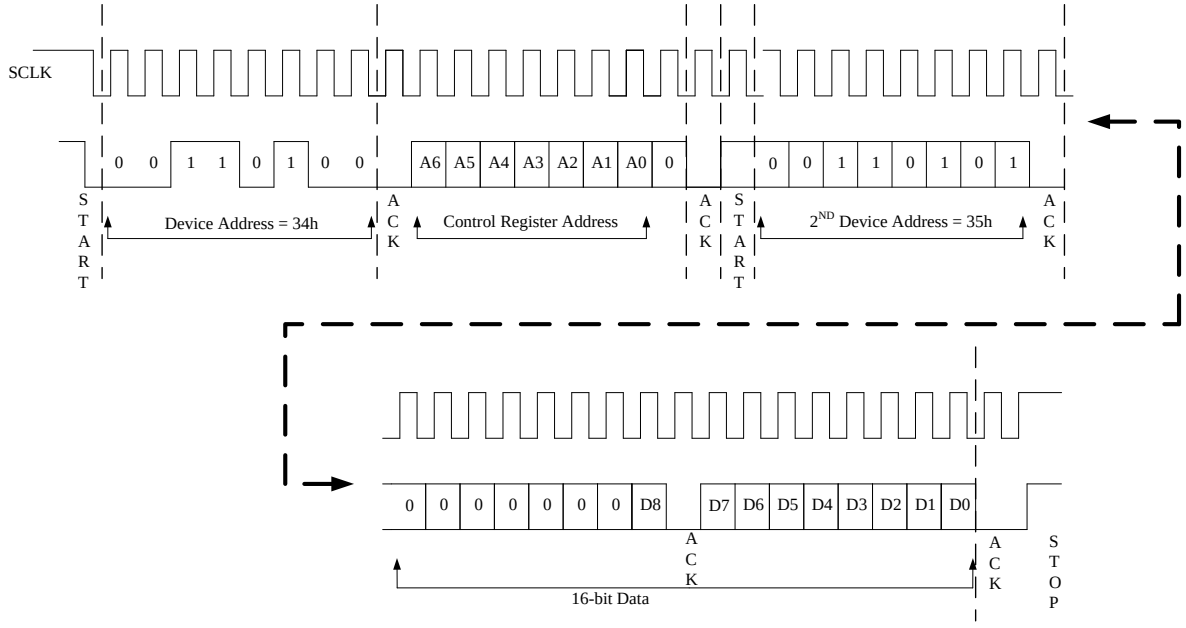


Figure 20: Read Sequence

9.6 SPI Control Interface Modes

The Serial Peripheral Interface (SPI) is a widely utilized interface protocol, and the NAU8822A supports two modes of SPI operation. When the MODE pin on the NAU8822A is in a logic HIGH condition, the device operates in the SPI 3-wire Write Mode. This is a write-only mode with a 16-bit transaction size. If the MODE pin is in a logic LOW condition, and the SPIEN control bit is set in Register 7, the SPI 4-wire Read/Write modes are enabled.

9.7 SPI 3-Wire Write Operation

Whenever the MODE pin on the NAU8822A is in the logic HIGH condition, the device control interface will operate in the 3-Wire Write mode. This is a write-only mode that does not require the fourth wire normally used to read data from a device on an SPI bus implementation. This mode is a 16-bit transaction consisting of a 7-bit Control Register Address, and 9-bits of control register data. In this mode, SDIO data bits are clocked continuously into a temporary holding register on each rising edge of SCLK, until the CSB pin undergoes a LOW-to-HIGH logic transition. At the time of the transition, the most recent 16-bits of data are latched into the NAU8822A, with the 9-bit data value being written into the NAU8822A control register addressed by the Control Register Address portion of the 16-bit value.

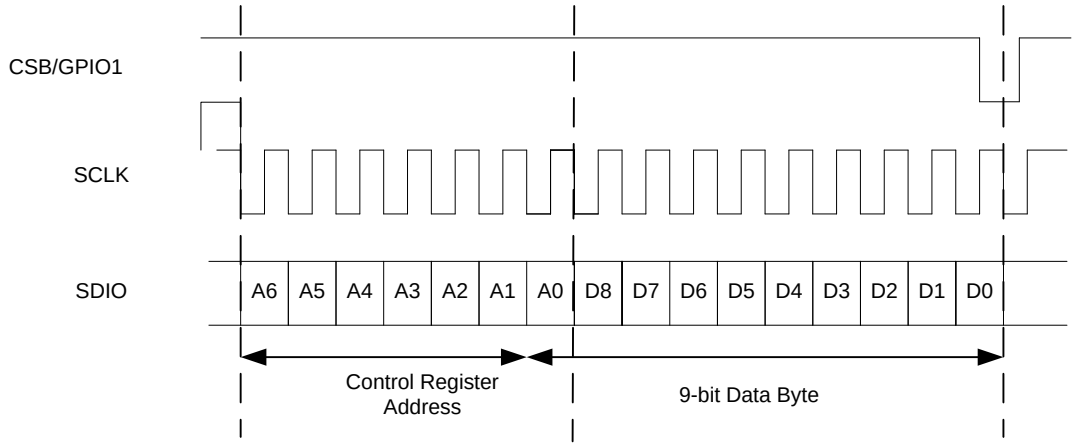


Figure 21: Register write operation using a 16-bit SPI Interface

9.8 SPI 4-Wire 24-bit Write and 32-bit Read Operation

The SPI 4-Wire Read/Write modes are enabled when the NAU8822A MODE pin is in a logic LOW condition, AND when the SPI Enable bit (SPIEN) is set in Register 7, Bit 8. Note that any time after either a hardware reset or software reset of the NAU8822A has occurred, the SPIEN bit must be set before the SPI 4-Wire Read/Write modes can be used. This must be done using either the SPI 3-Wire Write mode, or using the 2-Wire Write operation.

9.9 SPI 4-Wire Write Operation

The SPI 4-Wire write operation is a full SPI data transaction. However, only three wires are needed, as this is a write-only operation with no return data. A fourth wire is needed only when there are bi-directional data. The CSB/GPIO1 pin on the NAU8822A is used as the chip select function in the SPI transaction.

After CSB is held in a logic LOW condition, data bits from SDIO are clocked into the NAU8822A on every rising edge of SCLK. A write operation is indicated by the value 0x10 (hexadecimal) placed in the Device Address byte of the transaction. This byte is followed by a 7-bit Control Register Address and a 9-bit data value packed into the next two bytes of three-byte sequence. After the LSB of the Data Byte is clocked into the NAU8822A, the 9-bit data value is automatically transferred into the NAU8822A register addressed by the Control Register Address value.

If only a single register is to be written, CSB/GPIO must be put into a logic HIGH condition after the LSB of the Data Byte is clocked into the device. If CSB/GPIO1 remains in a logic LOW condition, the NAU8822A will auto-index the Control Register Address value to the next higher address, and the next two bytes will be clocked into the next sequential NAU8822A register address. This will continue as long as CSB/GPIO1 is in the logic LOW condition. If the Control Register Address being indexed inside the NAU8822A reaches the value 0x7F (hexadecimal), and after the value for this register is written, the index will roll over to 0x00 and the process will continue.

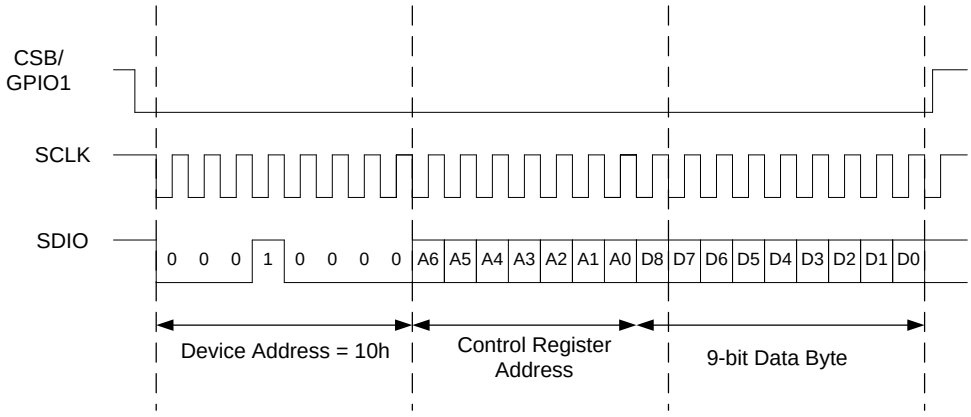


Figure 22: Register Write operation using a 24-bit SPI Interface

9.10 SPI 4-Wire Read Operation

The SPI 4-Wire Read operation is a full SPI data transaction with a two-byte address phase, and two-byte data phase. The CSB/GPIO1 pin on the NAU8822A is used as the chip select function in the SPI transaction.

After CSB is held in a logic LOW condition, data bits from SDIO are clocked into the NAU8822A on every rising edge of SCLK. A read operation is indicated by the value 0x20 (hexadecimal) placed in the Device Address byte of the transaction. This byte is followed by a 7-bit Control Register Address, padded by a non-used zero value in the LSB portion of the Control Register Address.

After the LSB of the Control Register Address is clocked, the NAU8822A will begin outputting its data on the GPIO3 pin, beginning with the very next SCLK rising edge. These data are transmitted in two bytes and contain the 9-bit value from the NAU8822A register selected by the Control Register Address. The data are transmitted MSB first, with the first 7-bits of the two byte value padded by zeros.

If only a single register is to be read, CSB/GPIO must be put into a logic HIGH condition after the LSB of the Data Byte 1 is clocked from the NAU8822A. If CSB/GPIO1 remains in a logic LOW condition, the NAU8822A will auto-index the Control Register Address value to the next higher address, and the next two bytes will be clocked from the next sequential NAU8822A register address. This will continue as long as CSB/GPIO1 is in the logic LOW condition. If the Control Register Address being indexed inside the NAU8822A reaches the value 0x7F (hexadecimal), and after the value for this register is output, the index will roll over to 0x00 and the process will continue.

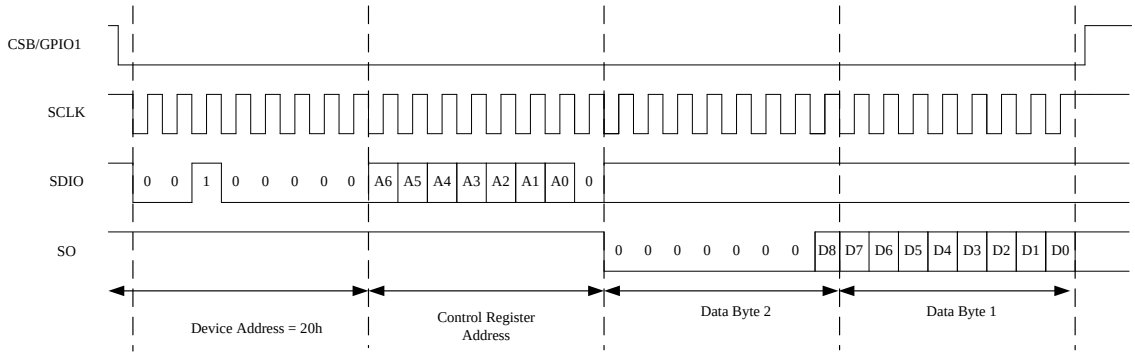


Figure 23: Register Read operation through a 32-bit SPI Interface

9.11 Software Reset

The entire NAU8822A and all of its control registers can be reset to default initial conditions by writing any value to Register 0, using any of the control interface modes. Writing to any other valid register address terminates the reset condition, but all registers will now be set to their power-on default values.

10 Digital Audio Interfaces

The NAU8822A can be configured as either the master or the slave, by setting register6, bit 0, to 1 for master mode and to 0 for slave mode. Slave mode is the default if this bit is not written. In master mode, NAU8822A outputs both Frame Sync (FS) and the audio data bit clock (BCLK,) has full control of the data transfer. In the slave mode, an external controller supplies BCLK and FS. Data are latched on the rising edge of BCLK; ADCOUT clocks out ADC data, while DACIN clocks in data for the DACs.

When not transmitting data, ADCOUT pulls LOW in the default state. Depending on the application, the output can be configured to pull-up or pull-down. To configure the output to pull up, write a 1 to register 60, bit 3 (PUDPS). When the time slot function is enabled (see below), there are additional output state modes including controlled tri-state capability.

NAU8822A supports six audio formats as shown in Table __, all with an MSB-first data format. The default mode is I^2S.

PCM Mode	Register 4, bits 3 -4 AIFF	Register 4, bit 7 LRP	Register 60, bit8 PCMTSEN
Right Justified	00	0	0
Left Justified	01	0	0
I^2S	10	0	0
PCM A	11	0	0
PCM B	11	1	0
PCM Time Slot	11	Don't care	1

Table 14: Digital Audio Interface Modes

10.1 Right-Justified Audio Data

In right-justified mode, the LSB is clocked on the last BCLK rising edge before FS transitions. When FS is HIGH, left channel data is transmitted and when FS is LOW, right channel data is transmitted.This is shown in the figure below.

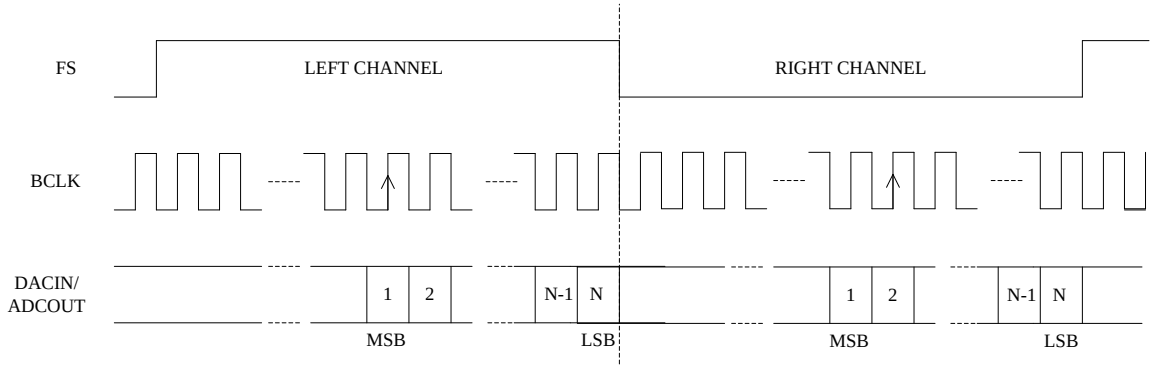


Figure 24: Right-Justified Audio Interface

10.2 Left-Justified Audio Data

In left-justified mode, the MSB is clocked on the first BCLK rising edge after FS transitions. When FS is HIGH, left channel data is transmitted and when FS is LOW, right channel data is transmitted. This is shown in the figure below.

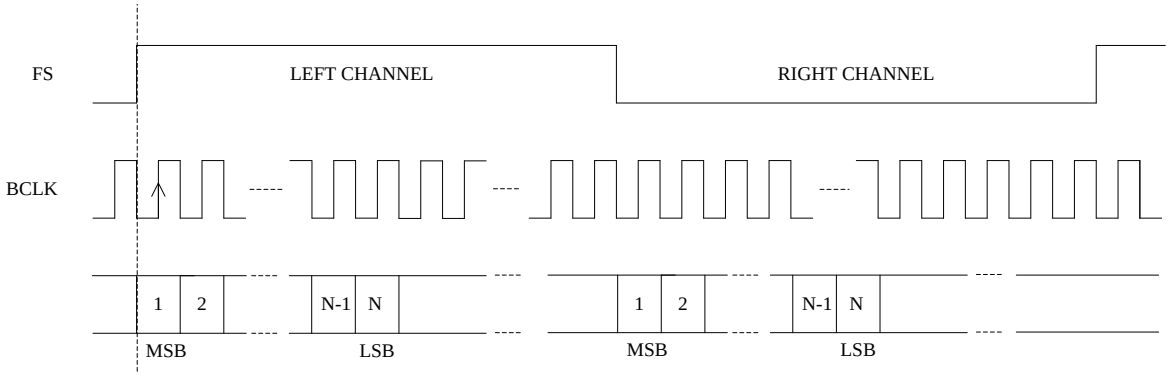


Figure 25: Left-Justified Audio Interface

10.3 I²S Audio Data

In I²S mode,the MSB is clocked on the second BCLK rising edge after FS transitions. When FS is LOW, left channel data is transmitted and when FS is HIGH, right channel data is transmitted. This is shown in the figure below.

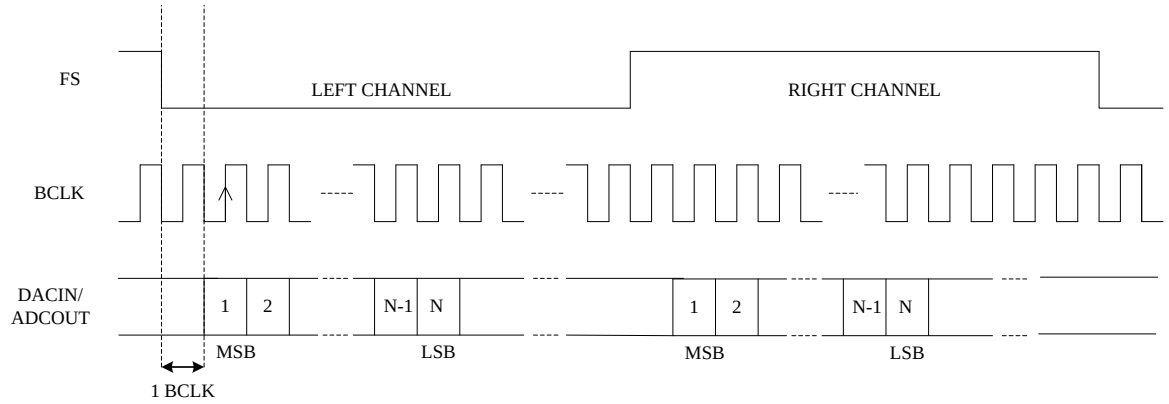


Figure 26: I2S Audio Interface

10.4 PCMA Audio Data

In the PCMA mode, left channel data is transmitted first followed immediately by right channel data. The left channel MSB is clocked on the second BCLK rising edge after the FS pulse rising edge, and the right channel MSB is clocked on the next SCLK after the left channel LSB. This is shown in the figure below.

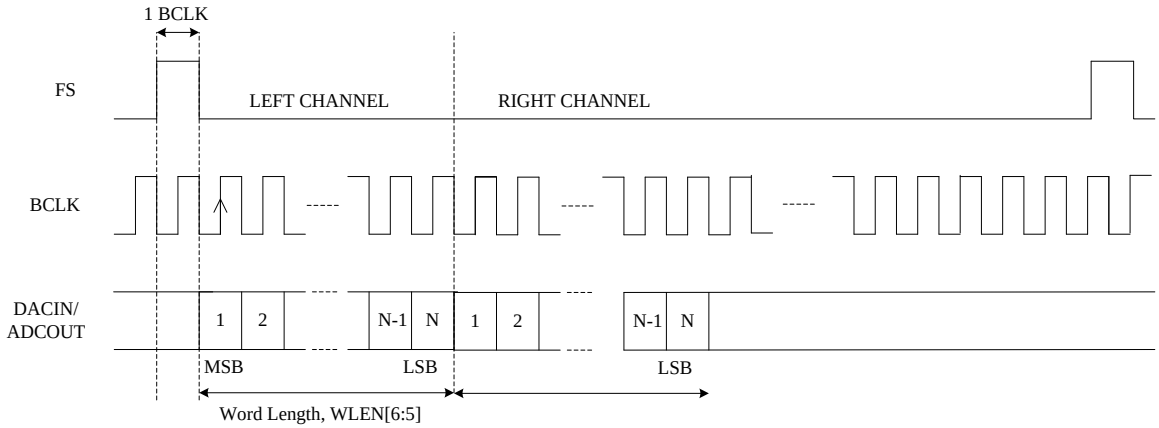


Figure 27: PCMA Audio Interface

10.5 PCMB Audio Data

In the PCM B mode, left channel data is transmitted first followed immediately by right channel data. The left channel MSB is clocked on the first BCLK rising edge after the FS pulse rising edge, and the right channel MSB is clocked on the next SCLK after the left channel LSB. This is shown in the figure below.

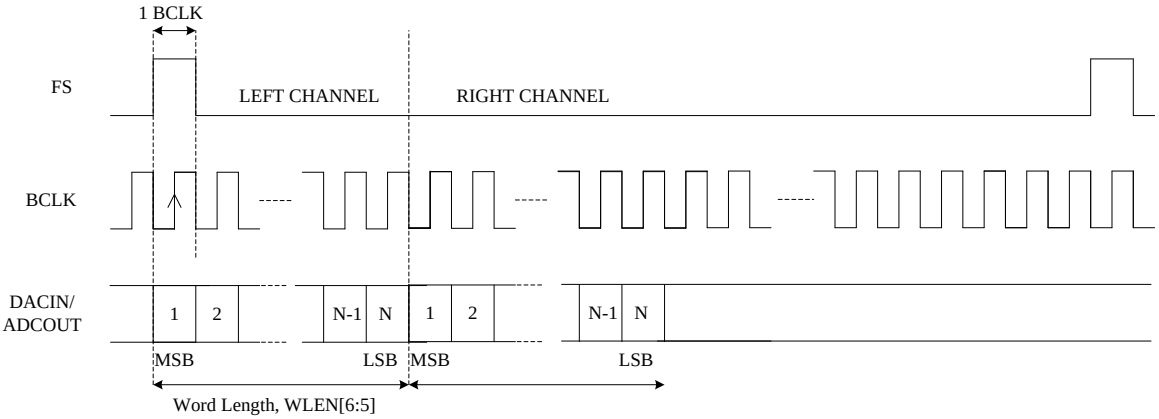


Figure 28: PCM-B Audio Interface

10.6 PCM Time Slot Audio Data

The PCM time slot mode is used to delay the time at which the DAC and/or ADC data are clocked. This increases the flexibility of the NAU8822A to be used in a wide range of system designs. One key application of this feature is to enable multiple NAU8822A or other devices to share the audio data bus, thus enabling more than two channels of audio. This feature may also be used to swap left and right channel data, or to cause both the left and right channels to use the same data.

Normally, the DAC and ADC data are clocked immediately after the Frame Sync (FS). In the PCM time slot mode, the audio data are delayed by a delay count specified in the device control registers. The left channel MSB is clocked on the BCLK rising edge defined by the delay count set in Registers 59 and 60. The right channel MSB is clocked on the BCLK rising edge defined by the delay count set in Registers 60 and 61.

Register 60 also controls ADCOUT output impedance options enabling the ADCOUT pin to share the same signal wire with other drivers. The default is the non-shared mode, with the output enable bit (PUDEN) set to logic=1. This results in the ADCOUT pin being actively driven at all times (never in a high-impedance state).

However, if PUDEN is logic=0, and PUDPE (pull-up/down enable) is logic=1, then ADCOUT will be pulled HIGH or LOW by means of an internal passive resistor. This enables wired-OR type bus sharing. The choice of passive pull-up, or passive pull-down is determined by the PUDPS (pull-up/down select) bit.

If PUDEN and PUDPE are both logic=0, ADCOUT is high impedance, except when actively transmitting left and right channel audio data. After outputting audio channel data, ADCOUT will return to high impedance on the BCLK negative edge during the LSB data period if Register 60, bit 7 (TRI), is HIGH, or on the BCLK positive edge of LSB if Register 60, bit 7 (TRI), is LOW. Tri-stating on the negative edge allows the transmission of data by multiple sources in adjacent timeslots with reduced risk of bus driver contention.

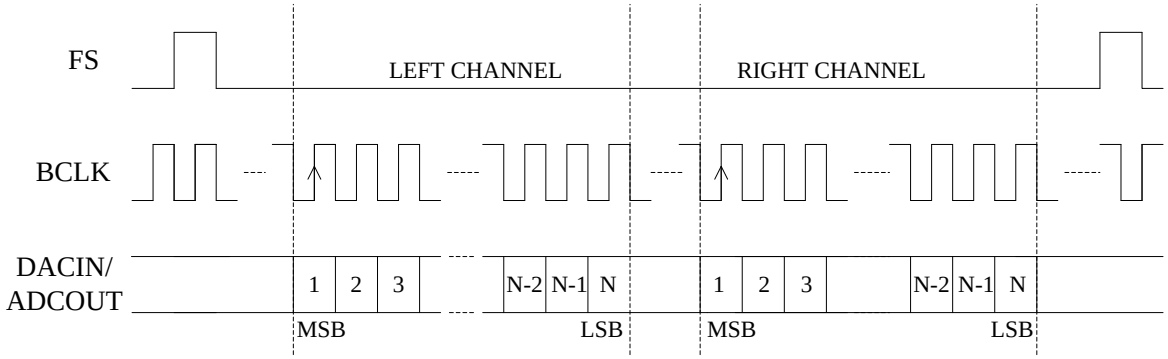


Figure 29: PCM Time Slot Audio Interface

10.7 Control Interface Timing

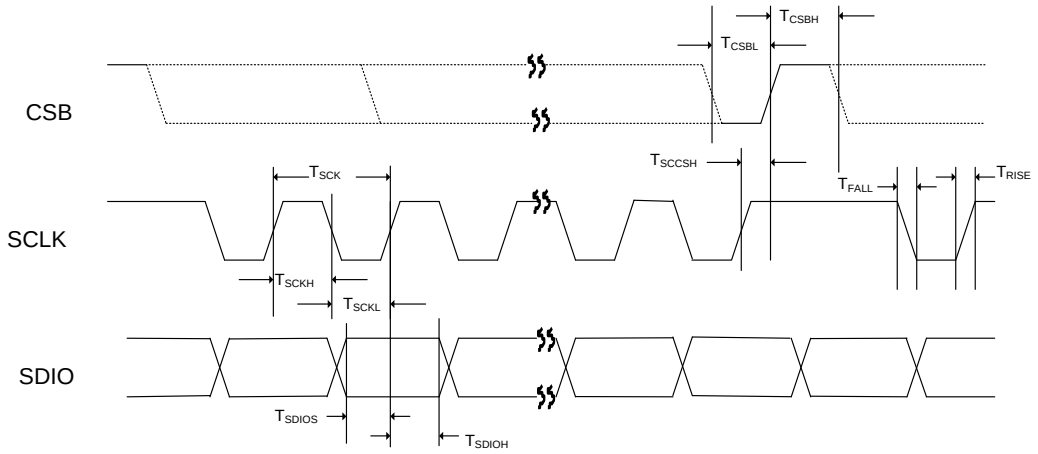


Figure 30: 3-wire ControlMode Timing

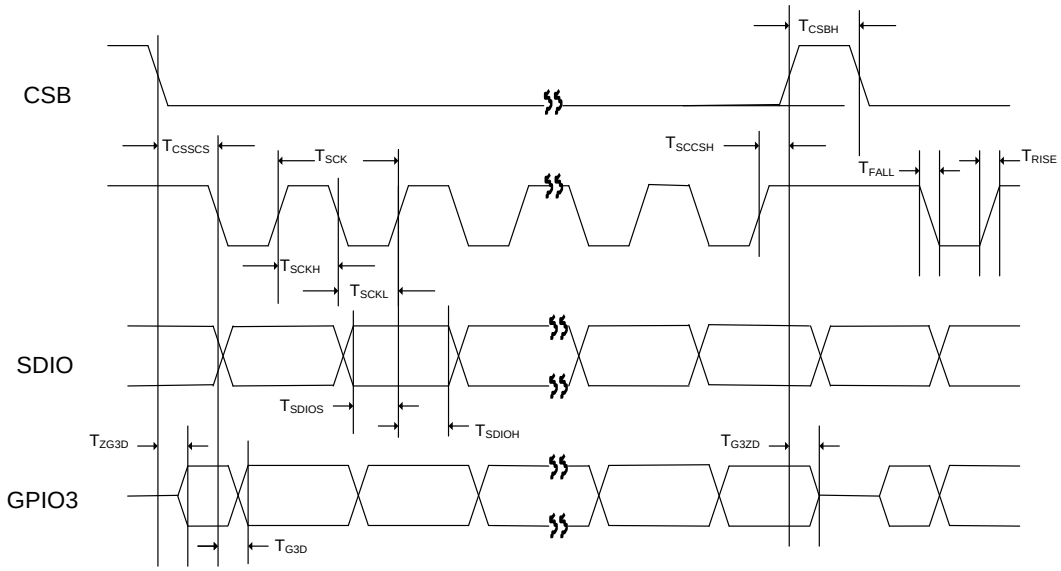


Figure 31: 4-wire ControlMode Timing

Symbol	Description	min	typ	max	unit
T_{SCK}	SCLK Cycle Time	80	-	-	ns
T_{SCKH}	SCLK High Pulse Width	35	-	-	ns
T_{SCKL}	SCLK Low Pulse Width	35	-	-	ns
T_{RISE}	Rise Time for all Control Interface Signals	-	-	10	ns
T_{FALL}	Fall Time for all Control Interface Signals	-	-	10	ns
T_{CSSCS}	CSB Falling Edge to 1st SCLK Falling Edge Setup Time (4 wire Mode Only)	30	-	-	ns
T_{SCCSH}	Last SCLK Rising Edge to CSB Rising Edge Hold Time	30	-	-	ns
T_{CSBL}	CSB Low Time	30	-	-	ns
T_{CSBH}	CSB High Time between CSB Lows	30	-	-	ns
T_{SDIOS}	SDIO to SCLK Rising Edge Setup Time	20	-	-	ns
T_{SDIOH}	SCLK Rising Edge to SDIO Hold Time	20	-	-	ns
T_{ZG3D}	Delay Time from CSB Falling Edge to GPIO3 Active (4 wire Mode Only)	--	--	15	ns
T_{G3ZD}	Delay Time from CSB Rising Edge to GPIO3 Tri-state (4-wire Mode Only)	--	--	15	ns
T_{G3D}	Delay Time from SCLK Falling Edge to GPIO3 (4-wire Mode Only)	-	-	15	ns

Table 15: Three- and Four Wire Control Timing Parameters

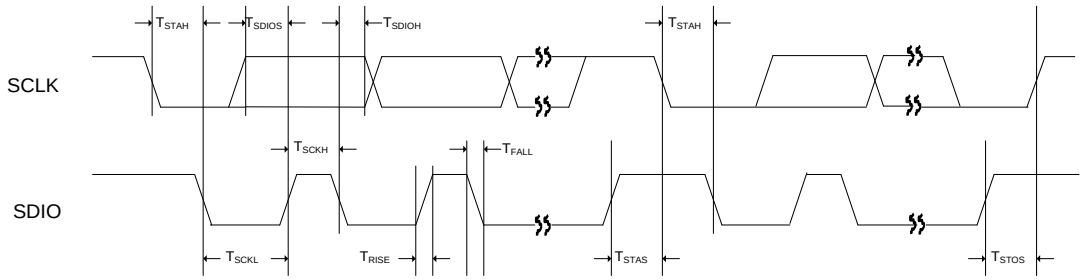


Figure 32: Two-wire Control Mode Timing

Symbol	Description	min	typ	max	unit
T_{STAH}	SCLK falling edge to SDIO falling edge hold timing in START / Repeat START condition	600	-	-	ns
T_{STAS}	SDIO rising edge to SCLK falling edge setup timing in Repeat START condition	600	-	-	ns
T_{STOS}	SDIO rising edge to SCLK rising edge setup timing in STOP condition	600	-	-	ns
T_{SCKH}	SCLK High Pulse Width	600	-	-	ns
T_{SCKL}	SCLK Low Pulse Width	1,300	-	-	ns
T_{RISE}	Rise Time for all 2-wire Mode Signals	-	-	300	ns
T_{FALL}	Fall Time for all 2-wire Mode Signals	-	-	300	ns
T_{SDIOS}	SDIO to SCLK Rising Edge DATA Setup Time	400	-	-	ns
T_{SDIOH}	SCLK falling Edge to SDIO DATA Hold Time	0	-	600	ns

Table 16: Two-wire Control Timing Parameters

10.8 Audio Interface Timing:

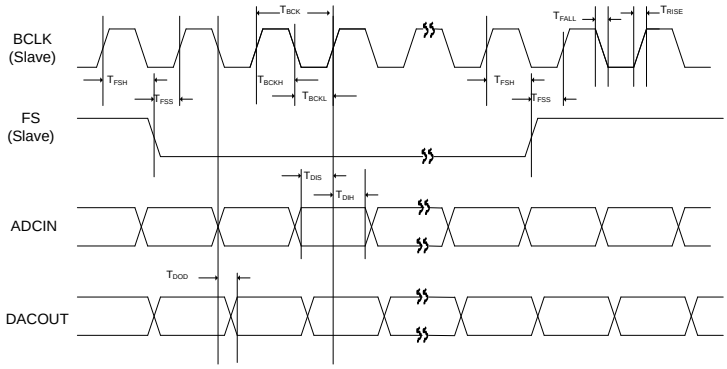


Figure 33: Digital Audio Interface Slave Mode Timing

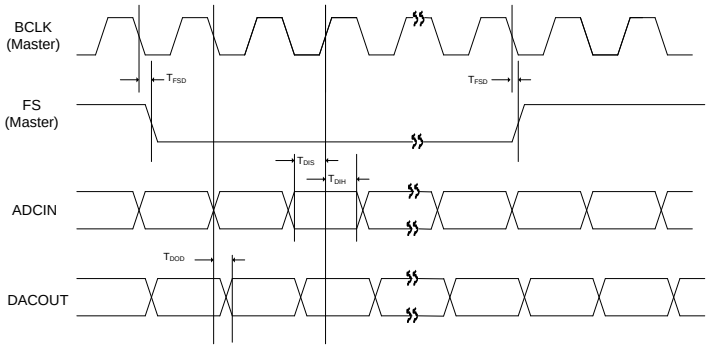


Figure 34: Digital Audio Interface Master Mode Timing

Symbol	Description	min	typ	max	unit
T_{BCK}	BCLK Cycle Time in Slave Mode	50	-	-	ns
T_{BCKH}	BCLK High Pulse Width in Slave Mode	20	-	-	ns
T_{BCKL}	BCLK Low Pulse Width in Slave Mode	20	-	-	ns
T_{FSS}	FS to BCLK Rising Edge Setup Time in Slave Mode	20	-	-	ns
T_{FSH}	BCLK Rising Edge to FS Hold Time in Slave Mode	20	-	-	ns
T_{FSD}	BCLK Falling Edge to FS Delay Timein Master Mode	-	-	10	ns
T_{RISE}	Rise Time for All Audio Interface Signals	-	-	10	ns
T_{FALL}	Fall Time for All Audio Interface Signals	-	-	10	ns
T_{DIS}	ADCIN to BCLK Rising Edge Setup Time	15	-	-	ns
T_{DIH}	BCLK Rising Edge to ADCIN Hold Time	15	-	-	ns
T_{DOD}	BCLK Falling Edge to DACOUT Delay Time	-	-	10	ns

Table 17: Audio Interface Timing Parameters

11 Application Information

11.1 Typical Application Schematic

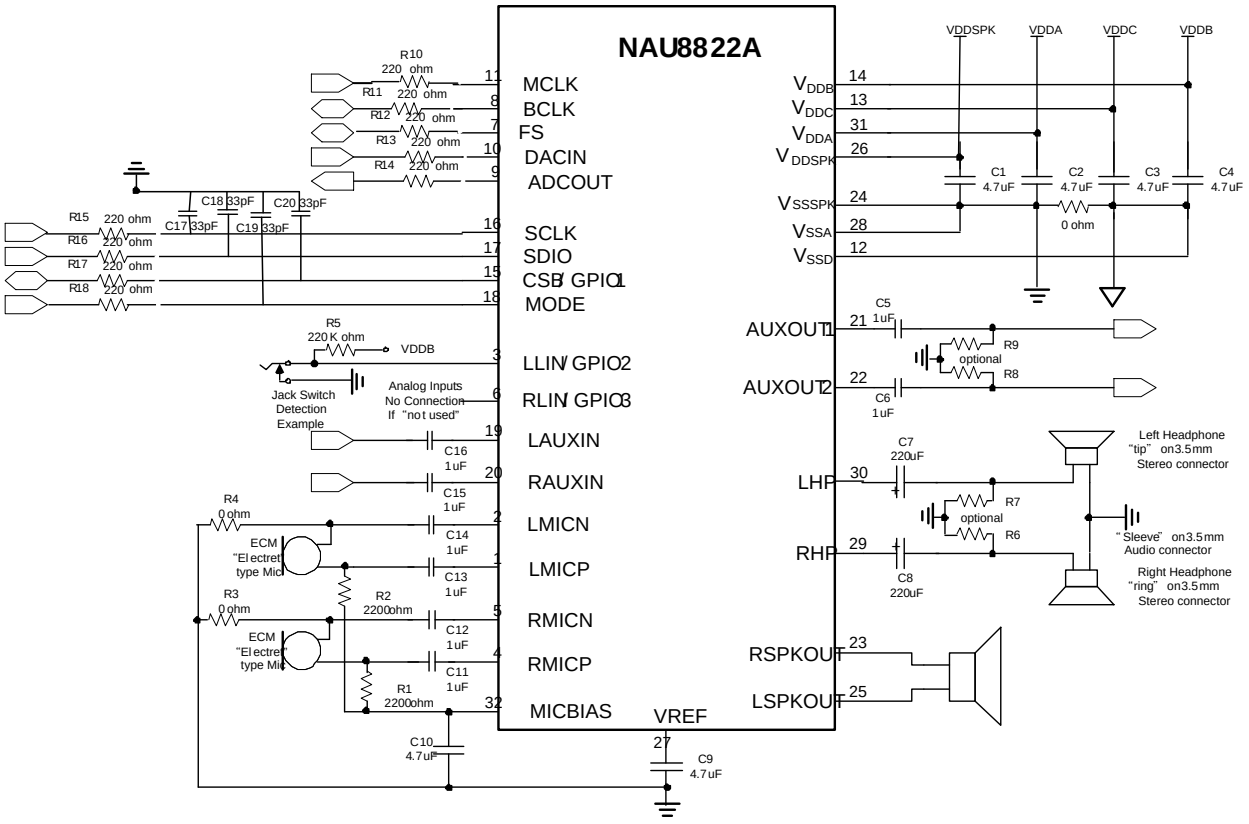


Figure 35: Schematic with recommended external components for typical application with AC-coupledheadphones and stereo electret (ECM) style microphones.

Note 1: All non-polar capacitors are assumed to be low ESR type parts, such as with MLC construction or similar. If capacitors are not low ESR, additional 0.1ufd and/or 0.01ufd capacitors may be necessary in parallel with the bulk 4.7ufd capacitors on the supply rails.

Note 2: Load resistors to ground on outputs may be helpful in some applications to insure a DC path for the output capacitors to charge/discharge to the desired levels. If the output load is always present and the output load provides a suitable DC path to ground, then the additional load resistors may not be necessary. If needed, such load resistors are typically a high value, but a value dependent upon the application requirements.

Note 3: To minimize pops and clicks, large polarized output capacitors should be a low leakage type.

Note 4: Depending on the microphone device and PGA gain settings, common mode rejection can be improved by choosing the resistors on each node of the microphone such that the impedance presented to any noise on either microphone wire is equal.

Note 5: Unused analog input pins should be left as no-connection.

Note 6: Unused digital input pins should be tied to ground.

Note 7: R15-R18 and C17-C20 are low pass filters to reduce glitch; the corner frequency are from 8MHz to 33MHz depending on PCB parasitics

11.2 Recommended power up and power down sequences

To minimize pop and click noise, the NAU8822A should be powered up and down using the procedures in this section as guidance. The power-up procedure should be followed upon system power-up, or after any time that the NAU8822A has been issued a register reset command.

The strongest cause of pops and clicks in most system is the sudden charging or discharging of capacitors used for AC-coupling to inputs and outputs. Any sudden change in voltage will cause a pop or click, with or without AC-coupling capacitors in the signal path. The general strategy for pop and click reduction is to allow such charging and discharging to happen slowly.

11.2.1 Power Up (and after a software generated register reset) Procedure Guidance

Turn on external power supplies and wait for supply voltages to settle. This amount of time will be dependent on the system design. Software may choose to test the NAU8822A to determine when it is no longer in an active reset condition. This procedure is described in more detail in the sections relating to power supplies.

If the VDDSPK supply voltage is 3.60V or less, the next step should be to configure all of the output registers for low voltage operation. This sets the internal DC levels and gains to optimal levels for operation at lower voltages. Register settings required for this are:

R49 Bit 2, SPKBST; Bit 3, AUX2BST; Bit 4, AUX1BST, set to logic = 1

As a general policy, it is a good idea to put any input or output driver paths into the “mute” condition any time internal register and data path configurations are being changed. Be sure at this time that all used inputs and outputs are in their muted/disconnected condition.

Next, the internal DC tie-off voltage buffers should be enabled:

R1 Bit 2, IOBUFEN, set to logic = 1
R1 Bit 8, DCBUFEN, set to logic = 1 if setting up for greater than 3.60V operation

Value to be written to R1 = 0x104

At this point, the NAU8822A has been prepared to start charging any input/output capacitors to their normal operating mode charge state. If this is done slowly, then there will be no pops and clicks. One way to accomplish this is to allow the internal/external reference voltage to charge slowly by means of its internal coupling resistors. This is accomplished by:

R1 Bits 1, Bit 0, REFIMP set to 80kΩ setting
R1 Bit 2, ABIASEN, set to logic = 1
Value to be written to R1 = 0x10D

After this, the system should wait approximately 250ms, or longer, depending on the external components that have been selected for a given specific application.

After this, outputs may be enabled, but with the drivers still in the mute condition. Unless power management requires outputs to be turned off when not used, it is best for pops and clicks to leave outputs enabled at all times, and to use the output mute controls to silence the outputs as needed.

Next, the NAU8822A can be programmed as needed for a specific application. The final step in most applications will be to unmute any outputs, and then begin normal operation.

11.2.2 Power Down

Powering down is more application specific. The most important step is to mute all outputs before any other steps. It then may be further helpful to disable all outputs just before the system power-down sequence is started.

11.2.3 Unused Input/Output Tie-Off Information

In audio and voice systems, any time there is a sudden change in voltage to an audio signal, an audible pop or click sound may be the result. Systems that change inputs and output configurations dynamically, or which are required to manage low power operation, need special attention to possible pop and click situations.

The NAU8822A includes many features which may be used to greatly reduce or eliminate pop and click sounds. The most common cause of a pop or click signal is a sudden change to an input or output voltage. This may happen in either a DC coupled system, or in an AC coupled system.

The strategy to control pops and clicks is similar for either a DC coupled system, or an AC coupled system. The case of the AC coupled system is the most common and the more difficult situation, and therefore, the AC coupled case will the focus for this information section.

When an input or output pin is being used, the DC level of that pin will be very close to ½ of the VDDA voltage that is present on the VREF pin. The only exception is that when outputs are operated in the 5-Volt mode known as the 1.5X boost condition, then the DC level for those outputs will be equal to 1.5xVREF.

In all cases, any input or output capacitors will become charged to the operating voltage of the used input or output pin. The goal to reduce pops and clicks is to insure that the charge voltage on these capacitors does not change suddenly at any time.

When an input or output is in a not-used operating condition, it is desirable to keep the DC voltage on that pin at the same voltage level as the DC level of the used operating condition. This is accomplished using special internal DC voltage sources that are at the required DC values. When an input or output is in the not-used condition, it is connected to the correct internal DC voltage as not to have a pop or click. This type of connection is known as a “tie-off” condition.

Two internal DC voltage sources are provided for making tie-off connections. One DC level is equal to the VREF voltage value, and the other DC level is equal to 1.5X the VREF value. All inputs are always tied off to the VREF voltage value. Outputs will automatically be tied to either the VREF voltage value or to the 1.5xVREF value, depending on the value of the “boost” control bit for that output. That is to say, when an output is set to the 1.5X gain condition, then that same output will automatically use the 1.5xVREF value for tie-off in the not-used condition.

To conserve power, these internal voltage buffers may be enabled/disabled using control register settings. To better manage pops and clicks, there is a choice of impedance of the tie-off connection for unused outputs. The nominal values for this choice are 1kΩ and 30kΩ. The low impedance value will better maintain the desired DC level in the case when there is some leakage on the output capacitor or some DC resistance to ground at the NAU8822A output pin. A tradeoff in using the low-impedance value is primarily that output capacitors could change more suddenly during power-on and power-off changes.

Automatic internal logic determines whether an input or output pin is in the used or un-used condition. This logic function is always active. An output is determined to be in the un-used condition when it is in the disabled unpowered condition, as determined by the power management registers. An input is determined to be in the un-used condition when all internal switches connected to that input are in the “open” condition.

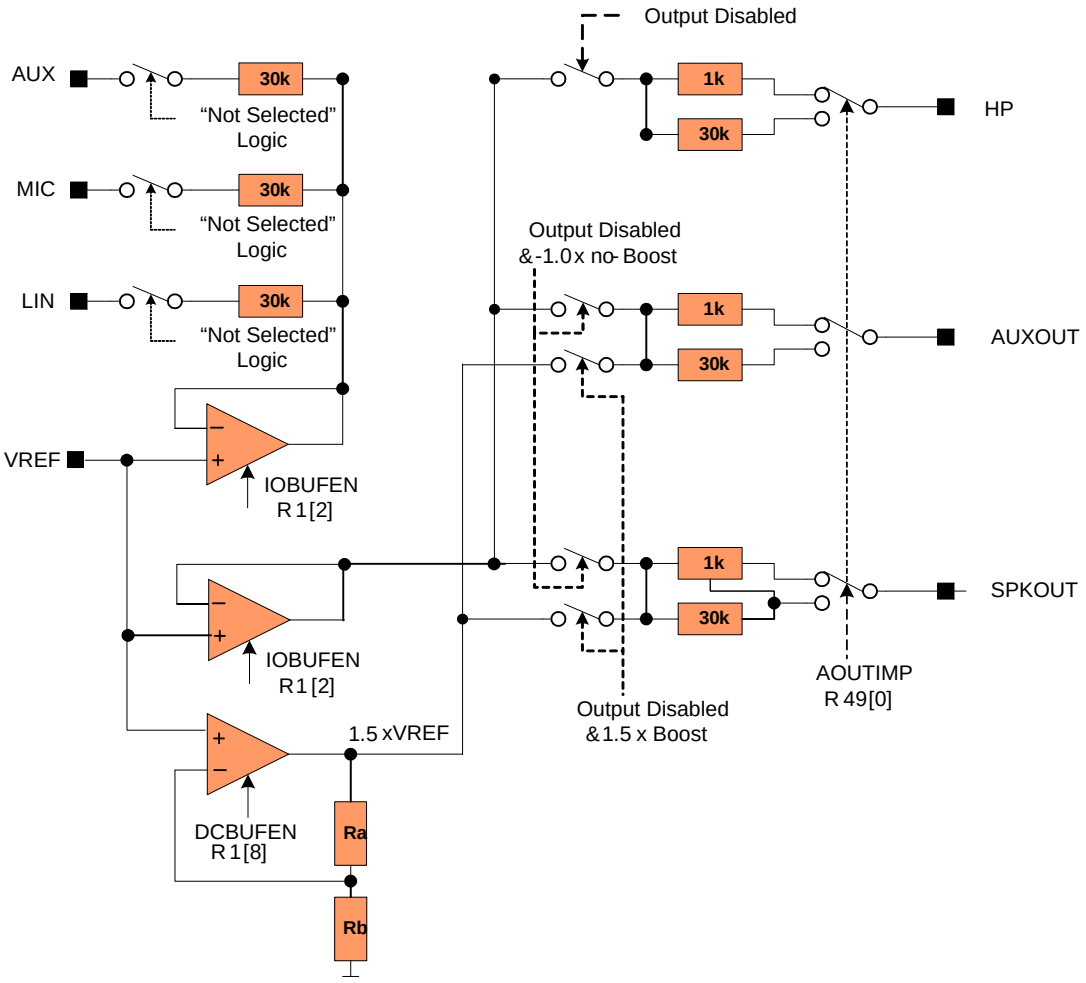


Figure 36: Tie-off Options for input and output pin examples

Register controls that directly affect the tie-off features are:

Register 1	Enable buffers for 1.0xVREF tie-off
Register 1	Enable buffer for 1.5xVREF tie-off
Register 49	Tie-off impedance selection
Register 74	Input tie-off management and manual overrides
Register 75	Input tie-off buffer controls and manual overrides
Register 79	Output tie-off buffer controls and manual overrides

Note: Resistor tie-off switches will open/close regardless of whether or not the associated internal DC buffer is in the enabled or disabled condition.

11.3 Power Consumption

The NAU8822A has flexible power management capability which allows sections not being used to be powered down, to draw minimum current in battery-powered applications. The following table shows typical power consumption in different operating conditions. The "off" condition is the initial power-on state with all subsystems powered down, and with no applied clocks.

Mode	Conditions	VDDA = 3V	VDDC = 1.8V	VDDB = 3V	Total Power
		mA	mA	mA	mW
OFF		0.008	0.001	0.0003	0.025
Sleep	VREF maintained @ 300kΩ, no clocks,	0.008	0.001	0.0003	0.025
	VREF maintained @ 75kΩ, no clocks,	0.014	0.001	0.0003	0.045
	VREF maintained @ 5kΩ, no clocks,	0.259	0.001	0.0003	0.781
Stereo Record	8kHz, 0.9Vrms input signal	6.44	1.07	0.10	21.5
	8kHz, 0.9Vrms input signal, PLL on	7.42	1.33	0.10	24.9
Stereo Playback	16Ω HP, 44.1kHz, quiescent	7.25	6.10	0.03	32.8
	16Ω HP, 44.1kHz, quiescent, PLL on	9.77	7.53	0.025	42.9
	16Ω HP, 44.1kHz, 0.6 Vrms sine wave	21.3	6.28	0.015	75.2
	16Ω HP, 44.1kHz, 0.6Vrms sine, PLL on	23.8	7.72	0.015	85.3

Table 18: Typical Power Consumption in Various Application Modes.

11.4 Supply Currents of Specific Blocks

The NAU8822A can be programmed to enable/disable various analog blocks individually, and the current to some of the major blocks can be reduced with minimum impact on performance. The table below shows the change in current consumed with different register settings. Sample rate settings affect current consumption of VDDC supply. Lower sampling rates draw lower current.

Register		Function	Bit	VDDA current increase/ Decrease when enabled
Dec	Hex			
1	01	Power Management 1	REFIMP[1:0]	+100µA for 80kΩ and 300kΩ +260µA for 3kΩ
			IOBUFEN[2]	+100µA
			ABIASEN[3]	+600µA
			MICBIASEN[4]	+540µA
			PLLEN[5]	+2.5 mA +1/5mA from VDDCwith clocks applied
			AUX2MXEN[6]	+200µA
			AUX1MXEN[7]	+200µA
			DCBUFEN[8]	+140µA
2	02	Power Management 2	LADCEN[0]	+2.3 mA with 64X OSR +3.3 mA with 128X OSR
			RADCEN[1]	+2.3 mA with 64X OSR +3.3 mA with 128X OSR
			LPGAEN[2]	+300µA
			RPGAEN[3]	+300µA
			LBSTEN[4]	+650µA
			RBSTEN[5]	+650µA
			SLEEP[6]	Same as PLLEN (R1[5])
			LHPEN[7]	+800µA
			RHPEN[8]	+800µA
3	03	Power Management 3	LDACEN[0]	+1.6 mA with 64X OSR +1.7 mA with 128X OSR
			RDACEN[1]	+1.6 mA with 64X OSR +1.7 mA with 128X OSR
			LMIXEN[2]	+250µA
			RMIXEN[3]	+250µA
			RSPKEN[5]	+1.1 mA from VDDSPK

Register		Function	Bit	VDDA current increase/ Decrease when enabled
Dec	Hex			
			LSPKEN[6]	+1.1 mA from VDDSPK
			AUXOUT2EN[7] AUXOUT1EN[8]	+225µA +225µA
58	3A	Power Management 4	IBIADJ[1:0]	-1.2mA with IBIADJ at 11
			REGVOLT[2:3]	
			MICBIASM[4]	
			LPSPKD[5]	
			LPADC[6]	-1.1mA with no SNR decrease @ 8kHz
			LPIPBST[7]	-600µA with no SNR decrease @ 8kHz
			LPDAC[8]	-1.1mA with 1.4dB SNR decrease @ 44.1kHz

Table 19: VDDA 3.3V Supply Current in Various Modes

12 Appendix A: Digital Filter Characteristics

Parameter	Conditions	Min	Typ	Max	Units
ADC Filter					
Passband	+/- 0.015dB	0		0.454	fs
	-6dB		0.5		fs
Passband Ripple				+/-0.015	dB
Stopband		0.546			fs
Stopband Attenuation	f > 0.546*fs	-60			dB
Group Delay			28.25		1/fs
ADCHighPass Filter					
HighPass Filter Corner Frequency	-3dB		3.7		Hz
	-0.5dB		10.4		Hz
	-0.1dB		21.6		Hz
DAC Filter					
Passband	+/- 0.035dB	0		0.454	fs
	-6dB		0.5		fs
Passband Ripple				+/-0.035	dB
Stopband		0.546			fs
Stopband Attenuation	f > 0.546*fs	-55			dB
Group Delay			28		1/fs

Table 20: Digital Filter Characteristics

TERMINOLOGY

1. Stop Band Attenuation (dB) – the degree to which the frequency spectrum is attenuated (outside audio band)
2. Pass-band Ripple – any variation of the frequency response in the pass-band region
3. Note that this delay applies only to the filters and does not include other latencies, such as from the serial data interface

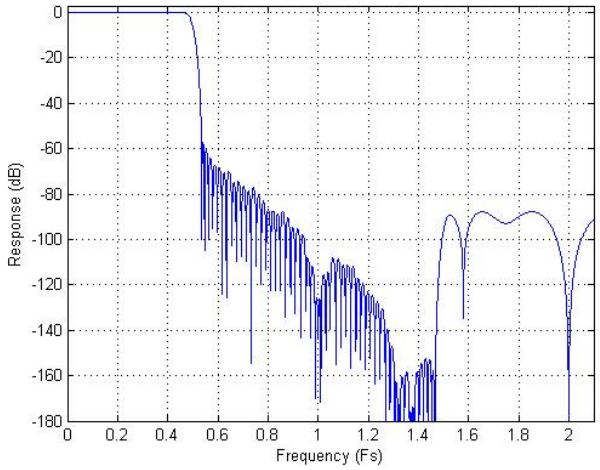


Figure 37: DAC Filter Frequency Response

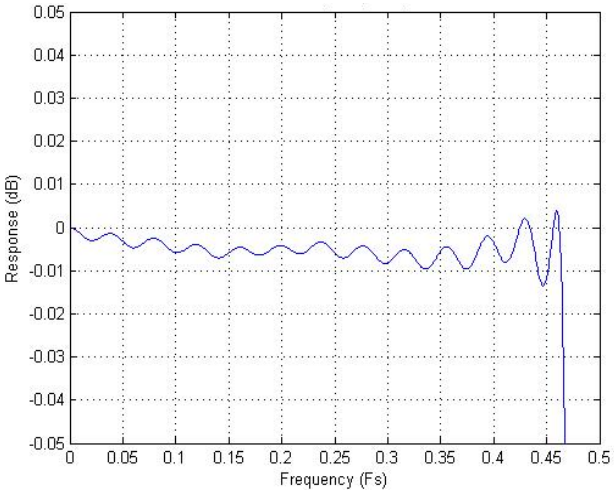


Figure 38: DAC Filter Ripple

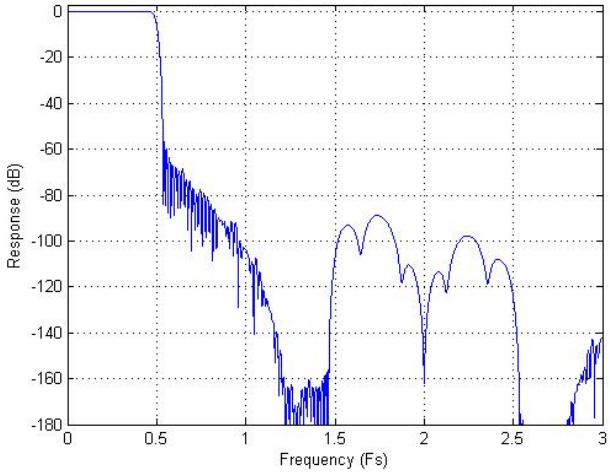


Figure 39: ADC Filter Frequency Response

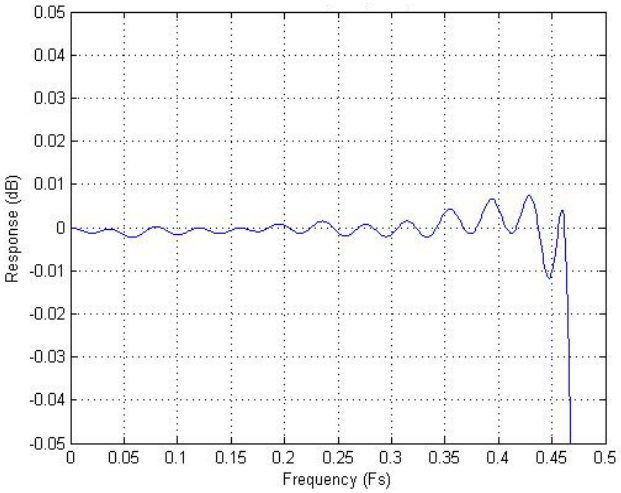


Figure 40: ADC Filter Ripple

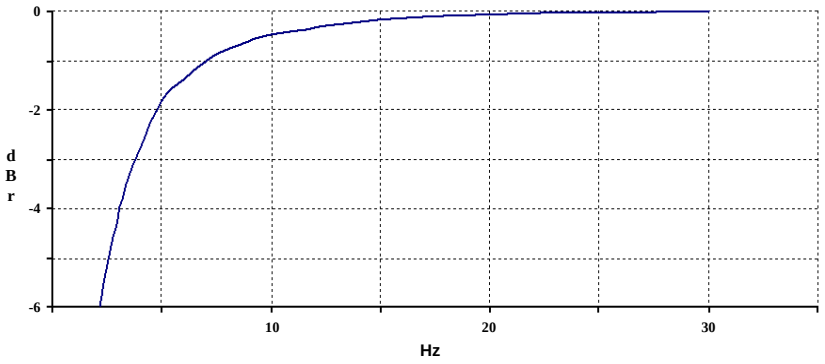


Figure 41: ADC Highpass Filter Response, Audio Mode

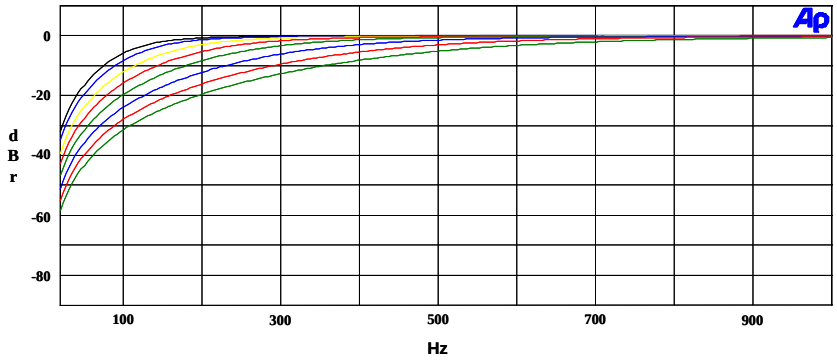


Figure 42: ADC Highpass Filter Response, HPF enabled, FS = 48kHz

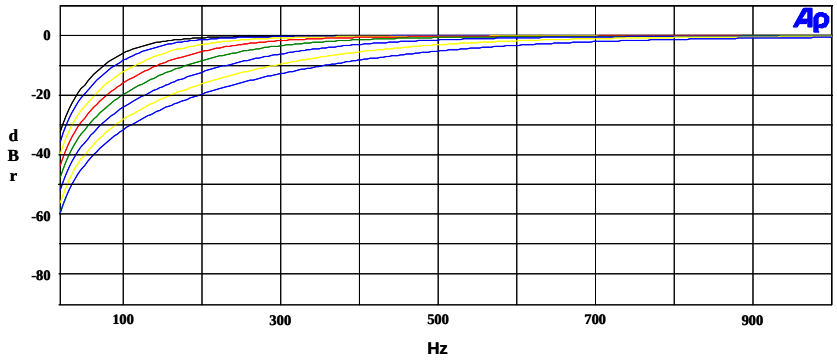


Figure 43: ADC Highpass Filter Response, HPF enabled, FS = 24kHz

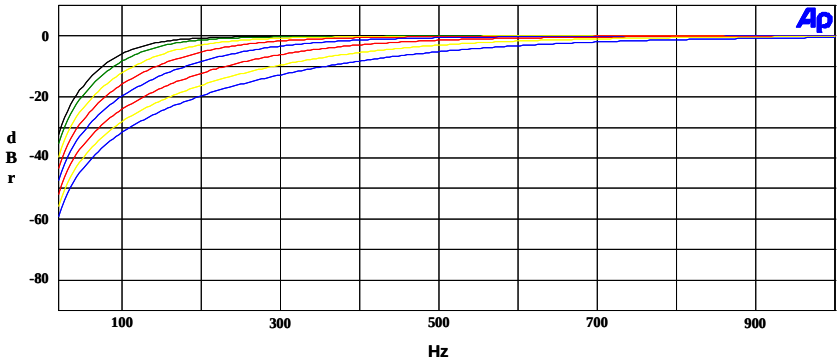


Figure 44: ADC Highpass Filter Response, HPF enabled, FS = 12kHz

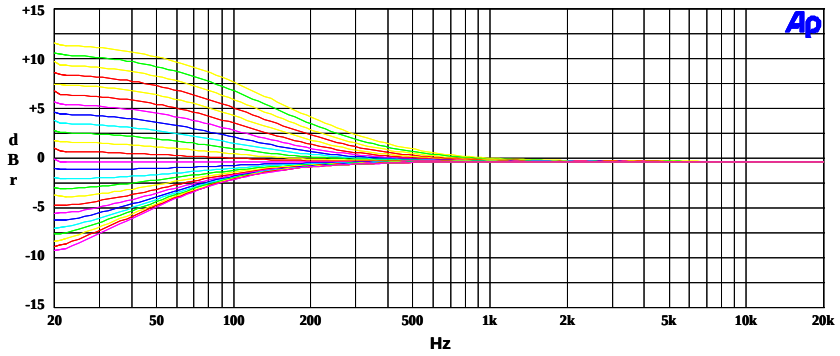


Figure 45: EQ Band 1 Gains for Lowest Cut-Off Frequency

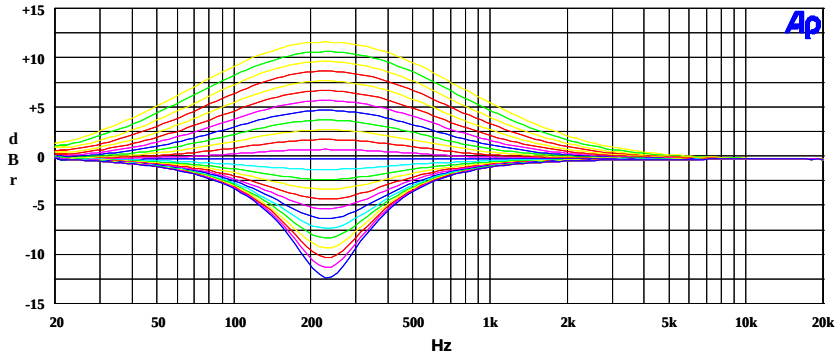


Figure 46: EQ Band 2 Peak Filter Gains for Lowest Cut-Off Frequency with EQ2BW = 0

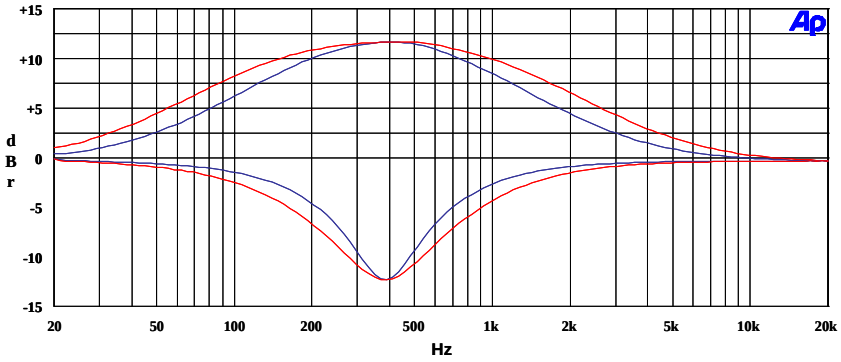


Figure 47: EQ Band 2, EQ2BW = 0 versus EQ2BW = 1

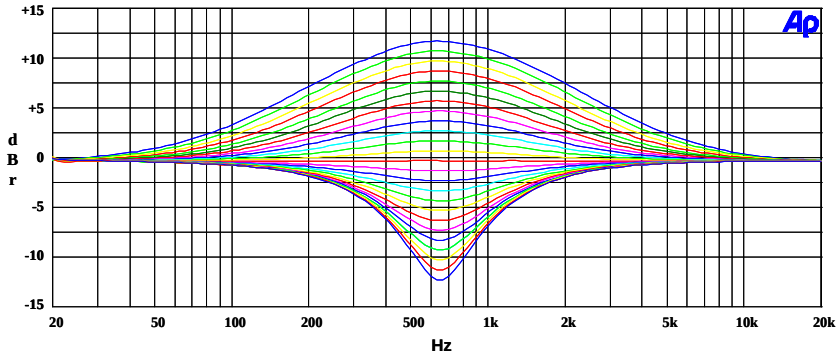


Figure 48: EQ Band 3 Peak Filter Gains for Lowest Cut-Off Frequency with EQ3BW = 0

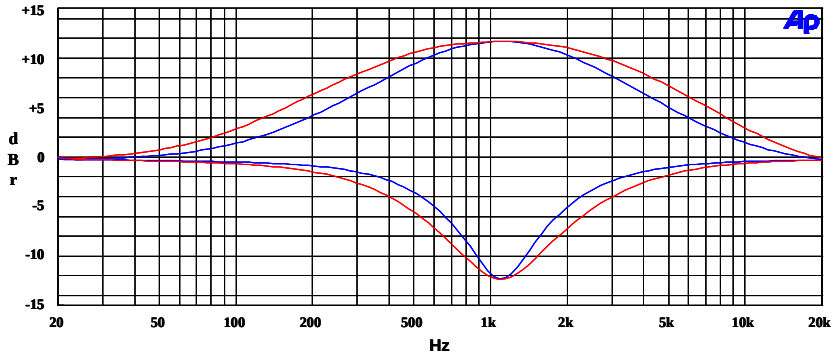


Figure 49: EQ Band 3, EQ3BW = 0 versus EQ3BW = 1

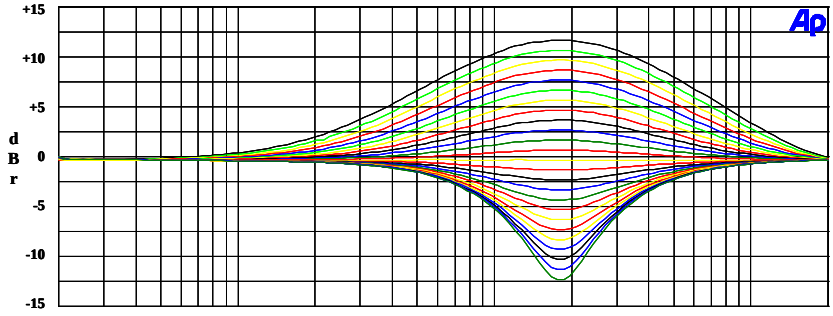


Figure 50: EQ Band 4 Peak Filter Gains for Lowest Cut-Off Frequencies with EQ4BW = 0

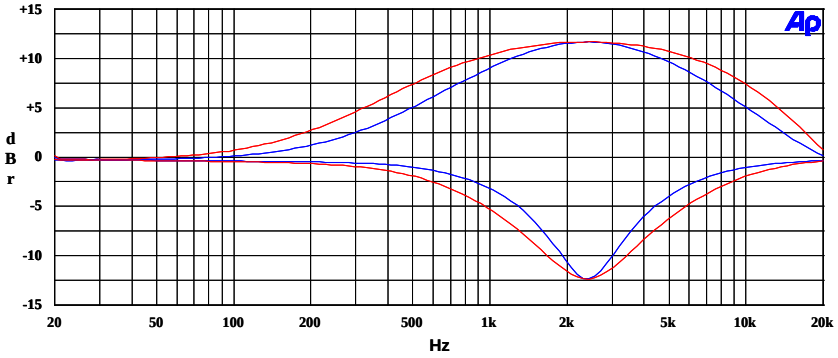


Figure 51: EQ Band 4, EQ4BW = 0 versus EQ4BW =1

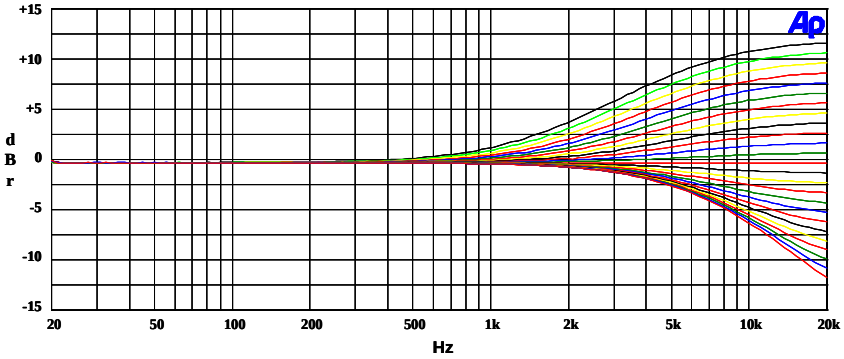


Figure 52: EQ Band 5 Gains for Lowest Cut-Off Frequency

13 Appendix B: Companding Tables

13.1 µ-Law / A-Law Codes for Zero and Full Scale

Level	µ-Law			A-Law		
	Sign bit (D7)	Chord bits (D6,D5,D4)	Step bits (D3,D2,D1,D0)	Sign bit (D7)	Chord bits (D6,D5,D4)	Step bits (D3,D2,D1,D0)
+ Full Scale	1	000	0000	1	010	1010
+ Zero	1	111	1111	1	101	0101
- Zero	0	111	1111	0	101	0101
- Full Scale	0	000	0000	0	010	1010

Table 21: Companding Codes for Zero and Full-Scale

13.2 µ-Law / A-Law Output Codes (Digital mW)

Sample	µ-Law			A-Law		
	Sign bit (D7)	Chord bits (D6,D5,D4)	Step bits (D3,D2,D1,D0)	Sign bit (D7)	Chord bits (D6,D5,D4)	Step bits (D3,D2,D1,D0)
1	0	001	1110	0	011	0100
2	0	000	1011	0	010	0001
3	0	000	1011	0	010	0001
4	0	001	1110	0	011	0100
5	1	001	1110	1	011	0100
6	1	000	1011	1	010	0001
7	1	000	1011	1	010	0001
8	1	001	1110	1	011	0100

Table 22: Companding Output Codes

14 ppendix C: Control and Status Registers

Register		Function	Name	Bit								Description
Dec	Hex			8	7	6	5	4	3	2	1	0	
0	00	SOFTWARE RESET											**Software Reset** (Write any value ***once*** to reset all the registers.)
1	01	POWER MANAGEMENT 1	DCBUFEN										**Internal Tie-off Buffer In 1.5X Boost Mode Condition Enable Control** 0 = Disable (DEFAULT) 1 = Enable
			AUX1MXEN										**AUX1 Mixer Enable Control** 0 = Disable (DEFAULT) 1 = Enable
			AUX2MXEN										**AUX2 Mixer Enable Control** 0 = Disable (DEFAULT) 1 = Enable
			PLLEN										**Internal PLL Enable Control** 0 = Disable (DEFAULT) 1 = Enable
			MICBIASEN										**Microphone Bias Buffer Amplifier Output Enable Control** (Pin#32) 0 = Disable (DEFAULT - MICBIAS pin in High-Z condition) 1 = Enable
			ABIASEN										**Internal Analog Bias Buffer Enable Control** 0 = Disable (DEFAULT) 1 = Enable
			IOBUFEN										**Internal Tie-off Buffer In Non-boost 1.0X Mode Condition Enable Control** 0 = Disable (DEFAULT) 1 = Enable
			REFIMP										**VREF Impedance Select** (Reference used to establish VREF for internal bias buffers) 00 = off (DEFAULT - Input to internal bias buffer in High-Z floating condition) 01 = 80kΩ nominal impedance at VREF pin 10 = 300kΩ nominal impedance at VREF pin 11 = 3kΩ nominal impedance at VREF pin
			DEFAULT	0	0	0	0	0	0	0	0	0	**0x000**
2	02	POWER MANAGEMENT 2	RHPEN										**Right Headphone Driver Enable Control** (RHP analog output - Pin#29) 0 = Disable (DEFAULT - RHP pin in High-Z condition) 1 = Enable
			LHPEN										**Left Headphone Driver Enable Control** (LHP analog output - Pin#30) 0 = Disable (DEFAULT - LHP pin in High-Z condition) 1 = Enable
			SLEEP										**Sleep Enable Control** 0 = Disable (DEFAULT - Normal mode) 1 = Enable (Low-power sleep mode)
			RBSTEN										**Right Channel Input ADC Mix/Boost Stage Enable Control** 0 = Disable (DEFAULT) 1 = Enable
			LBSTEN										**Left Channel Input ADC Mix/Boost Stage Enable Control** 0 = Disable (DEFAULT) 1 = Enable
			RPGAEN										**Right Channel input PGA Enable Control** 0 = Disable (DEFAULT) 1 = Enable
			LPGAEN										**Left Channel input PGA Enable Control** 0 = Disable (DEFAULT) 1 = Enable
			RADCEN										**Right Channel ADC Enable Control** 0 = Disable (DEFAULT) 1 = Enable
			LADCEN										**Left Channel ADC Enable Control** 0 = Disable (DEFAULT) 1 = Enable
			DEFAULT	0	0	0	0	0	0	0	0	0	**0x000**
3	03	POWER MANAGEMENT 3	AUXOUT1EN										**AUXOUT1 Analog Output Enable Control** (Pin#21) 0 = Disable (DEFAULT) 1 = Enable
			AUXOUT2EN										**AUXOUT2 Analog Output Enable Control** (Pin#22)

Register		Function	Name	Bit								Description
Dec	Hex			8	7	6	5	4	3	2	1	0	
													0 = Disable (DEFAULT) 1 = Enable
			LSPKEN										**Left Speaker Output Driver Enable Control** (Pin#25) 0 = Disable (DEFAULT) 1 = Enable
			RSPKEN										**Right Speaker Output Driver Enable Control** (Pin#23) 0 = Disable (DEFAULT) 1 = Enable
			RESERVED										**RESERVED**
			RMIXEN										**Right Channel Output Main Mixer Enable Control** 0 = Disable (DEFAULT) 1 = Enable
			LMIXEN										**Left Channel Output Main Mixer Enable Control** 0 = Disable (DEFAULT) 1 = Enable
			RDACEN										**Right Channel DAC Enable Control** 0 = Disable (DEFAULT) 1 = Enable
			LDACEN										**Left Channel DAC Enable Control** 0 = Disable (DEFAULT) 1 = Enable
			DEFAULT	0	0	0	0	0	0	0	0	0	0x000
			BCLKP										**BCLK Phase Polarity** 0 = Non-inverted (DEFAULT) 1 = Inverted
			LRP										**I2S Audio Data Interface Left/Right Phase Polarity** 0 = Non-inverted (DEFAULT) 1 = Inverted **PCMA & PCMB Left/Right Word Ordering Select** 0 = MSB is valid on 2nd rising edge of BCLK after rising edge of FS 1 = MSB is valid on 1st rising edge of BCLK after rising edge of FS
			WLEN										**Word Length Of Audio Data Stream Select** 00 = 16-bit word length 01 = 20-bit word length 10 = 24-bit word length (DEFAULT) 11 = 32-bit word length
4	04	AUDIO INTERFACE	AIFMT										**Audio Interface Data Format Select** 00 = Right justified 01 = Left justified 10 = Standard I2S format (DEFAULT) 11 = PCMA or PCMB audio data format option
			DACPHS										**DAC Audio Data Left-right Ordering Select** 0 = Left DAC data in left phase of LRP (DEFAULT) 1 = Left DAC data in right phase of LRP (left-right reversed)
			ADCPHS										**ADC Audio Data Left-right Ordering Select** 0 = Left ADC data is output in left phase of LRP (DEFAULT) 1 = Left ADC data is output in right phase of LRP (left-right reversed)
			MONO										**Mono Operation Enable Control** 0 = Mono mode with audio data in left phase of LRP (DEFAULT) 1 = Normal stereo mode of operation
			DEFAULT	0	0	1	0	1	0	0	0	0	0x050
			RESERVED										**RESERVED**
			CMB8										**8-bit Word Enable For Companding Mode Of Operation Enable Control** 0 = Normal operation ((DEFAULT - No companding) 1 = 8-bit operation for companding mode
5	05	COMPANDING	DACCM										**DAC Companding Mode Select** 00 = Off ((DEFAULT - Normal linear operation) 01 = RESERVED 10 = μ-law companding 11 = A-law companding
			ADCCM										**ADC companding Mode Select** 00 = Off ((DEFAULT - Normal linear operation) 01 = RESERVED 10 = μ-law companding 11 = A-law companding

Register		Function	Name	Bit								Description
Dec	Hex			8	7	6	5	4	3	2	1	0	
			ADDAP										**ADC Output Data Stream Directly Routed To DAC Input Data Path Enable Control** 0 = Disable (DEFAULT) 1 = Enable
			DEFAULT	0	0	0	0	0	0	0	0	0	**0x000**
6	06	CLOCK CONTROL 1	CLKM										**Master Clock Source Select** 0 = MCLK (Pin#11 used as master clock) 1 = Internal PLL oscillator output used as master clock (DEFAULT)
			MCLKSEL										**Scaling Divider For Internal MCLK From Master Clock Source** 000 = divide by 1 001 = divide by 1.5 010 = divide by 2 (DEFAULT) 011 = divide by 3 100 = divide by 4 101 = divide by 6 110 = divide by 8 111 = divide by 12
			BCLKSEL										**Scaling Divider For BCLK From MCLK Output** (BCLK Pin#8, When chip is in master mode.) 000 = divide by 1 (DEFAULT) 001 = divide by 2 010 = divide by 4 011 = divide by 8 100 = divide by 16 101 = divide by 32 110 = RESERVED 111 = RESERVED
			RESERVED										**RESERVED**
			CLKIOEN										**FS and BCLK Input / Output Enable Control** 0 = FS and BCLK are inputs (DEFAULT - Slave mode) 1 = FS and BCLK are outputs (Master mode)
			DEFAULT	1	0	1	0	0	0	0	0	0	**0x140**
7	07	CLOCK CONTROL 2	4WSPIEN										**4-wire Control Interface Enable Control** 0 = Disable (DEFAULT) 1 = Enable
			RESERVED										**RESERVED**
			SMPLR										**Audio Data Sample Rate Indication Select** (Sets up scaling for internal filter coefficients, but does not affect in any way the actual device sample rate. Should be set to value most closely matching the actual sample rate determined by 256FS internal node.) 000 = 48KHz (DEFAULT) 001 = 32KHz 010 = 24KHz 011 = 16KHz 100 = 12KHz 101 = 8KHz 110 = RESERVED 111 = RESERVED
			SCLKEN										**Slow Timer Clock Enable Control** **(**Starts internal timer clock derived by dividing master clock.) 0 = Disable (DEFAULT) 1 = Enable
			DEFAULT	0	0	0	0	0	0	0	0	0	**0x000**
8	08	GPIO	RESERVED										**RESERVED**
			GPIO1PLL										**Scaling Divider For GPIO Clock From PLL Clock** 00 = Divide by 1 (DEFAULT) 01 = Divide by 2 10 = Divide by 3 11 = Divide by 4
			GPIO1PL										**GPIO1 Polarity** 0 = Non-inverted (DEFAULT) 1 = Inverted
			GPIO1SEL										**CSB/GPIO1 Function Select** 000 = Input subject to MODE Pin#18 input logic level (DEFAULT) 001 = RESERVED 010 = Temperature OK status output (Logic 0 = thermal shutdown) 011 = DAC automute condition (Logic 1 = one or both DACs automuted)

Register		Function	Name	Bit								Description
Dec	Hex			8	7	6	5	4	3	2	1	0	
													100 = Output divided PLL clock 101 = PLL locked condition (Logic 1 = PLL locked) 110 = Output set to logic 1 condition 111 = Output set to logic 0 condition
			DEFAULT	0	0	0	0	0	0	0	0	0	0x000
9	09	JACK DETECT 1	JCKMIDEN										**Internal Bias Amplifiers By Jack Detection Enable Control** (Automatically enable internal bias amplifiers based on jack detection state sensed through GPIO pin associated to jack detection function.) Bit 7 = 1 (Enable bias amplifiers on jack at logic 0 level) Bit 8 = 1 (Enable bias amplifiers on jack at logic 1 level)
			JCKDEN										**Jack Detection Feature Enable Control** 0 = Disable (DEFAULT) 1 = Enable
			JCKDIO										**Jack Detection Pin Select** 00 = GPIO1 is used for jack detection feature (DEFAULT) 01 = GPIO2 is used for jack detection feature 10 = GPIO3 is used for jack detection feature 11 = RESERVED
			RESERVED										**RESERVED**
			DEFAULT	0	0	0	0	0	0	0	0	0	0x000
10	0A	DAC CONTROL	RESERVED										**RESERVED**
			SOFTMT										**DAC Softmute Enable Control** 0 = Disable (DEFAULT) 1 = Enable
			RESERVED										**RESERVED**
			DACOS										**DAC Oversampling Rate Select** 0 = 64x oversampling (DEFAULT) 1 = 128x oversampling
			AUTOMT										**DAC Automute Function Enable Control** 0 = Disable (DEFAULT) 1 = Enable
			RDACPL										**DAC Right Channel Output Polarity** 0 = Non-inverted (DEFAULT) 1 = Inverted
			LDACPL										**DAC Left Channel Output Polarity** 0 = Non-inverted (DEFAULT) 1 = Inverted
			DEFAULT	0	0	0	0	0	0	0	0	0	0x000
11	0B	LEFT DAC VOLUME	LDACVU										**DAC Left Digital Volume Update Bit** (Write-only bit for synchronized L/R DAC changes) If logic = 0 on R11 write, new R11 value stored in temporary register If logic = 1 on R11 write, new R11 and pending R12 values become active
			LDACGAIN										**DAC Left Digital Volume Control** (Step size is 0.5dB.) 0000 0000 = Digital mute condition 0000 0001 = -127.0dB 0000 0010 = -126.5dB ▼ 1111 1110 = -0.5dB 1111 1111 = 0.0dB (DEFAULT)
			DEFAULT	0	1	1	1	1	1	1	1	1	0x0FF
12	0C	RIGHT DAC VOLUME	RDACVU										**DAC Right Digital Volume Update Bit** (Write-only bit for synchronized L/R DAC changes) If logic = 0 on R12 write, new R12 value stored in temporary register If logic = 1 on R12 write, new R12 and pending R11 values become active
			RDACGAIN										**DAC Right Digital Volume Control** (Step size is 0.5dB.) 0000 0000 = Digital mute condition 0000 0001 = -127.0dB 0000 0010 = -126.5dB ▼ 1111 1110 = -0.5dB 1111 1111 = 0.0dB (DEFAULT)
			DEFAULT	0	1	1	1	1	1	1	1	1	0x0FF

Register		Function	Name	Bit								Description
Dec	Hex			8	7	6	5	4	3	2	1	0	
13	0D	JACK DETECT 2	RESERVED										RESERVED
			JCKDOEN1										**Output Drivers By Jack Detection Enable Control** (Automatically enable outputs drivers based on the designated jack detection input as logic = 1 condition with the jack detection feature enabled.) Bit 4 = 1 (Enable left and right headphone output drivers) Bit 5 = 1 (Enable left and right speaker output drivers) Bit 6 = 1 (Enable AUXOUT2 output driver) Bit 7 = 1 (Enable AUXOUT1 output driver)
			JCKDOEN0										**Output Drivers By Jack Detection Enable Control** (Automatically enable outputs drivers based on the designated jack detection input as logic = 0 condition with the jack detection feature enabled.) Bit 0 = 1 (Enable left and right headphone output drivers) Bit 1 = 1 (Enable left and right speaker output drivers) Bit 2 = 1 (Enable AUXOUT2 output driver) Bit 3 = 1 (Enable AUXOUT1 output driver)
			DEFAULT	0	0	0	0	0	0	0	0	0	0x000
14	0E	ADC CONTROL	HPFEN										**High Pass Filter For ADC Output Data Stream Enable Control** 0 = Disable 1 = Enable (DEFAULT)
			HPFAM										**High Pass Filter Mode Select** 0 = Normal audio mode, 1st order 3.7Hz high pass filter for DC blocking (DEFAULT) 1 = Application specific mode, variable 2nd order high pass filter
			HPF										**Application Specific Mode Cutoff Frequency Select** <See text and table for details>
			ADCOS										**ADC Oversampling Rate Select** 0 = 64x oversampling rate (DEFAULT) 1 = 128x oversampling rate
			RESERVED										RESERVED
			RADCPL										**ADC Right Channel Output Polarity** 0 = Non-inverted (DEFAULT) 1 = Inverted
			LADCPL										**ADC Left Channel Output Polarity** 0 = Non-inverted (DEFAULT) 1 = Inverted
			DEFAULT	1	0	0	0	0	0	0	0	0	0x100
15	0F	LEFT ADC VOLUME	LADCVU										**ADC Left Digital Volume Update Bit** (Write-only bit for synchronized L/R ADC changes) If logic = 0 on R15 write, new R15 value stored in temporary register If logic = 1 on R15 write, new R15 and pending R16 values become active
			LADCGAIN										**ADC Left Digital Volume Control** (Step size is 0.5dB.) 0000 0000 = Digital mute condition 0000 0001 = -127.0dB 0000 0010 = -126.5dB ▼ 1111 1110 = -0.5dB 1111 1111 = 0.0dB (DEFAULT)
			DEFAULT	0	1	1	1	1	1	1	1	1	0x0FF
16	10	RIGHT ADC VOLUME	RADCVU										**ADC Right Digital Volume Update Bit** (Write-only bit for synchronized L/R DAC changes) If logic = 0 on R16 write, new R16 value stored in temporary register If logic = 1 on R16 write, new R16 and pending R15 values become active
			RADCGAIN										**ADC Right Digital Volume Control** (Step size is 0.5dB.) 0000 0000 = Digital mute condition 0000 0001 = -127.0dB 0000 0010 = -126.5dB ▼ 1111 1110 = -0.5dB 1111 1111 = 0.0dB (DEFAULT)
			DEFAULT	0	1	1	1	1	1	1	1	1	0x0FF
17	11	RESERVED	RESERVED										RESERVED
18	12	EQ1 LOW CUTOFF	EQM										**Equalizer & 3D Audio Processing Block Assignment Select** 0 = Block operates on digital stream of ADC 1 = Block operates on digital stream of DAC (DEFAULT)

Register		Function	Name	Bit								Description
Dec	Hex			8	7	6	5	4	3	2	1	0	
			RESERVED										RESERVED
			EQ1CF										Equalizer Band 1 Low Pass -3dB Cut-off Frequency Select 00 = 80Hz 01 = 105Hz (DEFAULT) 10 = 135Hz 11 = 175Hz
			EQ1GC										EQ Band 1 Digital Gain Control (Step size is 1dB.) 00000 = +12dB 00001 = +11dB ▼ 01100 = 0dB (DEFAULT) ▼ 11000 = -12dB 11001 = RESERVED ▼ 11110 = RESERVED 11111 = RESERVED
			DEFAULT	1	0	0	1	0	1	1	0	0	0x12C
			EQ2BW										Equalizer Band 2 Bandwidth Select 0 = Narrow band characteristic (DEFAULT) 1 = Wide band characteristic
			RESERVED										RESERVED
			EQ2CF										Equalizer Band 2 Center Frequency Select 00 = 230Hz 01 = 300Hz (DEFAULT) 10 = 385Hz 11 = 500Hz
19	13	EQ2 - PEAK 1	EQ2GC										EQ Band 2 Digital Gain Control (Step size is 1dB.) 00000 = +12dB 00001 = +11dB ▼ 01100 = 0dB (DEFAULT) ▼ 11000 = -12dB 11001 = RESERVED ▼ 11110 = RESERVED 11111 = RESERVED
			DEFAULT	0	0	0	1	0	1	1	0	0	0x02C
			EQ3BW										Equalizer Band 3 Bandwidth Select 0 = Narrow band characteristic (DEFAULT) 1 = Wide band characteristic
			RESERVED										RESERVED
			EQ3CF										Equalizer Band 3 Center Frequency Select 00 = 650Hz 01 = 850Hz (DEFAULT) 10 = 1.1KHz 11 = 1.4KHz
20	14	EQ3 - PEAK 2	EQ3GC										EQ Band 3 Digital Gain Control (Step size is 1dB.) 00000 = +12dB 00001 = +11dB ▼ 01100 = 0dB (DEFAULT) ▼ 11000 = -12dB 11001 = RESERVED ▼ 11110 = RESERVED 11111 = RESERVED
			DEFAULT	0	0	0	1	0	1	1	0	0	0x02C
21	15	EQ4 - PEAK 3	EQ4BW										Equalizer Band 4 Bandwidth Select 0 = Narrow band characteristic (DEFAULT) 1 = Wide band characteristic
			RESERVED										RESERVED

Register		Function	Name	Bit								Description
Dec	Hex			8	7	6	5	4	3	2	1	0	
			EQ4CF										**Equalizer Band 4 Center Frequency Select** 00 = 1.8KHz 01 = 2.4KHz (DEFAULT) 10 = 3.2KHz 11 = 4.1KHz
			EQ4GC										**EQ Band 4 Digital Gain Control** (Step size is 1dB.) 00000 = +12dB 00001 = +11dB ▼ 01100 = 0dB (DEFAULT) ▼ 11000 = -12dB 11001 = RESERVED ▼ 11110 = RESERVED 11111 = RESERVED
			DEFAULT	0	0	0	1	0	1	1	0	0	0x02C
22	16	EQ5 - HIGH CUTOFF	RESERVED										RESERVED
			EQ5CF										**Equalizer Band 5 High Pass -3dB Cut-off Frequency Select** 00 = 5.3KHz 01 = 6.9KHz (DEFAULT) 10 = 9.0KHz 11 = 11.7KHz
			EQ5GC										**EQ Band 5 Digital Gain Control** (Step size is 1dB.) 00000 = +12dB 00001 = +11dB ▼ 01100 = 0dB (DEFAULT) ▼ 11000 = -12dB 11001 = RESERVED ▼ 11110 = RESERVED 11111 = RESERVED
			DEFAULT	0	0	0	1	0	1	1	0	0	0x02C
23	17	RESERVED	RESERVED										RESERVED
24	18	DAC LIMITER 1	DACLIMEN										**DAC Digital Limiter Enable Control** 0 = Disable (DEFAULT) 1 = Enable
			DACLIMDCY										**DAC Limiter Decay Time** (Proportional to actual DAC sample rate. Values given here are for 44.1kHz sample rate.) (Step size is ***double***.) 0000 = 0.544ms 0001 = 1.09ms 0010 = 2.18ms 0011 = 4.36ms (DEFAULT) 0100 = 8.72ms 0101 = 17.4ms 0110 = 34.8ms 0111 = 69.6ms 1000 = 139ms 1001 = 278ms 1010 = 566ms 1011 = 1130ms 1100 = 1130ms ▼ 1111 = 1130ms
			DACLIMATK										**DAC Limiter Attack Time** (Proportional to actual DAC sample rate. Values given here are for 44.1kHz sample rate.) (Step size is ***double***.) 0000 = 68.0us (microseconds) 0001 = 136us 0010 = 272us (DEFAULT) 0011 = 544us 0100 = 1.09ms (milliseconds) 0101 = 2.18ms 0110 = 4.36ms

Register		Function	Name	Bit								Description
Dec	Hex			8	7	6	5	4	3	2	1	0	
													0111 = 8.72ms 1000 = 17.4ms 1001 = 34.8ms 1010 = 69.6ms 1011 = 139ms 1100 = 139ms ▼ 1111 = 139ms
			DEFAULT	0	0	0	1	1	0	0	1	0	0x032
25	19	DAC LIMITER 2	RESERVED										RESERVED
			DACLIMTHL										**DAC Limiter Threshold Related To Full Scale Output Level** (0dB = full scale) 000 = -1dB (DEFAULT) 001 = -2dB 010 = -3dB 011 = -4dB 100 = -5dB 101 = -6dB 110 = -6dB 111 = -6dB
			DACLIMBST										**DAC Limiter Maximum Automatic Gain Boost In Limiter Mode** (If R24 limiter mode is disabled, specified gain value will be applied in addition to other gain values in the signal path.) (Step size is 1dB.) 0000 = 0dB (DEFAULT) 0001 = +1dB ▼ 1100 = +12dB 1101 = RESERVED 1110 = RESERVED 1111 = RESERVED
			DEFAULT	0	0	0	0	0	0	0	0	0	0x000
26	1A	RESERVED	RESERVED										RESERVED
27	1B	NOTCH FILTER 1	NFCU1										**Write-only Update Bit For Simultaneous Change Of All Notch Filter Parameters** (Logic 0 on R27 register write causes new value to be pending an update bit event on R27, R28, R29 or R30. Logic 1 on R27 register write operation causes new R27 value and any pending value in R28, R29, or R30 to go into effect.)
			NFCEN										**Notch Filter Enable Control** 0 = Disable (DEFAULT) 1 = Enable
			NFCA0										**Notch Filter A0 Coefficient MSB [13:7]** <See text and table for details>
			DEFAULT	0	0	0	0	0	0	0	0	0	0x000
28	1C	NOTCH FILTER 2	NFCU2										**Write-only Update Bit For Simultaneous Change Of All Notch Filter Parameters** (Logic 0 on R28 register write causes new value to be pending an update bit event on R27, R28, R29 or R30. Logic 1 on R28 register write operation causes new R28 value and any pending value in R27, R29, or R30 to go into effect.)
			RESERVED										RESERVED
			NFCA0										**Notch Filter A0 Coefficient LSB [6:0]** **<See text and table for details>**
			DEFAULT	0	0	0	0	0	0	0	0	0	0x000
29	1D	NOTCH FILTER 3	NFCU3										**Write-only Update Bit For Simultaneous Change Of All Notch Filter Parameters** (Logic 0 on R29 register write causes new value to be pending an update bit event on R27, R28, R29 or R30. Logic 1 on R29 register write operation causes new R29 value and any pending value in R27, R28, or R30 to go into effect.)
													RESERVED
			NFCA1										**Notch Filter A1 Coefficient MSB [13:7]** <See text and table for details>
			DEFAULT	0	0	0	0	0	0	0	0	0	0x000

Register		Function	Name	Bit								Description
Dec	Hex			8	7	6	5	4	3	2	1	0	
30	1E	NOTCH FILTER 4	NFCU4										**Write-only Update Bit For Simultaneous Change Of All Notch Filter Parameters** (Logic 0 on R30 register write causes new value to be pending an update bit event on R27, R28, R29 or R30. Logic 1 on R30 register write operation causes new R30 value and any pending value in R27, R28, or R29 to go into effect.)
			RESERVED										**RESERVED**
			NFCA1										**Notch Filter A1 Coefficient LSB [6:0]** **<See text and table for details>**
			DEFAULT	0	0	0	0	0	0	0	0	0	**0x000**
31	1F	RESERVED	RESERVED										**RESERVED**
32	20	ALC CONTROL 1	ALCEN										**Automatic Level Control Function Enable Control** 00 = Disable left & right channel ALCs (DEFAULT) 01 = Enable right channel ALC only 10 = Enable left channel ALC only 11 = Enable left & right channel ALCs
			RESERVED										**RESERVED**
			ALCMXGAIN										**Set Maximum Gain Limit For PGA Volume Changes Under ALC Control** (Step size is 6dB.) 111 = +35.25dB (DEFAULT) 110 = +29.25dB 101 = +23.25dB 100 = +17.25dB 011 = +11.25dB 010 = +5.25dB 001 = -0.75dB 000 = -6.75dB
			ALCMNGAIN										**Set Minimum Gain Limit For PGA Volume Changes Under ALC Control** (Step size is 6dB.) 000 = -12dB (DEFAULT) 001 = -6dB 010 = 0dB 011 = +6dB 100 = +12dB 101 = +18dB 110 = +24dB 111 = +30dB
			DEFAULT	0	0	0	1	1	1	0	0	0	**0x038**
33	21	ALC CONTROL 2	RESERVED										**RESERVED**
			ALCHT										**Hold time Before ALC Automated Gain Increase** (Step size is ***double***.) 0000 = 0ms (DEFAULT) 0001 = 2ms 0010 = 4ms ▼ 1001 = 512ms 1010 = 1000ms 1011 = 1000ms ▼ 1111 = 1000ms
			ALCSL										**ALC Target Level At ADC Output** (Step size is 1.5dB.) 1111 = -1.5dB FS (Full scale) 1110 = -1.5dB FS 1101 = -3.0dB FS 1100 = -4.5dB FS 1011 = -6.0dB FS (DEFAULT) 0001 = -21.0dB FS 0000 = -22.5dB FS (Lowest possible target signal level)
			DEFAULT	0	0	0	0	0	1	0	1	1	**0x00B**
34	22	ALC CONTROL 3	ALCM										**ALC Mode Control** 0 = Normal ALC operation (DEFAULT) 1 = Limiter Mode operation

Register		Function	Name	Bit								Description
Dec	Hex			8	7	6	5	4	3	2	1	0	
			ALCDCY										**ALC Decay Time** (Total response time can be estimated by the total number of steps necessary to compensate for a given magnitude change in the signal. Duration per step of gain change is for 0.75dB of PGA gain. For example, a 6dB decrease in the signal would require eight ALC steps to compensate.) (Step size is ***double***.) Normal Mode / Limiter Mode 0000 = 500us / 0000 = 125us 0001 = 1ms / 0001 = 250us 0010 = 2ms / 0010 = 500us 0011 = 4ms / 0011 = 1ms (DEFAULT) 1000 = 128ms / 1000 = 32ms 1001 = 256ms / 1001 = 64ms 1010 = 512ms / 1010 = 128ms ▼ / ▼ 1111 = 512ms / 1111 = 128ms
			ALCATK										**ALC Attack Time** (Total response time can be estimated by the total number of steps necessary to compensate for a given magnitude change in the signal. Duration per step of gain change is for 0.75dB of PGA gain. For example, a 6dB decrease in the signal would require eight ALC steps to compensate.) (Step size is ***double***.) Normal Mode / Limiter Mode 0000 = 125us / 0000 = 31us 0001 = 250us / 0001 = 62us 0010 = 500us / 0010 = 125us (DEFAULT) 1000 = 32ms / 1000 = 8ms 1001 = 64ms / 1001 = 16ms 1010 = 128ms / 1010 = 32ms ▼ / ▼ 1111 = 128ms / 1111 = 32ms
			DEFAULT	0	0	0	1	1	0	0	1	0	0x032
35	23	NOISE GATE	RESERVED										RESERVED
			ALCNEN										**ALC Noise Gate Function Enable Control** 0 = Disable (DEFAULT) 1 = Enable
			ALCNTH										**ALC Noise Gate Threshold Level** (Step size is 6dB.) 000 = -39dB (DEFAULT) 001 = -45dB 010 = -51dB 011 = -57dB 100 = -63dB 101 = -69dB 110 = -75dB 111 = -81dB
			DEFAULT	0	0	0	0	0	0	0	0	0	0x000
36	24	PLL N	RESERVED										RESERVED
			PLLMCLK										**Pre-scale Divider For PLL Clock Input From MCLK** 0 = MCLK divide by 1 (DEFAULT) 1 = MCLK divide by 2
			PLLN										**Integer Portion Of PLL Input/Output Frequency Ratio Divider** (Decimal value should be constrained to 6, 7, 8, 9, 10, 11, or 12. Default decimal value is 8.) (See text for details.)
			DEFAULT	0	0	0	0	0	1	0	0	0	0x008
37	25	PLL K 1	RESERVED										RESERVED
			PLLK[23:18]										**High Order Bits Of Fractional Portion Of PLL Input/Output Frequency Ratio Divider** (See text for details.)
			DEFAULT	0	0	0	0	0	1	1	0	0	0x00C

Register		Function	Name	Bit								Description
Dec	Hex			8	7	6	5	4	3	2	1	0	
38	26	PLL K 2	PLLK[17:9]										**Middle Order Bits Of Fractional Portion Of PLL Input/Output Frequency Ratio Divider** (See text for details.)
			DEFAULT	0	1	0	0	1	0	0	1	1	**0x093**
39	27	PLL K 3	PLLK{8:0]										**Low Order Bits Of Fractional Portion Of PLL Input/Output Frequency Ratio Divider** (See text for details.)
			DEFAULT	0	1	1	1	0	1	0	0	1	**0x0E9**
40	28	RESERVED	RESERVED										**RESERVED**
41	29	3D CONTROL	RESERVED										**RESERVED**
			3DDEPTH										**3D Stereo Enhancement Effect Depth Select** (Step size is 6.67%.) 0000 = 0.0% effect – Disable (DEFAULT) 0001 = 6.67% effect 0010 = 13.3% effect 1110 = 93.3% effect 1111 = 100% effect (MAX)
			DEFAULT	0	0	0	0	0	0	0	0	0	**0x000**
42	2A	RESERVED	RESERVED										**RESERVED**
43	2B	RIGHT SPEAKER SUBMIXER	RESERVED										**RESERVED**
			RMIXMUT										**RMIX Speaker Signal Gain Stage Output In Right Speaker Submixer Mute Enable Control** 0 = Disable (DEFAULT) 1 = Enable
			RSUBBYP										**Right Speaker Submixer Bypass Control** 0 = Right speaker amplifier directly connected to RMIX speaker signal gain stage (DEFAULT) 1 = Right speaker amplifier connected to submixer output (inverts RMIX for BTL)
			RAUXRSUBG										**RAUXIN Input To Right Speaker Submixer Input Gain Control** (Step size is 3dB.) 000 = -15dB (DEFAULT) 001 = -12dB 010 = -9dB 011 = -6dB 100 = -3dB 101 = 0dB 110 = +3dB 111 = +6dB
			RAUXSMUT										**RAUXIN Input To Right Speaker Submixer Input Mute Enable Control** 0 = Disable (DEFAULT) 1 = Enable
			DEFAULT	0	0	0	0	0	0	0	0	0	**0x000**
44	2C	INPUT CONTROL	MICBIASV										**Microphone Bias Voltage Select** (Values change slightly with R40 MISBIAS mode selection control. Open circuit voltage on MICBIAS Pin#32 is shown as follows as a fraction of the VDDA Pin#31 supply voltage.) Normal Mode / Low Noise Mode 00 = 0.9x (DEFAULT) / 00 = 0.85x 01 = 0.65x / 01 = 0.60x 10 = 0.75x / 10 = 0.70x 11 = 0.50x / 11 = 0.50x
			RLINRPGA										**Right Line Input To Right PGA Positive Input Path Enable Control** 0 = Disable (DEFAULT) 1 = Enable
			RMICNRPGA										**Right Microphone Negative Input To Right PGA Negative Input Path Enable Control** 0 = Disable 1 = Enable (DEFAULT)

Register		Function	Name	Bit								Description
Dec	Hex			8	7	6	5	4	3	2	1	0	
			RMICPRPGA										**Right Microphone Positive Input To Right PGA Positive Input Path Enable Control** 0 = Disable 1 = Enable (DEFAULT)
			RESERVED										**RESERVED**
			LLINLPGA										**Left Line Input To Left PGA Positive Input Path Enable Control** 0 = Disable (DEFAULT) 1 = Enable
			LMICNLPGA										**Left Microphone Negative Input To Left PGA Negative Input Path Enable Control** 0 = Disable 1 = Enable (DEFAULT)
			LMICPLPGA										**Left Microphone Positive Input To Left PGA Positive Input Path Enable Control** 0 = Disable 1 = Enable (DEFAULT)
			DEFAULT	0	0	0	1	1	0	0	1	1	**0x033**
			LPGAU										**PGA Volume Update Bit** (Write-only bit for synchronized L/R PGA changes) If logic = 0 on R45 write, new R45 value stored in temporary register If logic = 1 on R45 write, new R45 and pending R46 values become active
			LPGAZC										**Left Channel Input Zero-crossing Detection Enable Control** 0 = Gain changes to PGA register happen immediately (DEFAULT) 1 = Gain changes to PGA happen pending zero-crossing logic
			LPGAMT										**Left Channel PGA Mute Enable Control** 0 = PGA not muted, normal operation (DEFAULT) 1 = PGA in muted condition not connected to LADC Mix/Boost stage
45	2D	LEFT INPUT PGA GAIN	LPGAGAIN										**Left Channel Input PGA Volume Control** (Setting becomes active when zero-crossing and/or update bit features enabled.) (Step size is 0.75dB.) 00 0000 = -12dB 00 0001 = -11.25dB ▼ 00 1111 = -0.75dB 01 0000 = 0dB (DEFAULT) 01 0001 = 0.75dB ▼ 11 1110 = +34.50dB 11 1111 = +35.25dB
			DEFAULT	0	0	0	0	1	0	0	0	0	**0x010**
			RPGAU										**PGA Volume Update Bit** (Write-only bit for synchronized L/R PGA changes) If logic = 0 on R46 write, new R46 value stored in temporary register If logic = 1 on R46 write, new R46 and pending R45 values become active
			RPGAZC										**Right Channel Input Zero-crossing Detection Enable Control** 0 = Gain changes to PGA register happen immediately (DEFAULT) 1 = Gain changes to PGA happen pending zero-crossing logic
			RPGAMT										**Right Channel PGA Mute Enable Control** 0 = PGA not muted, normal operation (DEFAULT) 1 = PGA in muted condition not connected to RADC Mix/Boost stage
46	2E	RIGHT INPUT PGA GAIN	RPGAGAIN										**Right Channel Input PGA Volume Control** (Setting becomes active when zero-crossing and/or update bit features enabled.) (Step size is 0.75dB.) 00 0000 = -12dB 00 0001 = -11.25dB ▼ 00 1111 = -0.75dB 01 0000 = 0dB (DEFAULT) 01 0001 = 0.75dB ▼ 11 1110 = +34.50dB 11 1111 = +35.25dB
			DEFAULT	0	0	0	0	1	0	0	0	0	**0x010**

Register		Function	Name	Bit								Description
Dec	Hex			8	7	6	5	4	3	2	1	0	
47	2F	LEFT ADC BOOST	LPGABST										**LPGA Output To LADC Mix/Boost Stage Input +20dB Boost Enable Control** 0 = Disable 1 = Enable (DEFAULT)
			RESERVED										**RESERVED**
			LPGABSTGAIN										**Left Line Input To LADC Mix/Boost Stage Input Gain Control** (Step size is 3dB.) 000 = Path disconnected (DEFAULT) 001 = -12dB 010 = -9dB 011 = -6dB 100 = -3dB 101 = 0dB 110 = +3dB 111 = +6dB
			RESERVED										**RESERVED**
			LAUXBSTGAIN										**LAUXIN Input To LADC Mix/Boost Stage Input Gain Control** (Step size is 3dB.) 000 = Path disconnected (DEFAULT) 001 = -12dB 010 = -9dB 011 = -6dB 100 = -3dB 101 = 0dB 110 = +3dB 111 = +6dB
			DEFAULT	1	0	0	0	0	0	0	0	0	**0x100**
48	30	RIGHT ADC BOOST	RPGABST										**RPGA Output To RADC Mix/Boost Stage Input +20dB Boost Enable Control** 0 = Disable 1 = Enable (DEFAULT)
			RESERVED										**RESERVED**
			RPGABSTGAIN										**Right Line Input To RADC Mix/Boost Stage Input Gain Control** (Step size is 3dB.) 000 = Path disconnected (DEFAULT) 001 = -12dB 010 = -9dB 011 = -6dB 100 = -3dB 101 = 0dB 110 = +3dB 111 = +6dB
			RESERVED										**RESERVED**
			RAUXBSTGAIN										**RAUXIN Input To RADC Mix/Boost Stage Input Gain Control** (Step size is 3dB.) 000 = Path disconnected (DEFAULT) 001 = -12dB 010 = -9dB 011 = -6dB 100 = -3dB 101 = 0dB 110 = +3dB 111 = +6dB
			DEFAULT	1	0	0	0	0	0	0	0	0	**0x100**
49	31	OUTPUT CONTROL	RESERVED										**RESERVED**
			LDACRMX										**Left DAC Output To RMAIN MIXER Input Cross-coupling Path Enable Control** 0 = Disable (DEFAULT) 1 = Enable
			RDACLMX										**Right DAC Output To LMAIN MIXER Input Cross-coupling Path Enable Control** 0 = Disable (DEFAULT) 1 = Enable
			AUX1BST										**AUXOUT1 Gain +1.5X Boost Enable Control** 0 = Disable (DEFAULT - Preferred setting for 3.6V and lower operation) 1 = Enable (Required setting for greater than 3.6V operation)

Register		Function	Name	Bit								Description
Dec	Hex			8	7	6	5	4	3	2	1	0	
			AUX2BST										**AUXOUT1 Gain +1.5X Boost Enable Control** 0 = Disable (DEFAULT - Preferred setting for 3.6V and lower operation) 1 = Enable (Required setting for greater than 3.6V operation)
			SPKBST										**LSPKOUT & RSPKOUT Amplifier Gain +1.5X Boost Enable Control** 0 = Disable (DEFAULT - Preferred setting for 3.6V and lower operation) 1 = Enable (Required setting for greater than 3.6V operation)
			TSEN										**Thermal Shutdown Enable Control** (To protects chip from thermal destruction on overload.) 0 = Disable 1 = Enable (DEFAULT)
			AOUTIMP										**Output Tie-off Impedance Select** (Unused and disabled outputs tie to internal voltage reference to reduce pops and clicks.) 0 = Tie-off impedance value of 1KΩ (DEFAULT) 1 = Tie-off impedance value of 30KΩ
			DEFAULT	0	0	0	0	0	0	0	1	0	0x002
50	32	LEFT MIXER	LAUXMXGAIN										**LAUXIN Input To LMAIN MIXER Input Gain Control** (Step size is 3dB.) 000 = -15dB (DEFAULT) 001 = -12dB 010 = -9dB 011 = -6dB 100 = -3dB 101 = 0dB 110 = +3dB 111 = +6dB
			LAUXLMX										**LAUXIN Input To LMAIN MIXER Input Path Enable Control** 0 = Disable (DEFAULT) 1 = Enable
			LBYPMXGAIN										**LADC Mix/Boost Stage Output To LMAIN MIXER Input Bypass Gain Control** (Step size is 3dB.) 000 = -15dB (DEFAULT) 001 = -12dB 010 = -9dB 011 = -6dB 100 = -3dB 101 = 0dB 110 = +3dB 111 = +6dB
			LBYPLMX										**LADC Mix/Boost Stage Output To LMAIN MIXER Input Bypass Path Enable Control** 0 = Disable (DEFAULT) 1 = Enable
			LDACLMX										**LDAC Output To LMAIN MIXER Path Enable Control** 0 = Disable 1 = Enable (DEFAULT)
			DEFAULT	0	0	0	0	0	0	0	0	1	0x001
51	33	RIGHT MIXER	RAUXMXGAIN										**RAUXIN Input To RMAIN MIXER Input Gain Control** (Step size is 3dB.) 000 = -15dB (DEFAULT) 001 = -12dB 010 = -9dB 011 = -6dB 100 = -3dB 101 = 0dB 110 = +3dB 111 = +6dB
			RAUXRMX										**RAUXIN Input To RMAIN MIXER Input Path Enable Control** 0 = Disable (DEFAULT) 1 = Enable

Register		Function	Name	Bit								Description
Dec	Hex			8	7	6	5	4	3	2	1	0	
			RBYPMXGAIN										**RADC Mix/Boost Stage Output To RMAIN MIXER Input Gain Control** (Step size is 3dB.) 000 = -15dB (DEFAULT) 001 = -12dB 010 = -9dB 011 = -6dB 100 = -3dB 101 = 0dB 110 = +3dB 111 = +6dB
			RBYPRMX										**RADC Mix/Boost Stage Output To RMAIN MIXER Input Bypass Path Enable Control** 0 = Disable (DEFAULT) 1 = Enable
			RDACRMX										**RDAC Output To RMAIN MIXER Path Enable Control** 0 = Disable 1 = Enable (DEFAULT)
			DEFAULT	0	0	0	0	0	0	0	0	1	**0x001**
52	34	LHP VOLUME	LHPVU										**Left Headphone Output Volume Update Bit** (Write-only bit for synchronized changes of left and right headphone output settings.) If logic = 0 on R52 write, new R52 value stored in temporary register If logic = 1 on R52 write, new R52 and pending R53 values become active
			LHPZC										**Left headphone Output Zero-crossing Detection Enable Control** 0 = Gain changes to left headphone happen immediately (DEFAULT) 1 = Gain changes to left headphone pending zero-crossing logic
			LHPMUTE										**Left headphone Output Mute Enable Control** 0 = Disable (DEFAULT) 1 = Enable
			LHPGAIN										**Left Headphone Output Volume Control** (Setting becomes active when zero-crossing and/or update bit features enabled.) (Step size is 1dB.) 00 0000 = -57dB 00 0001 = -56dB ▼ 11 1000 = -1dB 11 1001 = 0dB (DEFAULT) 11 1010 = 1dB ▼ 11 1110 = +5dB 11 1111 = +6dB
			DEFAULT	0	0	0	1	1	1	0	0	1	**0x039**
53	35	RHP VOLUME	RHPVU										**Right Headphone Output Volume Update Bit** (Write-only bit for synchronized changes of left and right headphone output settings.) If logic = 0 on R53 write, new R53 value stored in temporary register If logic = 1 on R53 write, new R53 and pending R52 values become active
			RHPZC										**Right headphone Output Zero-crossing Detection Enable Control** 0 = Gain changes to right headphone happen immediately (DEFAULT) 1 = Gain changes to right headphone pending zero-crossing logic
			RHPMUTE										**Right headphone Output Mute Enable Control** 0 = Disable (DEFAULT) 1 = Enable
			RHPGAIN										**Right Headphone Output Volume Control** (Setting becomes active when zero-crossing and/or update bit features enabled.) (Step size is 1dB.) 00 0000 = -57dB 00 0001 = -56dB ▼ 11 1000 = -1dB 11 1001 = 0dB (DEFAULT) 11 1010 = 1dB ▼ 11 1110 = +5dB 11 1111 = +6dB
			DEFAULT	0	0	0	1	1	1	0	0	1	**0x039**

Register		Function	Name	Bit								Description
Dec	Hex			8	7	6	5	4	3	2	1	0	
54	36	LSPKOUT VOLUME	LSPKVU										**Left Speaker Output Volume Update Bit** (Write-only bit for synchronized changes of left and right speaker output settings.) If logic = 0 on R54 write, new R54 value stored in temporary register If logic = 1 on R54 write, new R54 and pending R55 values become active
			LSPKZC										**Left Speaker Output Zero-crossing Detection Enable Control** 0 = Gain changes to left speaker happen immediately (DEFAULT) 1 = Gain changes to left speaker pending zero-crossing logic
			LSPKMUTE										**Left Speaker Output Mute Enable Control** 0 = Disable (DEFAULT) 1 = Enable
			LSPKGAIN										**Left Speaker Output Volume Control** (Setting becomes active when zero-crossing and/or update bit features enabled.) (Step size is 1dB.) 00 0000 = -57dB 00 0001 = -56dB ▼ 11 1000 = -1dB 11 1001 = 0dB (DEFAULT) 11 1010 = 1dB ▼ 11 1110 = +5dB 11 1111 = +6dB
			DEFAULT	0	0	0	1	1	1	0	0	1	0x039
55	37	RSPKOUT VOLUME	RSPKVU										**Right Speaker Output Volume Update Bit** (Write-only bit for synchronized changes of left and right speaker output settings.) If logic = 0 on R55 write, new R55 value stored in temporary register If logic = 1 on R55 write, new R55 and pending R54 values become active
			RSPKZC										**Right Speaker Output Zero-crossing Detection Enable Control** 0 = Gain changes to right speaker happen immediately (DEFAULT) 1 = Gain changes to right speaker pending zero-crossing logic
			RSPKMUTE										**Right Speaker Output Mute Enable Control** 0 = Disable (DEFAULT) 1 = Enable
			RSPKGAIN										**Right Speaker Output Volume Control** (Setting becomes active when zero-crossing and/or update bit features enabled.) (Step size is 1dB.) 00 0000 = -57dB 00 0001 = -56dB ▼ 11 1000 = -1dB 11 1001 = 0dB (DEFAULT) 11 1010 = 1dB ▼ 11 1110 = +5dB 11 1111 = +6dB
			DEFAULT	0	0	0	1	1	1	0	0	1	0x039
56	38	AUX2 MIXER	RESERVED										**RESERVED**
			AUXOUT2MT										**AUXOUT2 Output Mute Enable Control** 0 = Disable (DEFAULT) 1 = Enable
			RESERVED										**RESERVED**
			AUX1MIX2										**AUX1 Mixer Output To AUX2 MIXER Input Path Enable Control** 0 = Disable (DEFAULT) 1 = Enable
			LADCAUX2										**LADC Mix/Boost Stage Output To AUX2 MIXER Input Path Enable Control** 0 = Disable (DEFAULT) 1 = Enable
			LMIXAUX2										**LMAIN MIXER Output To AUX2 MIXER Input Path Enable Control** 0 = Disable (DEFAULT) 1 = Enable
			LDACAUX2										**LDAC Output To AUX2 MIXER Input Path Enable Control** 0 = Disable 1 = Enable (DEFAULT)
			DEFAULT	0	0	0	0	0	0	0	0	1	0x001

Register		Function	Name	Bit								Description
Dec	Hex			8	7	6	5	4	3	2	1	0	
57	39	AUX1 MIXER	RESERVED										RESERVED
			AUXOUT1MT										AUXOUT1 Output Mute Enable Control 0 = Disable (DEFAULT) 1 = Enable
			AUX1HALF										AUXOUT1 -6dB Attenuation Enable Control 0 = Disable (DEFAULT) 1 = Enable
			LMIXAUX1										LMAIN MIXER Output To AUX1 MIXER Input Path Enable Control 0 = Disable (DEFAULT) 1 = Enable
			LDACAUX1										LDAC Output To AUX1 MIXER Input Path Enable Control 0 = Disable (DEFAULT) 1 = Enable
			RADCAUX1										RADC Mix/Boost Stage Output To AUX1 MIXER Input Path Enable Control 0 = Disable (DEFAULT) 1 = Enable
			RMIXAUX1										RMAIN MIXER Output To AUX1 MIXER Input Path Enable Control 0 = Disable (DEFAULT) 1 = Enable
			RDACAUX1										RDAC Output To AUX1 MIXER Input Path Enable Control 0 = Disable 1 = Enable (DEFAULT)
			DEFAULT	0	0	0	0	0	0	0	0	1	0x001
58	3A	POWER MANAGEMENT 4	LPDAC										Low Power DAC Operating Mode Enable Control (Reduce supply current by 50%.) 0 = Disable (DEFAULT) 1 = Enable
			LPIPBST										Low Power ADC Mix/Boost Stage Amplifier Operating Mode Enable Control (Reduce supply current by 50%.) 0 = Disable (DEFAULT) 1 = Enable
			LPADC										Low Power ADC Operating Mode Enable Control (Reduce supply current by 50%.) 0 = Disable (DEFAULT) 1 = Enable
			LPSPKD										Low Power Speaker Amplifier Operating Mode Enable Control (Reduce supply current by 50%.) 0 = Disable (DEFAULT) 1 = Enable
			MICBIASM										Low Noise Microphone Bias Operating Mode Enable Control 0 = Disable (DEFAULT - Low-Z MICBIAS output impedance) 1 = Enable (200Ohms MICBIAS output impedance)
			REGVOLT										Regulator Voltage Control Power Reduction Select 00 = 1.80VDC operation (DEFAULT) 01 = 1.61VDC operation 10 = 1.40VDC operation 11 = 1.218VDC operation
			IBADJ										Master Bias Current Power Reduction Select 00 = Normal operation (DEFAULT) 01 = 25% reduced bias current 10 = 14% reduced bias current 11 = 25% reduced bias current
			DEFAULT	0	0	0	0	0	0	0	0	0	0x000
59	3B	LEFT TIME SLOT	LTSLOT[8:0]										Left channel PCM Time Slot Start Count (LSB portion of total number of bit times to wait from frame sync before clocking audio channel data. LSB portion is combined with MSB from R60 to get total number of bit times to wait.)
			DEFAULT	0	0	0	0	0	0	0	0	0	0x000
60	3C	MISC	PCMTSEN										PCM Mode Time Slot Function Enable Control 0 = Disable (DEFAULT) 1 = Enable
			TRI										Tri-state ADCOUT After Second Half Of LSB Enable Control 0 = Disable (DEFAULT) 1 = Enable
			PCM8BIT										PCM 8-bit Word Length Enable Control 0 = Disable (DEFAULT)

Register		Function	Name	Bit								Description
Dec	Hex			8	7	6	5	4	3	2	1	0	
													1 = Enable
			PUDEN										**ADCOUT Output Driver Enable Control** 0 = Disable (High-Z state) 1 = Enable (DEFAULT)
			PUDPE										**ADCOUT Passive Resistor Pull-up Or Pull-down Enable Control** 0 = Disable (DEFAULT) 1 = Enable
			PUDPS										**ADCOUT Passive Resistor Pull-up Or Pull-down Select** (If PUDPE = 1) 0 = Passive pull-down (DEFAULT) 1 = Passive pull-up
			RESERVED										**RESERVED**
			RTSLOT[9]										**Right Channel PCM Time Slot Start Count** (MSB portion of total number of bit times to wait from frame sync before clocking audio channel data. MSB is combined with LSB portion from R61 to get total number of bit times to wait.)
			LTSLOT[9]										**Left Channel PCM Time Slot Start Count** (MSB portion of total number of bit times to wait from frame sync before clocking audio channel data. MSB is combined with LSB portion from R59 to get total number of bit times to wait.)
			DEFAULT	0	0	0	1	0	0	0	0	0	**0x020**
61	3D	RIGHT TIME SLOT	RTSLOT[8:0]										**Right Channel PCM Time Slot Start Count** (LSB portion of total number of bit times to wait from frame sync before clocking audio channel data. LSB portion is combined with MSB from R60 to get total number of bit times to wait.)
			DEFAULT	0	0	0	1	0	0	0	0	0	**0x020**
62	3E	DEVICE REVISION NUMBER	RESERVED										**RESERVED**
			REV										**Device Revision Number** (For readback over control interface = read-only value)
			DEFAULT	0	0	x	x	x	x	x	x	x	**0x07F (RevA SILICON)**
63	3F	DEVICE ID#	DEVICE ID#	0	0	0	0	1	1	0	1	0	**Device ID (0x01A)** (Equivalent to control bus address = read-only value)
65	41	DAC DITHER	MOD DITHER										**DAC Modulator Dither Select** (To eliminate all non-random noise.) 0 0000 = Dither off 1 0010 = Nominal optimal dither (DEFAULT) 1 1111 = Maximum dither
			ANALOG DITHER										**DAC Analog Output Dither Select** (To eliminate all non-random noise.) 0000 = Dither off 0100 = Nominal optimal dither (DEFAULT) 1111 = Maximum dither
			DEFAULT	1	0	0	0	1	0	1	0	0	**0x124**
69	45	5VOLT BIASING	RESERVED										**RESERVED**
			HVOPU										**Update Bit For HV Override Feature**
			RESERVED										**RESERVED**
			HVOP										**Override To Automatic 3V/5V Bias Select** 0 = Set internal output biasing to be optimal for 3.6V$_{DC}$ or lower operation 1 = Set internal output biasing to be optimal for higher than 3.6V$_{DC}$ operation (DEFAULT)
			DEFAULT	0	0	0	0	0	0	0	0	0	**0x001**
70	46	ALC ENHANCEMENT 1	ALCTBLSEL										**ALC Target Level Table Select** 0 = Target level table spanning -1.5dB through -22.5dB FS (DEFAULT) 1 = Optional ALC target level table spanning -6.0dB through -28.5dB FS
			ALCPKSEL										**ALC Threshold Logic Value Select** 0 = Use rectified peak detector output value (DEFAULT) 1 = Use peak-to-peak detector output value
			ALCNGSEL										**Noise Gate Threshold Logic Value Select** 0 = Use rectified peak detector output value (DEFAULT) 1 = Use peak-to-peak detector output value
			ALCGAINL										**Real-time ALC Gain Value Used By Left Channel PGA**
			DEFAULT	0	0	0	0	1	0	0	0	0	**0x010**

Register		Function	Name	Bit								Description
Dec	Hex			8	7	6	5	4	3	2	1	0	
71	47	ALC ENHANCEMENT 2	PKLIMENA										**ALC Fast Peak Limiter Enable Control** 0 = Enable (DEFAULT) 1 = Disable
			RESERVED										**RESERVED**
			ALCGAINR										**Real-time ALC Gain Value Used By Right Channel PGA**
			DEFAULT	0	0	0	0	1	0	0	0	0	**0x010**
72	48	RESERVED	RESERVED										**RESERVED**
73	49	MISC CONTROLS	4WSPIENA										**SPI 4-wire Force Mode Enable Control** 0 = Disable (DEFAULT) 1 = Enable (Force SPI 4-wire mode regardless of state of MODE #Pin18)
			FSERRVAL										**Short Frame Sync Detection Period Value Select** 00 = Trigger if frame time less than 252 MCLK edges (DEFAULT) 01 = Trigger if frame time less than 253 MCLK edges 10 = Trigger if frame time less than 254 MCLK edges 11 = Trigger if frame time less than 255 MCLK edges
			FSERFLSH										**DSP State Flush On Short Frame Sync Event** 0 = Ignore short frame sync events (DEFAULT) 1 = Set DSP state to initial conditions on short frame sync event
			FSERRENA										**Short Frame Cycle Detection Logic Enable control** 0 = Disable (DEFAULT) 1 = Enable
			NOTCHDLY										**Notch Filter Output Delay Control** 0 = Delay using notch filter output 512 sample times after notch enabled (DEFAULT) 1 = Use notch filter output immediately after notch filter enabled
			DACINMUTE										**DAC Limiter Output Mute Enable Control** (when softmute is enabled.) 0 = DAC limiter output may be exactly zero during softmute (DEFAULT) 1 = DAC limiter output muted to exactly zero during softmute
			PLLLOCKBP										**PLL VCO output Enable control** (When PLL is not in phase locked condition.) 0 = Disable (DEFAULT) 1 = Enable
			DACOSR256										**DAC 256x Oversampling Rate Force Control** (Best at lower sample rates) 0 = Use oversampling rate determined by Register 0x0A[3] (DEFAULT) 1 = Force 256x oversampling rate regardless of Register 0x0A[3]
			DEFAULT	0	0	0	0	0	0	0	0	0	**0x000**
74	4A	INPUT TIE-OFF DIRECT MANUAL CONTROL	MANINENA										**Direct Control Over Input Tie-off Resistor Switch Manual Force General Enable Control** 0 = Ignore Register 0x4A bits to control input tie-off resistor switch (DEFAULT) 1 = Use Register 0x4A bits to override automatic tie-off resistor switch
			MANRAUX										**RAUXIN Input Tie-off Resistor Switch Manual Force Enable Control** (If MANUINEN = 1) 0 = Tie-off resistor switch for RAUXIN input is forced open (DEFAULT) 1 = Tie-off resistor switch for RAUXIN input is forced closed
			MANRLIN										**RLIN Input Tie-off Resistor Switch Manual Force Enable Control** (If MANUINEN = 1) 0 = Tie-off resistor switch for RLIN input is forced open (DEFAULT) 1 = Tie-off resistor switch for RLIN input is forced closed
			MANRMICN										**RMICN Input Tie-off Resistor Switch Manual Force Enable Control** (If MANUINEN = 1) 0 = Tie-off resistor switch for RMICN input is forced open (DEFAULT) 1 = Tie-off resistor switch for RMICN input is forced closed
			MANRMICP										**RMICP Input Tie-off Resistor Switch Manual Force Enable Control** (If MANUINEN = 1) 0 = Tie-off resistor switch for RMICP input is forced open (DEFAULT) 1 = Tie-off resistor switch for RMICP input is forced closed
			MANLAUX										**LAUXIN Input Tie-off Resistor Switch Manual Force Enable Control** (If MANUINEN = 1) 0 = Tie-off resistor switch for LAUXIN input is forced open (DEFAULT) 1 = Tie-off resistor switch for LAUXIN input is forced closed
			MANLLIN										**LLIN Input Tie-off Resistor Switch Manual Force Enable Control** (If MANUINEN = 1) 0 = Tie-off resistor switch for LLIN input is forced open (DEFAULT) 1 = Tie-off resistor switch for LLIN input is forced closed

Register		Function	Name	Bit								Description
Dec	Hex			8	7	6	5	4	3	2	1	0	
			MANLMICN										**LMICN Input Tie-off Resistor Switch Manual Force Enable Control** (If MANUINEN = 1) 0 = Tie-off resistor switch for LMICN input is forced open (DEFAULT) 1 = Tie-off resistor switch for LMICN input is forced closed
			MANLMICP										**LMICP Input Tie-off Resistor Switch Manual Force Enable Control** (If MANUINEN = 1) 0 = Tie-off resistor switch for LMICP input is forced open (DEFAULT) 1 = Tie-off resistor switch for LMICP input is forced closed
			DEFAULT	0	0	0	0	0	0	0	0	0	**0x000**
76	4C	AGC PEAK-TO-PEAK READOUT	P2PVAL										(Read-only register which outputs the instantaneous value contained in the peak-to-peak amplitude register used by the ALC for signal level dependent logic. Value is highest of left or right input when both inputs are under ALC control.)
77	4D	AGCPEAK DETECTOR READOUT	PEAKVAL										(Read-only register which outputs the instantaneous value contained in the peak detector amplitude register used by the ALC for signal level dependent logic. Value is highest of left or right input when both inputs are under ALC control.)
78	4E	AUTOMUTE CONTROL AND STATUS READOUT	RESERVED										**RESERVED**
			AMUTCTRL										**Observation Point Used By DAC Output Automute Feature Select** 0 = Automute operates on data at the input to the DAC digital attenuator (DEFAULT) 1 = Automute operates on data at the DACIN input pin
			HVDET										**Status Bit Of High Voltage Detection Circuit Monitoring VDDSPK Voltage** (Read-only) 0 = Voltage on VDDSPK pin measured at approximately 4.0V_{DC} or less (DEFAULT) 1 = Voltage on VDDSPK pin measured at approximately 4.0V_{DC} or greater
			NSGATE										**Status bit Of Noise Gate Function Logic Control** (Read-only) 0 = Signal is greater than the noise gate threshold and ALC gain can change (DEFAULT) 1 = Signal is less than the noise gate threshold and ALC gain is held constant
			ANAMUTE										**Status Bit Of Analog Mute Function Of DAC Channels** 0 = Non-automute condition (DEFAULT) 1 = Automute condition
			DIGMUTEL										**Status Bit Of Digital Mute Function Of left Channel DAC** 0 = Digital gain value is greater than zero (DEFAULT) 1 = Digital gain is zero either by direct setting or operation of softmute function
			DIGMUTER										**Status Bit Of Digital Mute Function Of Right Channel DAC** 0 = Digital gain value is greater than zero (DEFAULT) 1 = Digital gain is zero either by direct setting or operation of softmute function
			DEFAULT	0	0	0	0	0	0	0	0	0	**0x000**
79	4F	OUTPUT TIE-OFF DIRECT MANUAL CONTROLS	MANOUTEN										**Output Tie-off Resistor Switch Manual Force General Enable Control** 0 = Ignore Register 0x4F bits to control input tie-off resistor/buffer switch (DEFAULT) 1 = Use Register 0x4F bits to override automatic tie-off resistor/buffer switch
			SHRTBUFH										**Bypass Switch Around 1.5x Boost Output Tie-off Buffer Amplifier Manual Force Enable Control** **(If MANUOUTEN = 1)** 0 = Normal automatic operation of bypass switch (DEFAULT) 1 = Bypass switch in closed position when output buffer amplifier is disabled
			SHRTBUFL										**Bypass Switch Around 1.0x Non-boost Output Tie-off Buffer Amplifier Manual Force Enable Control** **(If MANUOUTEN = 1)** 0 = Normal automatic operation of bypass switch (DEFAULT) 1 = Bypass switch in closed position when output buffer amplifier is disabled
			SHRTLSPK										**Left Speaker Output Tie-off Resistor Switch Manual Force Enable Control** **(If MANUOUTEN = 1)** 0 = Tie-off resistor switch for LSPKOUT speaker output is forced open (DEFAULT) 1 = Tie-off resistor switch for LSPKOUT speaker output is forced closed
			SHRTRSPK										**Right Speaker Output Tie-off Resistor Switch Manual Force Enable Control** **(If MANUOUTEN = 1)**

Register		Function	Name	Bit								Description
Dec	Hex			8	7	6	5	4	3	2	1	0	
													0 = Tie-off resistor switch for RSPKOUT speaker output is forced open (DEFAULT) 1 = Tie-off resistor switch for RSPKOUT speaker output is forced closed
			SHRTAUX1										**AUXOUT1 Output Tie-off Resistor Switch Manual Force Enable Control (If MANUOUTEN = 1)** 0 = Tie-off resistor switch for AUXOUT1 output is forced open (DEFAULT) 1 = Tie-off resistor switch for AUXOUT1 output is forced closed
			SHRTAUX2										**AUXOUT2 Output Tie-off Resistor Switch Manual Force Enable Control (If MANUOUTEN = 1)** 0 = Tie-off resistor switch for AUXOUT2 output is forced open (DEFAULT) 1 = Tie-off resistor switch for AUXOUT2 output is forced closed
			SHRTLHP										**Left Headphone Output Tie-off Resistor Switch Manual Force Enable Control (If MANUOUTEN = 1)** 0 = Tie-off resistor switch for LHP output is forced open (DEFAULT) 1 = Tie-off resistor switch for LHP output is forced closed
			SHRTRHP										**Right Headphone Output Tie-off Resistor Switch Manual Force Enable Control (If MANUOUTEN = 1)** 0 = Tie-off resistor switch for RHP output is forced open (DEFAULT) 1 = Tie-off resistor switch for RHP output is forced closed
			DEFAULT	0	0	0	0	0	0	0	0	0	0x000
81	51	POWER REDUCTION AND OUTPUT TIE-OFF DIRECT MANUAL CONTROL	IBTHALFI										**ADC MIX/BOOST Stage Half Bias Current Enable Control** (Reduce supply current by 50%.) 0 = Disable (DEFAULT) 1 = Enable
			RESERVED										**RESERVED**
			IBT500UP										**ADC MIX/BOOST Stage Increase Bias Current Enable Control** (Increase supply current by 500uA.) 0 = Disable (DEFAULT) 1 = Enable
			IBT250DN										**ADC MIX/BOOST Stage Decrease Bias Current Enable Control** (Decrease supply current by 250uA.) 0 = Disable (DEFAULT) 1 = Enable
			MANINBBP										**Bypass Switch Around Input Tie-off Buffer Amplifier Manual Force Enable Control** 0 = Normal automatic operation of bypass switch (DEFAULT) 1 = Bypass switch in closed position when input buffer amplifier is disabled
			MANINPAD										**Switch To Ground Tie-off Buffer Amplifier Manual Force Enable Control** 0 = Normal automatic operation of switch to ground (DEFAULT) 1 = Switch to ground in closed position when input buffer amplifier is disabled
			MANVREFH										**Switch For V_{REF} 600k-Ohm Resistor To Ground Manual Force Enable Control** 0 = Switch to ground controlled by REG0x01 (DEFAULT) 1 = Switch to ground in the closed position
			MANVREFM										**Switch For V_{REF} 160k-Ohm Resistor To Ground Manual Force Enable Control** 0 = Switch to ground controlled by REG0x01 (DEFAULT) 1 = Switch to ground in the closed position
			MANVREFL										**Switch For V_{REF} 6k-Ohm Resistor To Ground Manual Force Enable Control** 0 = Switch to ground controlled by REG0x01 (DEFAULT) 1 = Switch to ground in the closed position
			DEFAULT	0	0	0	0	0	0	0	0	0	0x000

15 Appendix D: Register Overview

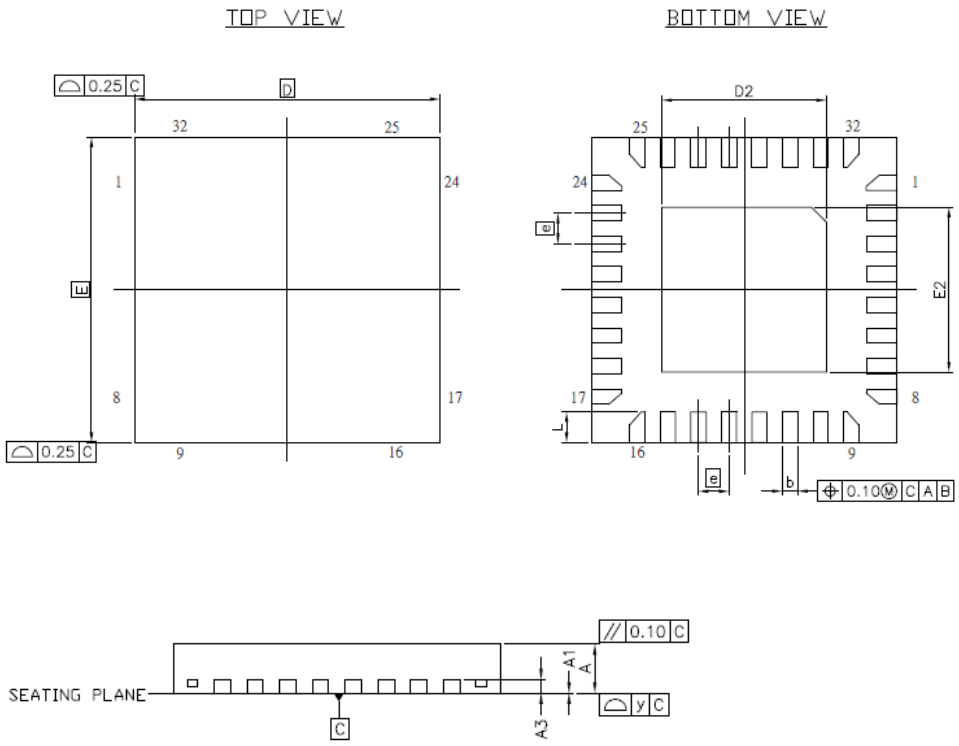
DEC	HEX	NAME	Bit 8	Bit 7	Bit 6	Bit5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
0	00	SOFTWARE RESET	RESET (SOFTWARE)									000
1	01	POWER MANAGEMENT 1	DCBUFEN	AUX1MXEN	AUX2MXEN	PLLEN	MICBIASEN	ABIASEN	IOBUFEN	REFIMP		000
2	02	POWER MANAGEMENT 2	RHPEN	NHPEN	SLEEP	RBSTEN	LBSTEN	RPGAEN	LPGAEN	RADCEN	LADCEN	000
3	03	POWER MANAGEMENT 3	AUXOUT1EN	AUXOUT2EN	LSPKEN	RSPKEN	RESERVED	RMIXEN	LMIXEN	RDACEN	LDACEN	000
GENERAL AUDIO CONTROLS												
4	04	AUDIO INTERFACE	BCLKP	LRP	WLEN		AIFMT		DACPHS	ADCPHS	MONO	050
5	05	COMPANDING	0	0	0	CMB8	DACCM		ADCCM		ADDAP	000
6	06	CLOCK CONTROL 1	CLKM	MCLKSEL			BCLKSEL			0	CLKIOEN	140
7	07	CLOCK CONTROL 2	4WSPIEN	0	0	0	0	SMPLR			SCLKEN	000
8	08	GPIO	0	0	0	GPIO1PLL		GPIO1PL	GPIO1SEL			000
9	09	JACK DETECT 1	JCKMIDEN		JCKDEN	JCKDIO		0	0	0	0	000
10	0A	DAC CONTROL	0	0	SOFTMT	0	0	DACOS	AUTOMT	RDACPL	LDACPL	000
11	0B	LEFT DAC VOLUME	LDACVU	LDACGAIN								0FF
12	0C	RIGHT DAC VOLUME	RDACVU	RDACGAIN								0FF
13	0D	JACK DETECT 2	0	JCKDOEN1				JCKDOEN0				000
14	0E	ADC CONTROL	HPFEN	HPFAM	HPF			ADCOS	0	RADCPL	LADCPL	100
15	0F	LEFT ADC VOLUME	LADCVU	LADCGAIN								0FF
16	10	RIGHT ADC VOLUME	RADCVU	RADCGAIN								0FF
17	11	RESERVED										006
EQUALIZER												
18	12	EQ1-LOW CUTOFF	EQM	0	EQ1CF		EQ1GC					12C
19	13	EQ2-PEAK 1	EQ2BW	0	EQ2CF		EQ2GC					02C
20	14	EQ3-PEAK 2	EQ3BW	0	EQ3CF		EQ3GC					02C
21	15	EQ4-PEAK3	EQ4BW	0	EQ4CF		EQ4GC					02C
22	16	EQ5-HIGH CUTOFF	0	0	EQ5CF		EQ5GC					02C
23	17	RESERVED										000
DAC LIMITER												
24	18	DAC LIMITER 1	DACLIMEN	DACLIMDCY				DACLIMATK				032
25	19	DAC LIMITER 2	0	0	DACLIMTHL			DACLIMBST				000
26	1A	RESERVED										000
NOTCH FILTER												
27	1B	NOTCH FILTER 1	NFCU1	NFCEN	NFCA0[13:7]							000
28	1C	NOTCH FILTER 2	NFCU2	0	NFCA0[6:0]							000
29	1D	NOTCH FILTER 3	NFCU3	0	NFCA1[13:7]							000
30	1E	NOTCH FILTER 4	NFCU4	0	NFCA1[6:0]							000
31	1F	RESERVED										000
ALC AND NOISE GATE CONTROL												
32	20	ALC CONTROL 1	ALCEN		0	ALCMXGAIN			ALCMNGAIN			038
33	21	ALC CONTROL 2	0	ALCHT				ALCSL				00B
34	22	ALC CONTROL 3	ALCM	ALCDCY				ALCATK				032

DEC	HEX	NAME	Bit 8	Bit 7	Bit 6	Bit5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
35	23	NOISE GATE	0	0	0	0	0	ALCNEN	ALCNTH			000
PHASE LOCKED LOOP												
36	24	PLL N	0	0	0	0	PLLMCLK	PLLN				008
37	25	PLL K 1	0	0	0	PLLK[23:18]						00C
38	26	PLL K 2	PLLK[17:9]									093
39	27	PLL K 3	PLLK[8:0]									0E9
40	28	RESERVED										000
MISCELLANEOUS												
41	29	3D CONTROL	0	0	0	0	0	3DDEPTH				000
42	2A	RESERVED										000
43	2B	RIGHT SPEAKER SUBMIX	0	0	0	RMIXMUT	RSUBBYP	RAUXRSUBG			RAUXSMUT	000
44	2C	INPUT CONTROL	MICBIASV		RLINRPGA	RMICNRPGA	RMICPRPGA	0	LLINLPGA	LMICNLPGA	LMICPLPGA	033
45	2D	LEFT INPUT PGA GAIN	LPGAU	LPGAZC	LPGAMT	LPGAGAIN						010
46	2E	RIGHT INPUT PGA GAIN	RPGAU	RPGAZC	RPGAMT	RPGAGAIN						010
47	2F	LEFT ADC BOOST	LPGABST	0	LPGABSTGAIN			0	LAUXBSTGAIN			100
48	30	RIGHT ADC BOOST	RPGABST	0	RPGABSTGAIN			0	RAUXBSTGAIN			100
49	31	OUTPUT CONTROL	0	0	LDACRMX	RDACLMX	AUX1BST	AUX2BST	SPKBST	TSEN	AOUTIMP	002
50	32	LEFT MIXER	LAUXMXGAIN			LAUXLMX	LBYPMXGAIN			LBYPLMX	LDACLMX	001
51	33	RIGHT MIXER	RAUXMXGAIN			RAUXRMX	RBYPMXGAIN			RBYPRMX	RDACRMX	001
52	34	LHP VOLUME	LHPVU	LHPZC	LHPMUTE	LHPGAIN						039
53	35	RHP VOLUME	RHPVU	RHPZC	RHPMUTE	RHPGAIN						039
54	36	LSPKOUT VOLUME	LSPKVU	LSPKZC	LSPKMUTE	LSPKGAIN						039
55	37	RSPKOUT VOLUME	RSPKVU	RSPKZC	RSPKMUTE	RSPKGAIN						039
56	38	AUX2 MIXER	0	0	AUXOUT2MT	0	0	AUX1MIX>2	LADCAUX2	LMIXAUX2	LDACAUX2	001
57	39	AUX1 MIXER	0	0	AUXOUT1MT	AUX1HALF	LMIXAUX1	LDACAUX1	RADCAUX1	RMIXAUX1	RDACAUX1	001
BEGIN NAU88C22 PROPRIETARY REGISTER SPACE												
58	3A	POWER MANAGEMENT 4	LPDAC	LPIPBST	LPADC	LPSPKD	MICBIASM	REGVOLT		IBADJ		000
PCM TIME SLOT AND ADCOUT IMPEDANCE OPTION CONTROL												
59	3B	LEFT TIME SLOT	LTSLOT[8:0]									000
60	3C	MISC	PCMTSEN	TRI	PCM8BIT	PUDEN	PUDPE	PUDPS	RESERVED	RTSLOT[9]	LTSLOT[9]	020
61	3D	RIGHT TIME SLOT	RTSLOT[8:0]									020
SILICON REVISION AND DEVICE ID												
62	3E	DEVICE REVISION #	RESERVED	REV = 0X07F FOR REV-A								07F
63	3F	DEVICE ID	ID									01A
65	41	DAC DITHER	MODE DITHER					ANALOG DITHER				110
70	46	ALC ENHANCEMENTS	ALCTBLSEL	ALCPKSEL	ALCNGSEL	ALCGAINL						010
71	47	ALC ENHANCEMENTS	PKLIMENA	RESERVED		ALCGAINR						010
72	48	RESERVED										000
73	49	MISC CONTROLS	4WSPIENA	FSERRVAL		FSERFLSH	FSERRENA	NOTCHDLY	DACINMUTE	PLLLOKBP	DACOS256	000
74	4A	TIE-OFF OVERRIDES	MANINENA	MANRAUX	MANRLIN	MANRMICN	MANRMICP	MANLAUX	MANLLIN	MANLMICN	MANLMICP	000
76	4C	P2P DETECTOR READ	P2PVAL									000
77	4D	PEAK DETECTOR READ	PEAKVAL									000

DEC	HEX	NAME	Bit 8	Bit 7	Bit 6	Bit5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
78	4E	CONTROL AND STATUS	RESERVED	RESERVED	RESERVED	AMUTCTRL	HVDET	NSGATE	ANAMUTE	DIGMUTEL	DIGMUTER	000
79	4F	OUTPUT TIE-OFF CTRL	MANOUTEN	SHRTBUFH	SHRTBUFL	SHRTLSPK	SHRTRSPK	SHRTAUX1	SHRTAUX2	SHRTLHP	SHRTRHP	000
81	51	POWER/TIE-OFF CTRL	IBTHALFI	RESERVED	IBT500UP	IBT250DN	MANINBBP	MANINPAD	MANVREFH	MANVREFM	MANVREFL	000

16 Package Dimensions

32-lead plastic QFN 32L; 5X5mm^2, 0.8mm thickness, 0.5mm lead pitch



SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	28	30	32
A1	0	0.02	0.05	0	0.8	2.0
A3	0.203 REF			8 REF		
b	0.18	0.25	0.30	7	10	12
D	4.90	5.00	5.10	193	197	201
D2	2.60	2.70	2.80	102.4	106.3	110.2
E	4.90	5.00	5.10	193	197	201
E2	2.60	2.70	2.80	102.4	106.3	110.2
e	0.50 BSC			19.7 BSC		
L	0.30	0.40	0.50	12	16	20
y	0.10			4		

17 Ordering Information

Part Number	Dimension	Package	Package Material
NAU8822AYG	5x5 mm	QFN-32	Green

NAU8822A _ _

Package Material:

G = Pb-free Package

Package Type:

Y = 32-Pin QFN Package

18 Revision history

VERSION	DATE	PAGE	DESCRIPTION
1.0	July 29, 2009		Initial Release
2.0	January 25, 2011	17	Corrected location of low power mic bias bit from R40 to R58
2.1	November 08, 2011	39,41 88	PLL registers programming sequence is required to keep the IMCLK not greater than 12.288MHz. QFN32 Package diagram updated
2.2	November 20, 2014	52	Corrected Tsdio setup time
2.3	June 10, 2015	88	Updated package dimensions
2.4	March 2016	34	Add Important Notice
2.5	July 2016	41	Revise f1 equation from * to /
2.6	Mach, 2017	91	Added the automotive ordering part number
2.7	July 2018	55	Low pass filters added in control pins
2.8	Nov 2, 2020	38-41	PLL IMCLK Description Update Output Control register Update
2.9	Mar 23, 2021	35-36	Speaker Outputs Description Update Auxiliary Outputs Description Update
3.0	May 5, 2021	91	Table 13 Mode pin=0 for SPI 4 Wire removal, and 9.1 last paragraph removal
3.1	May 17, 2021	43 86	Section 9.6 Appendix D
3.2	Oct 20, 2021	39 65-88	Removed 96KHz/192KHz Setting Updated Register Table Format

Table 23: Revision History

s

Important Notice

Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, "Insecure Usage".

Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.