General Description

The CCX1030 is a WPC QI 1.2.4 compliant and high integrated wireless power transmitter SOC. It can work under large input voltage ranging from 4.25V to 21V and deliver 5W/7.5W/10W/15W output power. The chip integrates everything except power mosfets and some passive components. These include a switch step-down converter, two linear regulators (1.8V and 3.3V), a microprocessor , Q detector, two high voltage gate driver groups , voltage and current ASK decoder circuits etc.

The CCX1030 has very low standby power consumption and high charging efficiency (up to 85% in 15W WPT situation).The chip supports fast charging power adaptors of different protocols, including USB PD, QC 2.0/3.0 etc. Meanwhile, it supports off-chip DCDC voltage tuning. The chip can realize Apple 7.5W fixed frequency voltage tuning charging by off-chip DCDC or QC 3.0 adaptors. CCX1030 provides a wide range of system protection including over-current, over-voltage, under-voltage lockout and over-temperature management to ensure the safety of the wireless charging system under abnormal conditions. Users can read voltage, current, frequency and all kinds of abnormal protection information conveniently through I2C interface. CCX1030 is available in a lead-free and space-saving 5x5 QFN 32pin package. The product is rated for an operating temperature range from -40℃ to +85℃.

Features

- WPC-1.2.4 compliant, flexible coil configuration
- Wide input voltage range:4.25V to 21V and high efficiency buck converter
- 5W/7.5W/10W/15W high efficient power transfer with typical 85% efficiency at 15W output
- Supports fast charging power adaptors of USB PD,QC 2.0/3.0 etc
- Integrated current detect amplifier, embedded voltage and current ASK decoder.
- Low standby power consumption with typical 8mA standby current.
- Supports NTC detection
- Supports 127.7KHz fixed frequency and voltage tuning by QC 3.0 protocols or off-chip DCDC
- Supports WPC EPP Q detection or self-defined Q detection with programmable FOD sensitivity
- Integrated 32bit ARM Cortex M0 microprocessor
- Supports over-voltage, over-current, over-temperature detection and protection
- Supports program update ,debug and control through I2C interface
- Power transfer LED indicators
- 5mm x 5mm 0.5pitch QFN 32pin package

Typical Applications

- BPP and EPP charging Pad
- BPP and EPP vertical charging Pad
- Transmitter for smart watch
- Power bank
- Cradles
- Tablets
- Portable instruments

Description for Implementation

1 Overview and function

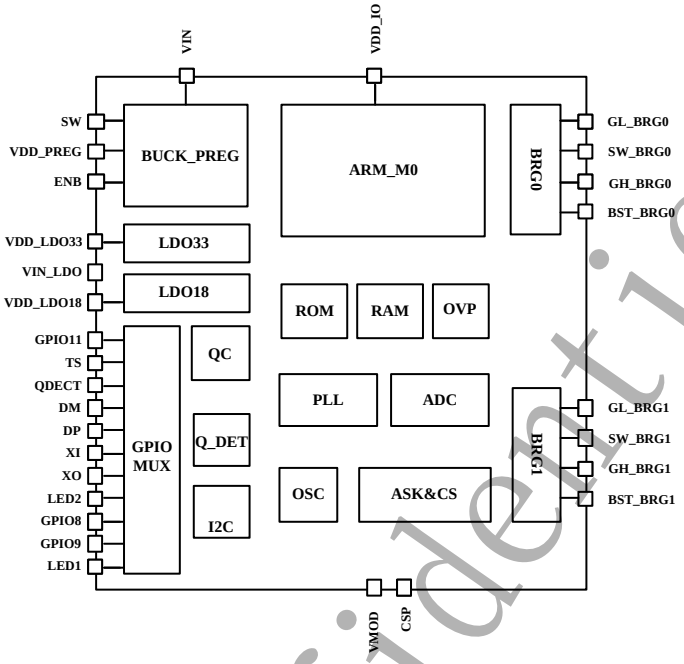


Fig1 CCX1030 function block diagram

Fig1 is the function block diagram of CCX1030 which is compliant with QI 1.2.4 and supports 5W/7.5W/10W/15W transmission power. The chip integrates high efficient buck, linear LDOs , ADC, PLL, ARM M0 processor, two groups of high voltage gate drivers, fast charging protocol controllers and Q detector circuits. The high efficient buck can work stably with input voltage from 4.25V to 21V and be bypassed when it is below the working voltage. It can automatically change the PFM and PWM modulation according to the load condition which can get best efficiency in different conditions.

The CCX1030 high voltage drivers change DC power to AC power with external MOS. The drivers can be configured with different dead zone time and driving ability according to external MOS conditions. Each PWM's frequency and duty cycle can be configured independently from 110KHz to 200KHz frequency output. High resolution PLL can realize 1Hz frequency step and 0.1% duty PWM resolution. The CCX1030 provides the 127.7 KHz Apple 7.5W fast wireless charging with 16M/32M crystal. Q factor detector is the key feature which can realize the object detection, FOD detection and low standby power operation. The chip can be completely shut down when ENB pin is tied to high.

The Chip realizes the communication with the receiver through ASK and FSK modulation. It supports voltage and current ASK demodulation without any external active device. The patented demodulation algorithm can ensure the charging stability under various interferences and different positions. The high speed PWM clock guarantees that the difference between FSK reference frequency and modulation frequency conforms to QI EPP standard.

The CCX1030 supports internal voltage, current, temperature detection and abnormal protection. External NTC protection can be used to ensure chip charging safety. Two LED outputs are used to indicate charging status and abnormal protection. FOD sensitivity can be set according to user's requirement.

2 Pin Definition and Descriptions

2.1 Pin Definition

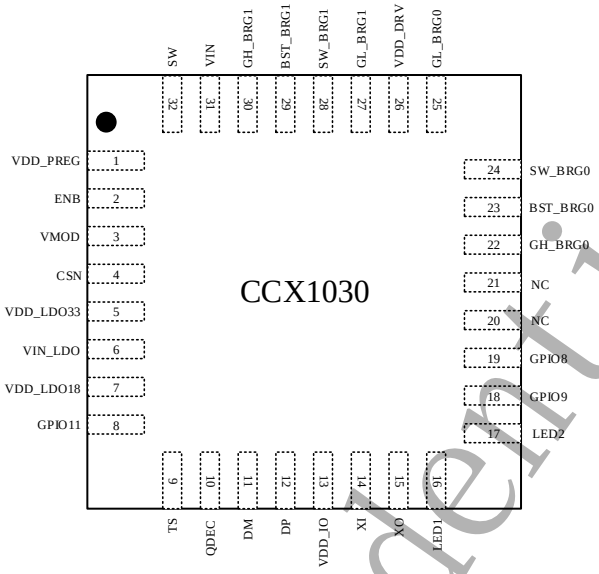


Fig 2 CCX1030 Pin Definition (QFN 32pin 5mm x 5mm, 0.5mm pitch)

2.2 Pin Description

Order	Name	I/O Type	Description
1	VDD_PREG	PO (5V)	Regulated 5V output used for Internal device biasing, connect a 1uF capacitor from this pin to ground
2	ENB	AI	Active-LOW enable pin. When connected to logic HIGH, enters the Shut Down Mode. When connected to logic LOW, enter the Normal Mode.
3	VMOD	AI	Voltage Mode ASK demodulation pin for data packets based on coil voltage variation;
4	CSN	AI	Current Sense amplifier negative input terminal
5	VDD_LDO33	PO (3.3V)	Regulated 3.3V output used for internal device biasing. Connect a 1 µF capacitor from this pin to ground.
6	VIN_LDO	PI (5.0V)	Regulated 3.3V output used for internal device biasing. Connect a 1 µF capacitor from this pin to ground.
7	VDD_LDO18	PO (1.8V)	Regulated 1.8V output used for internal device biasing. Connect a 1 µF capacitor from this pin to ground
8	GPIO11	D/A-IO	USB PD CCID connection pin (GPIO optional)
9	TS	D/A-IO	Temperature sensor (GPIO optional)
10	QDEC	D/A-IO	Q factor detection function (GPIO optional)

11	DM	D/A-IO	USB negative interface function (GPIO optional)
12	DP	D/A-IO	USB positive interface function (GPIO optional)
13	VDD_IO	PO(3.3V)	Internal digital IO power supply Connect a 1μF capacitor from this pin to ground.
14	XI	D/A-IO	Crystal oscillator input function (GPIO optional)
15	XO	D/A-IO	Crystal oscillator output function (GPIO optional)
16	LED1	D/A-IO	LED1 open drain output (IDAC output optional)
17	LED2	D/A-IO	LED2 open drain output (IDAC output optional) The pin is forbidden to tie GND LED2不能接GND或悬空
18	GPIO9	D/A-IO	General purpose I/O; Used as I2C SCL clock (recommended)
19	GPIO8	D/A-IO	General purpose I/O; Used as I2C SDA data (recommended)
20	NC		
21	NC		
22	GH_BRG0	DO	Gate driver output for the high-side FET of half bridge group-0.
23	BST_BRG0	DI	Bootstrap pin for half bridge group-0. Tie an external capacitor from this pin to the SW_BRG0 pin to generate a drive voltage higher than the input voltage.
24	SW_BRG0	DO	Switch node for half bridge group-0.
25	GL_BRG0	DO	Gate driver output for the low-side FET of half bridge group-0.
26	VDD_DRV	PI	Input power supply for the internal gate drivers. Connect a 10μF capacitor from this pin to ground.
27	GL_BRG1	DO	Gate driver output for the low-side FET of half bridge group-1.
28	SW_BRG1	DO	Switch node for half bridge group-1.
29	BST_BRG1	DI	Bootstrap pin for half bridge group-1. Tie an external capacitor from this pin to the SW_BRG1 pin to generate a drive voltage higher than the input voltage.
30	GH_BRG1	DO	Gate driver output for the high-side FET of half bridge group-1.
31	VIN	AI	input voltage terminal
32	SW	DO	Switch node for the Buck

3 Electrical Characteristic

3.1 Absolute Maximum Ratings

Item(V/I)	Pin Name	Min	Max	Unit
Input Voltage	VIN, SW, SW_BRG0/1	-0.3	24	V
	BST_BRG0/1 GH_BRG0/1	-0.3	SW_BRGx +6	V
	other pins	-0.3	6	V
	VDD_LDO18	-0.3	2	V
	GND/EPAD	-0.3	0.3	V
Source Current	GPIO8,GPIO9	0	30 上拉能力	mA
Sink Current	GPIO8,GPIO9	0	40 下拉能力	mA

3.2 ESD Ratings

Test Model	Min	Max	Unit	Note
Human Body Model (HBM)		2	KV	All pins
Charged Device Model (CDM)		500	V	All pins
Machine Model (MM)		200	V	All pins

3.3 Recommended Operating Conditions

Rating	Min	Typ	Max	Unit
Input Operating Range, V_{IN}	4.25	12	21	V
Analog voltage Range V_{DD_LDO33}	3.0	3.3	3.6	V
Input Voltage Range for GPIO, V_{DD_IO}	1.8	3.3	3.6	V
Digital voltage range, V_{DD_LDO18}	1.62	1.8	1.98	V
Ambient Temperature, T_A	0		85	℃
Junction Temperature, T_J	-20		125	℃

3.4 Electrical Characteristic

Note: V_{IN} = 5V or 12V, ENB=0, MP-A2 Coil , T_A = -40 to 85℃; Typical values aret 25℃, use IDT9221 as receivers, unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Unit
System Efficiency					
15W WPT	@V_{IN}=12V & I_{LOAD}=1.3A		85		%
10W WPT	@V_{IN}=12V & I_{LOAD}=0.8A		85		%
5W WPT	@V_{IN}=12V & I_{LOAD}=0.4A		80		%
5W WPT	@V_{IN}=5V & I_{LOAD}=1A		79		%
Input Supplies and UVLO					
Input Operating Range, V_{IN}		4.25	5/9/12	21	V
Under-Voltage Lockout, V_{IN_UVLO}	V_{IN} rising		3.74		V
Under-Voltage Hysteresis, V_{IN_UVHYS}	V_{IN} falling		0.34		V
Operating Mode Input Current, I_{IN}	Power Transfer Phase @V_{IN}=12V		16	20	mA
Standby Mode Current, I_{STDBY}	Periodic Ping		8		mA
Shut Down Current, I_{SHD}	ENB=5V		8		uA
Enable Pin Threshold (ENB)					
Input Threshold HIGH, V_{IH}		2.5			V
Input Threshold LOW, V_{IL}				0.5	V
ENB Pin Input Leakage Current, I_{ENB_LKG}	V_{ENB}=0V (Grounded or NC)		0.2		uA
	V_{ENB}=5V		4		uA
Buck Regulator (DCDC)					
Buck Output Voltage, V_{OUT}	@V_{IN}=12V, C_{OUT} = 10μF; L=4.7μH	4.5	5.0	5.5	V
Buck Output Current, I_{OUT}	@V_{IN}=12V, C_{OUT} = 10μF; L=4.7μH		20		mA
Buck Efficiency, η_{EFF}	@V_{IN}=12V, I_{OUT}=20mA		73.5		%
N-Channel MOSFET Drivers					
High Side Rise/Fall Time, T_{HS_RF}	@ C_L=3nF (10%-90%) (Driver Strength 0/3)	35		133	ns
Low Side Rise/Fall Time, T_{LS_RF}	@ C_L=3nF (10%-90%) (Driver Strength 0/3)	35		133	ns
Crystal Oscillator (XO)					
XO Frequency, F_{XO}	Support 16M/32M crystal, recommend 32M	16	32		MHz
Frequency Accuracy	Support apple mode 127.7KHz (+/-47ppm)		20	40	ppm
ADC					
VIN_ADC	ADC input voltage		3.3		V
N_ADC	Number of bits		11		bit

N_CHANNEL			16		N
S_ADC	ADC sample rate		250		KSPS
IDAC (full range and resolution based on output load resistor)					
VIN_DAC	DAC output voltage range		3.3		V
N_DAC			6		bits
Current Sense (CS)					
Input Amplifier offset voltage, V_{SEN_OFST}	@V_{CSP} = V_{CSN}		0.6		mV
	@ ±3 sigma			12	mV
Measured CS Accuracy, I_{SEN_ACC}	V_{R_ISEN} = 25mV, I_{SEN}=1.25A @ R_{SEN}=20mΩ		±3.5	±5	%
Over Current Protection (OCP) (programmable)					
Over Current Protection, I_{OCP}	@15W WPT, R_{SEN}=20mΩ		2		A
Over Current hysteresis, I_{OCP_hys}	@ OCP falling hysteresis		0.2		A
Over Voltage Protection (OVP) (programmable)					
Over Voltage Protection, V_{OVP}	@VIN Rising		25		V
Over Voltage hysteresis, V_{OVP_hys}	@VIN falling hysteresis		4		V
Low Voltage Detector (LVD) (programmable)					
Low Voltage Detector, V_{LVD}	@VIN Falling		5		V
Low Voltage Detector, V_{LVD_hys}	@VIN rising hysteresis		0.3		V
Thermal Protection (OTP) (programmable)					
Thermal Warning, T_{J_WAR}	Die Junction Temp Rising		120		℃
T_{J_WAR} Hysteresis, T_{J_HYS}	Die Junction Temp Falling		20		℃
Thermal Shutdown, T_{J_SD}	Die Junction Temp Rising		140		℃
T_{J_SD} Hysteresis, T_{J_HYS}	Die Junction Temp Falling		20		℃
I2C Interface (SCL, SDA)					
Clock Frequency, F_{SCL}	As I2C Slave		100	300	kHz
Capacitive Load, C_B			150		pF
Input Capacitance, C_I			5		pF
Digital Input/ Output Pins Logic Levels (GPIO)					
Input Voltage HIGH Level, V_{IH}	> 0.7*VDD_IO	70			%
Input Voltage LOW Level, V_{IL}	< 0.3*VDD_IO			30	%
Leakage Current, I_{LKG}	@VIN=3.3V		±1	10	uA
Output Logic HIGH, V_{OH}	> 0.9*VDD_IO	90			%
Output Logic LOW, V_{OL}	< 0.1*VDD_IO			10	%
Source Current, I_{SRC}	@ V_{GS}=3.3V, R_{ON}=100Ω	4	12		mA
Sink Current, I_{SINK}	@ V_{GS}=3.3V, R_{ON}=80Ω	4	12		mA

4 Application Guide

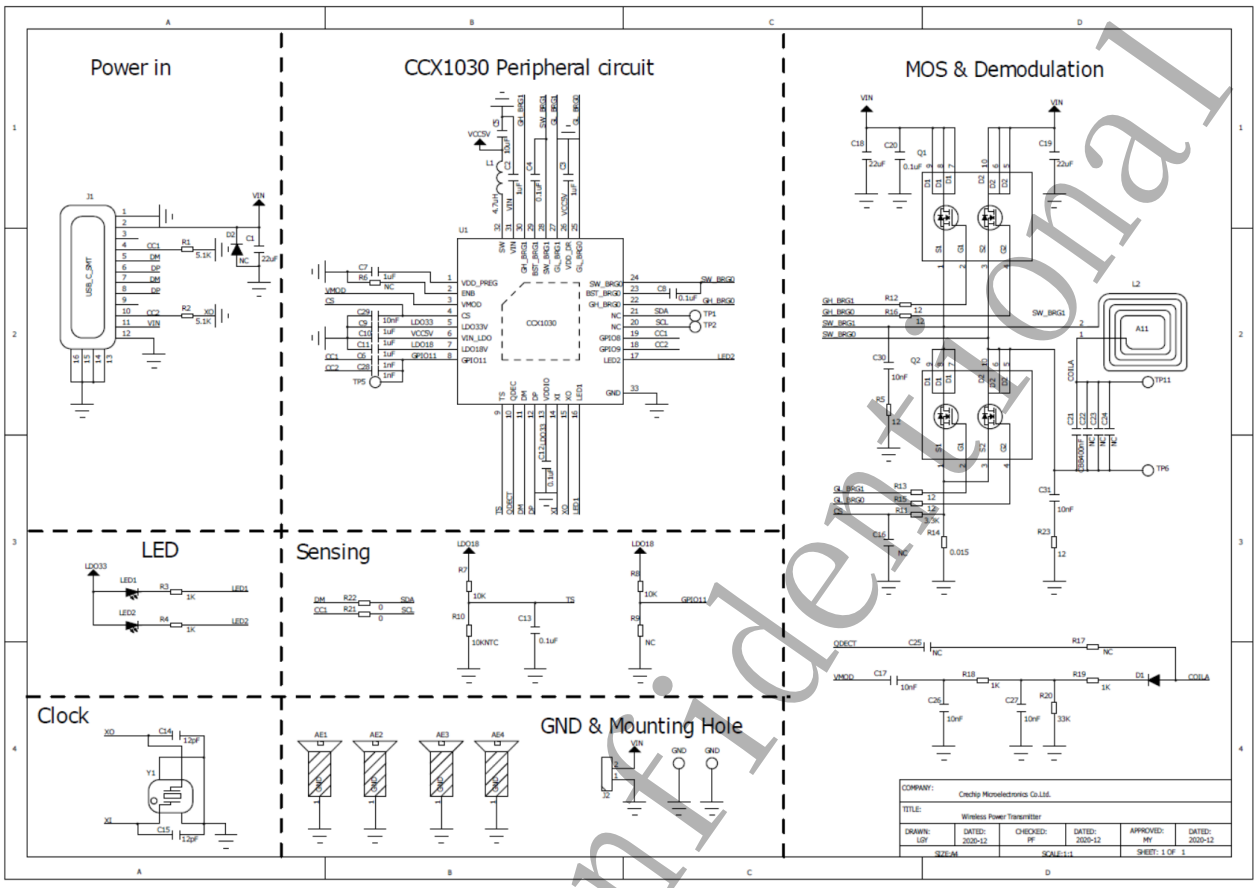


Fig3 CCX1030 application Diagram

Item	Index	Value	Qty	Decal	Part Number	Manufacturer	Reference
1	CAP	12pF	2	CAP0402	CC0402JRNP09BN120	YAGEO	C14-15
2	CAP	100pF	1	CAP0402	GRT1555C2A101JA02D	Murata	C25
3	CAP	1nF	2	CAP0402	CC0402KRX7R9BB102	YAGEO	C6 C28
4	CAP	10nF	6	CAP0402	CC0402KRX7R9BB103	YAGEO	C17 C26-27 C29-31
5	CAP	0.1uF	5	CAP0402	CL05A104KA5NNND	SAMSUNG	C4 C8 C12-13 C20
6	CAP	1uF	6	CAP0402	CL05A105KA5NQNC	SAMSUNG	C2-3 C7 C9-11
7	CAP	10uF	1	CAP0603	CL10A106MA8NRNC	SAMSUNG	C5
8	CAP	22uF	3	CAP0805	CL21A226MAQNNNE	SAMSUNG	C1 C18-19
9	CAP	CBB400nF	1	P7.5	404J100V	ZZEC	C21
10	IC	CCX1030	1	QFN32	CCX1030	Crechip	U1
11	IND	A11	1	MP-A2	BT-S5352320HU-MPA2SXX	BTCOIL	L2
12	CRY	32MHz	1	3.2x2.5mm	1C232000AA0B	KDS	Y1
13	DIO	BAV21W	1	SOD123	BAV21W-7-F	DIO	D1
14	IND	4.7uH	1	IND2012	CIG10W4R7MNC	SAMSUNG	L1
15	LED	Green	2	LED0603	LTST-C190GKT	LITEON	LED1-2
16	MOS	QN3121M3N	2	DFN3x3mm	QN3121M3N	UPI	Q1-2
17	RES	0	2	RES0402	RC0402JR-070RL	YAGEO	R21-22
18	RES	12	6	RES0402	RC0402FR-0712RL	YAGEO	R5 R12-13 R15-16 R23
19	RES	1K	4	RES0402	C-02W1001FT	FH	R3-4 R18-19
20	RES	3.3K	1	RES0402	C-02W3301FT	FH	R11
21	RES	5.1K	2	RES0402	RC-02W5101FT	FH	R1-2
22	RES	10K	2	RES0402	RC0402FR-0710KL	Yegao	R7-8
23	RES	33K	1	RES0402	RC-02W3302FT	FH	R20
24	RES	0.015	1	RES0805	RBF-06YR015FT	FH	R14
25	RES	10K/NTC	1	805	CMFB103F3950FANT	FH	R10
26	CON	Type-C	1	SMD	TYPE-C16PIN	SHOUHAN	J1

Fig 4 CCX1030 BOM List (Recommended)

5 Typical Performance

Note: V_{IN} = 12V, ENB=0, MP-A2 coil, T_A = -40 to 85℃;Typical values are at 25℃, unless otherwise noted.

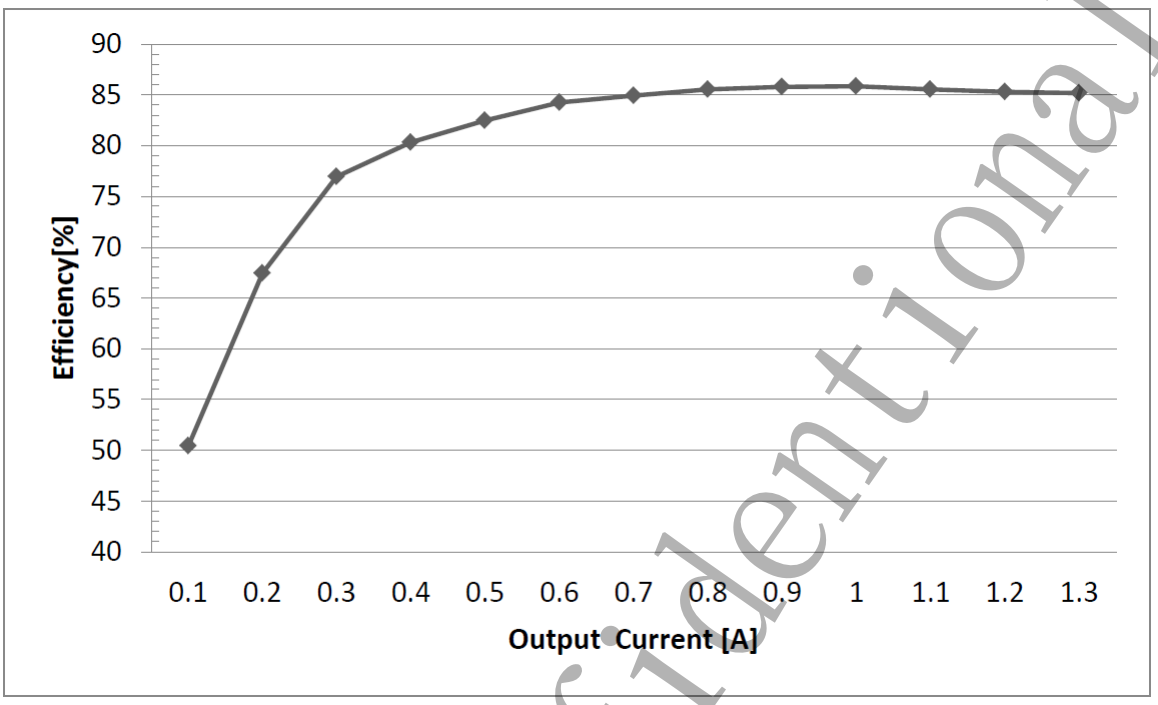


Fig5 WPT Efficiency vs Output Load : Vout_Rx =12V (Rx with IDT9221)

Note: V_{IN} = 5V, ENB=0, A11 coil, T_A = -40 to 85℃;Typical values are at 25℃, unless otherwise noted.

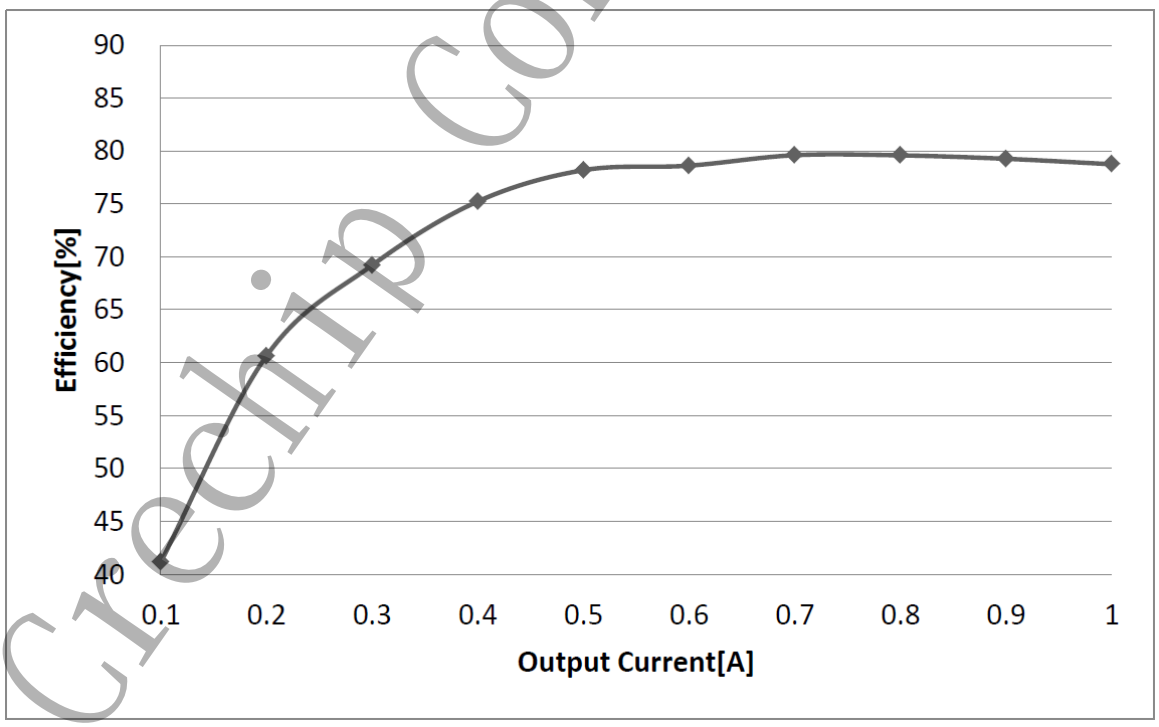
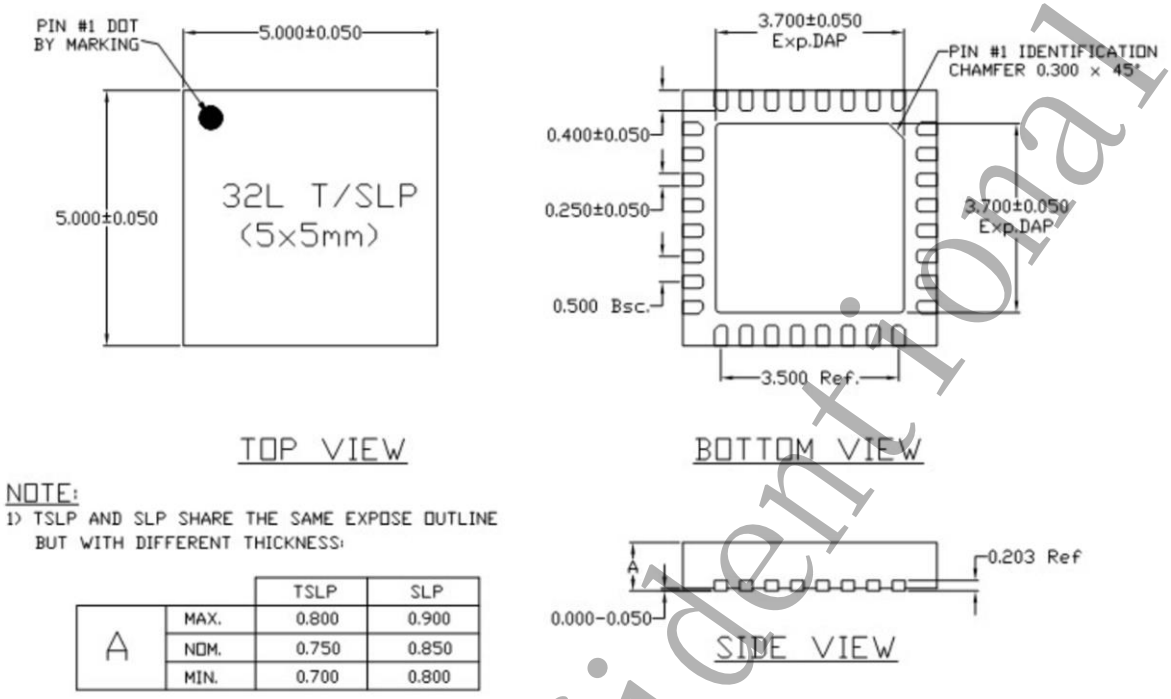


Fig6 WPT Efficiency vs Output Load : Vout_Rx =5V (Rx with electrical load)

6 Package information



		TSLP	SLP
A	MAX.	0.800	0.900
	NOM.	0.750	0.850
	MIN.	0.700	0.800

Fig7 CCX1030 Package information

7 Revision History

Date	Version	Description	Owner
March-2,2020	V1.0	Initial draft version for CCX1030	
March-3,2020	V1.1	Add the Bom List	
March-10,2020	V1.2	Update PD reference design	
December-12, 2020	V1.3	Update SCH\Layout\BOM	