

N-Channel MOSFET

Applications:

- Adaptor
- Charger
- .SMPS

Lead Free Package and Finish

V _{DSS}	R _{DS(ON)} (Typ.)	I _D
650V	2.3Ω	5A

Features:

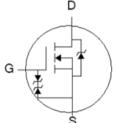
- RoHS Compliant
- Low ON Resistance
- Low Gate Charge
- Peak Current vs Pulse Width Curve
- Inductive Switching Curves

Ordering Information

PART NUMBER	PACKAGE	BRAND					
LSU05N65A	TO-251	IPS					







T_C=25°C unless otherwise specified **Absolute Maximum Ratings**

Symbol	Parameter	LSU05N65A	Units
V_{DSS}	Drain-to-Source Voltage	650	V
I _D	Continuous Drain Current	5	Α
I _{DM}	Pulsed Drain Current, V _{GS} @10V (NOTE *2)	20	Α
D	Power Dissipation	70	W
P _D	Derating Factor above 25℃	0.56	W/℃
V _{GS}	Gate-to-Source Voltage	±20	V
E _{AS}	Single Pulse Avalanche Energy(L=10mH)	150	mJ
E _{AR}	Avalanche Energy ,Repetitive	30	mJ
I _{AR}	Avalanche Current	2.5	Α
VESD(G-S)	Gate to Source ESD(HBM-C=100pF,R=1.5KΩ)	3000	V
TL	Maximum Temperature for Soldering	300	
T _J and T _{STG}	Operating Junction and Storage Temperature Range (NOTE *1)	-55 to150	${\mathbb C}$

Thermal Resistance

Symbol	Parameter	Тур.	Max.	Units	Test Conditions
$R_{\theta,JC}$	Junction-to-Case		1.78		Water cooled heatsink, P _D adjusted for a
000				°C⁄W	peak junction temperature of +150°C.
$R_{\theta JA}$	Junction-to-Ambient		62.5		1 cubic foot chamber, free air.

OFF Characteristics $T_C=25^{\circ}C$ unless otherwise specified

- Ст Ст.							
Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions	
BV _{DSS}	Drain-to-Source Breakdown Voltage	650			V°C	V_{GS} =0V, I_D =250 μ A	
	Drain-to-Source Leakage Current			- 1	- μΑ	V _{DS} =650V, V _{GS} =0V	
						T _J =25°C	
I _{DSS}				100		V_{DS} =520V, V_{GS} =0V	
				100		T _J =125℃	
	Gate-to-Source Forward Leakage			+10		V _{GS} =+20V	
I _{GSS}	Gate-to-Source Reverse Leakage			-10	uA	V _{GS} = -20V	

ON Characteristics T_J=25°C unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
В	StaticDrain-to-Source		2.2	2.8	Ω	V_{GS} =10V, I_D =2.5A
R _{DS(ON)}	On-Resistance(NOTE *3)		2.3	2.0	12	
V _{GS(TH)}	Gate Threshold Voltage	2		4	V	$V_{DS}=V_{GS}$, $I_{D}=250\mu A$
g _{fs}	Forward Transconductance(NOTE *3)		3.5		S	V _{DS} =15V, I _D =2.5A

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
C _{iss}	Input Capacitance		560			\/ 0\/\/ 05\/
C _{oss}	Output Capacitance		50		pF	V_{GS} = 0V, V_{DS} = 25V f =1.0MHz
C _{rss}	Reverse Transfer Capacitance		2.2			
Q_g	Total Gate Charge		13			1 54 1/ 5201/
Q_{gs}	Gate-to-Source Charge		2.7		nC	$I_D=5A, V_{DD}=520V$ $V_{GS}=10V$
Q _{gd}	Gate-to-Drain ("Miller") Charge		5.5			v _{GS} = 10V

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
t _{d(ON)}	Turn-on Delay Time		14			
t _{rise}	Rise Time		22		no	V_{DD} =325V, I_{D} =5A,
t _{d(OFF)}	Turn-Off Delay Time		29		ns	$V_G=10V R_G=10\Omega$
t _{fall}	Fall Time		15			

Page 2 of 6



Source-Drain Diode Characteristics Tc=25℃ unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
	Continuous Source Current			5	Α	
Is	(Body Diode)			3	A	T _C =25℃
	Maximum Pulsed Current			20	А	
ISM	(Body Diode)					
V_{SD}	Diode Forward Voltage			1.5	V	I_{SD} =5A, V_{GS} =0V
t _{rr}	Reverse Recovery Time		250		ns	I _F = I _S
Q _{rr}	Reverse Recovery Charge		1200		nC	di/dt=100A/us

Notes:

- *1. $T_J = +25^{\circ}C$ to $+150^{\circ}C$.
- *2. Repetitive rating; pulse width limited by maximum junction temperature.
- *3. Pulse width < 380 μ s; duty cycle < 2%.



Test Circuits and Waveforms

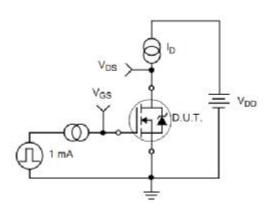


Figure 1. Gate Charge Test Circuit

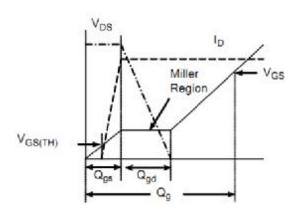


Figure 2. Gate Charge Waveforms

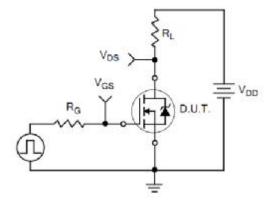


Figure 3. Resistive Switching Test Circuit

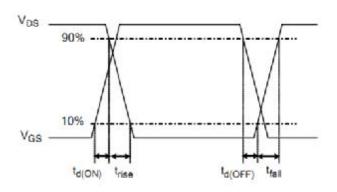
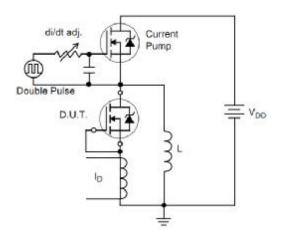


Figure 4. Resistive Switching Waveforms



Test Circuits and Waveforms



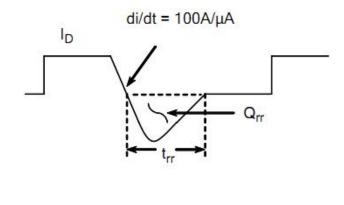


Figure 5. Diode Reverse Recovery Test Circuit

Figure 6. Diode Reverse Recovery Waveform

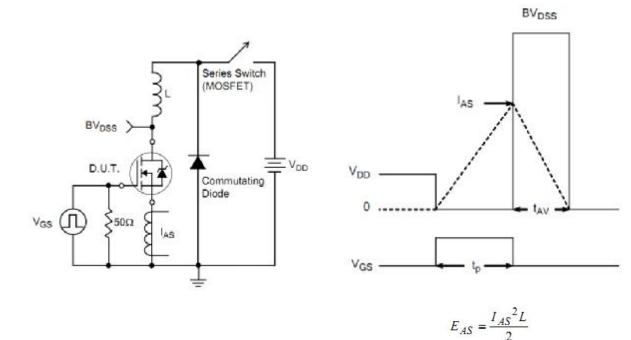


Figure 7. Unclamped Inductive Switching Test Circuit Figure 8. Unclamped Inductive Switching Waveform



Disclaimers:

InPower Semiconductor Co., Ltd (IPS) reserves the right to make changes without notice in order to improve reliability, function or design and to discontinue any product or service without notice. Customers should obtain the latest relevant information before orders and should verify that such information is current and complete. All products are sold subject to IPS's terms and conditions supplied at the time of order acknowledgement.

InPower Semiconductor Co., Ltd warrants performance of its hardware products to the specifications at the time of sale, Testing reliability and quality control are used to the extent IPS deems necessary to support this warrantee. Except where agreed upon by contractual agreement, testing of all parameters of each product is not necessarily performed.

InPower Semiconductor Co., Ltd does not assume any liability arising from the use of any product or circuit designs described herein. Customers are responsible for their products and applications using IPS's components. To minimize risk, customers must provide adequate design and operating safeguards.

InPower Semiconductor Co., Ltd does not warrant or convey any license either expressed or implied under its patent rights, nor the rights of others. Reproduction of information in IPS's data sheets or data books is permissible only if reproduction is without modification or alteration. Reproduction of this information with any alteration is an unfair and deceptive business practice. InPower Semiconductor Co., Ltd is not responsible or liable for such altered documentation.

Resale of IPS's products with statements different from or beyond the parameters stated by InPower Semiconductor Co., Ltd for that product or service voids all express or implied warrantees for the associated IPS's product or service and is unfair and deceptive business practice. InPower Semiconductor Co., Ltd is not responsible or liable for any such statements.

Life Support Policy:

InPower Semiconductor Co., Ltd's products are not authorized for use as critical components in life support devices or systems without the expressed written approval of InPower Semiconductor Co., Ltd.

As used herein:

- 1. Life support devices or systems are devices or systems which:
 - a. are intended for surgical implant into the human body,
 - b. support or sustain life,
 - c. whose failure to perform when properly used in accordance with instructions for used provided in the labeling, can be reasonably expected to result in significant injury to the user.
- A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.