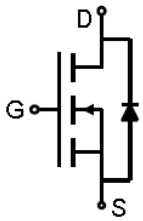
深圳市诚芯微科技有限公司
SHENZHEN CHENGXINWEI TECHNOLOGY CO., LTD.

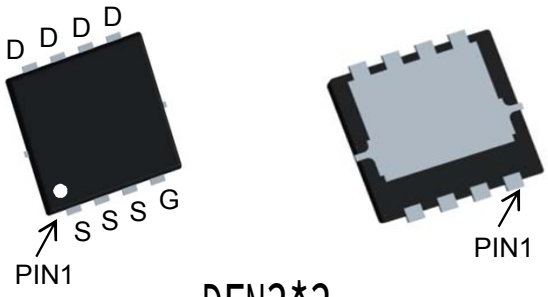
N-channel Enhancement Mode Mosfet CX4040

DESCRIPTION

The CX4040 uses advanced trench technology to provide excellent RDS(ON) and low gate charge. This device is suitable for use as a load switch or in PWM applications.



Schematic diagram



DFN3*3

GENERAL FEATURES

- RDS(ON) <5.5mΩ@VGS=10V
  RDS(ON) < 8mΩ @ VGS=4.5V
- High Power and current handing capability
- Lead free product is acquired
- Surface Mount Package

Application

- PWM applications
- Load switch
- Power management

■ **Absolute Maximum Ratings** (T_A=25℃unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	40	V
Gate-source Voltage		V_{GS}	±20	V
Drain Current	T_C=25℃	I_D	40	A
	T_C=100℃		25	
Pulsed Drain Current [A]		I_{DM}	160	A
Total Power Dissipation	T_C=25℃	P_D	27.8	W
	T_C=100℃		13	W
Single Pulse Avalanche Energy [B]		E_{AS}	42	mJ
Thermal Resistance Junction-to-Case [C]		$R_{\theta JC}$	3.75	℃/ W
Junction and Storage Temperature Range		T_J ,T_{STG}	-55～+150	℃

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ELECTRICAL CHARACTERISTICS (T_A=25℃unless otherwise noted)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Static Parameter							
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA		40			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=32V,V_{GS}=0V	T_J=25℃			1	μA
			T_J=55℃			5	
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V				±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA		1.0	1.5	2.5	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}= 10V, I_D=12A			5.5	8	mΩ
		V_{GS}= 4.5V, I_D=10A			8	11	
Diode Forward Voltage	V_{SD}	I_S=15A,V_{GS}=0V			0.85	1.2	V
Maximum Body-Diode Continuous Current	I_S					40	A
Dynamic Parameters							
Input Capacitance	C_{iss}	I_{SD}=40A, dI_{SD}/dt=100A/μs V_{DS}=20V,V_{GS}=0V,f=1MHZ			690		pF
Output Capacitance	C_{oss}				193		
Reverse Transfer Capacitance	C_{rss}				38		
Switching Parameters							
Total Gate Charge	Q_g	V_{GS}=10V,V_{DS}=32V,I_D=40A			5.8		nC
Gate-Source Charge	Q_{gs}				3		
Gate-Drain Charge	Q_{gd}				1.2		
Reverse Recovery Chrage	Q_{rr}	I_{SD}=40A, dI_{SD}/dt=100A/μs			15		
Reverse Recovery Time	t_{rr}				9		ns
Turn-on Delay Time	$t_{D(on)}$	V_{DD}=20V,I_{DS}=40A, V_{GEN}=10V,R_G=4.7Ω			5		
Turn-on Rise Time	t_r				24		
Turn-off Delay Time	$t_{D(off)}$				35		
Turn-off fall Time	t_f				12		

A. Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.

B. T_j=25℃, V_{DD}=20V, V_G=10V, L=0.5mH, R_g=25Ω

C. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

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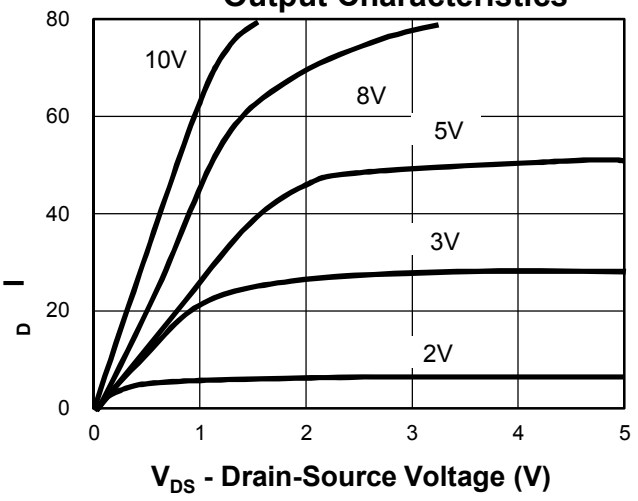
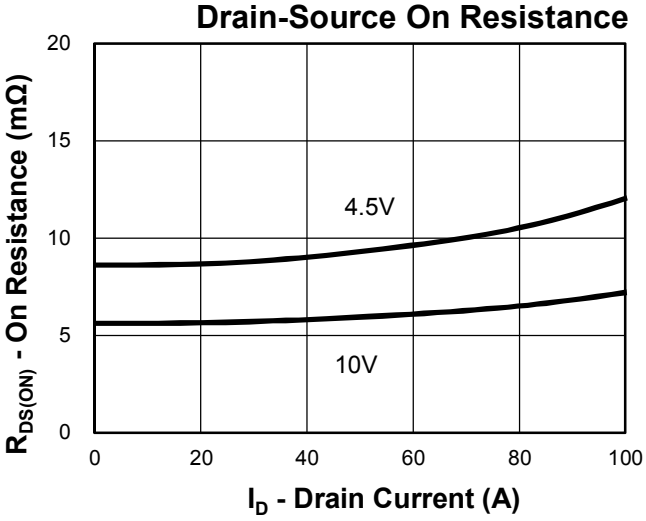
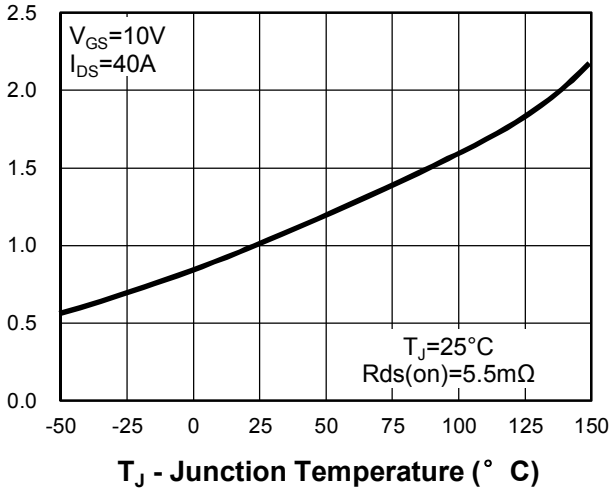
Output Characteristics



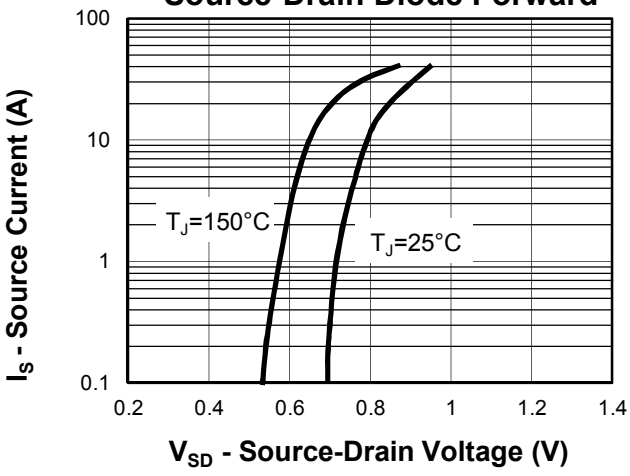
Drain-Source On Resistance



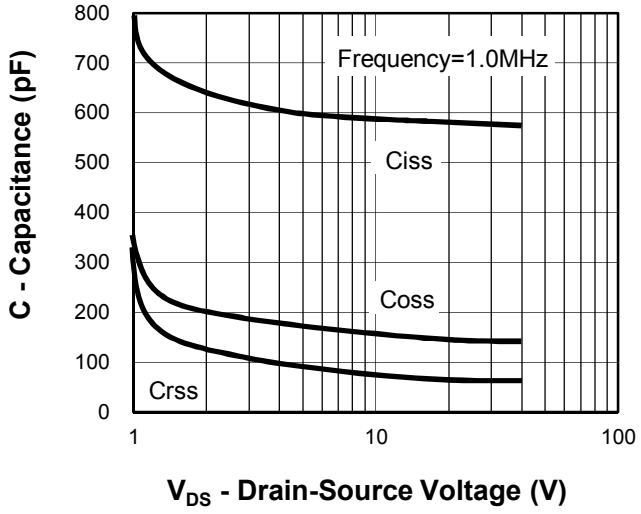
Drain-Source On Resistance



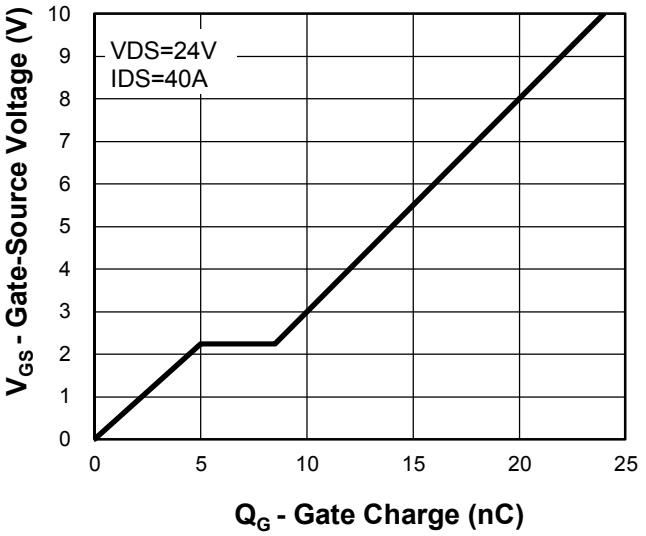
Source-Drain Diode Forward



Capacitance



Gate Charge



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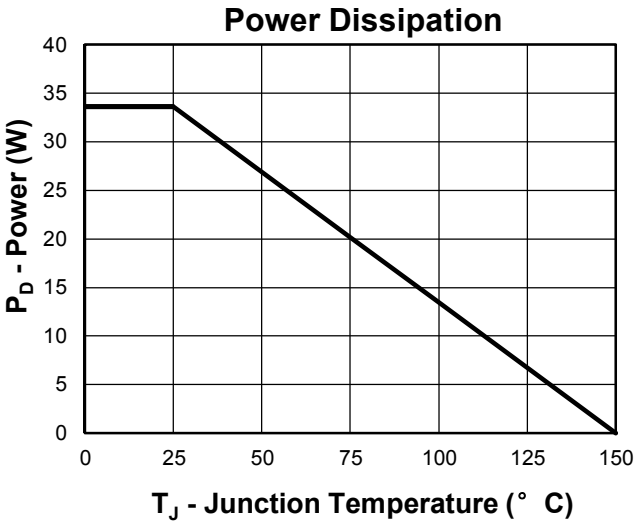
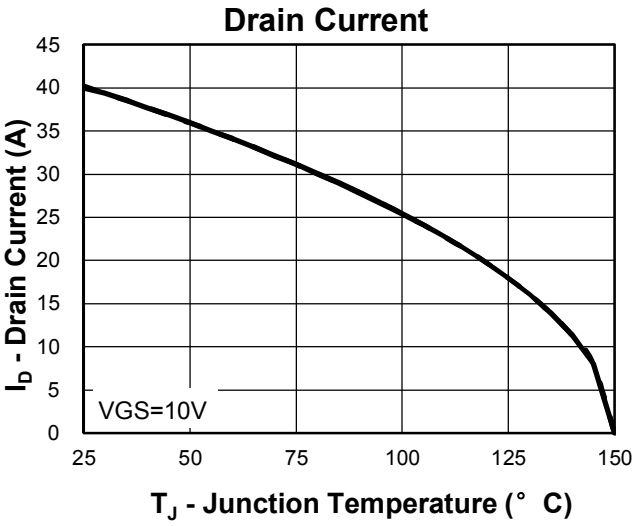
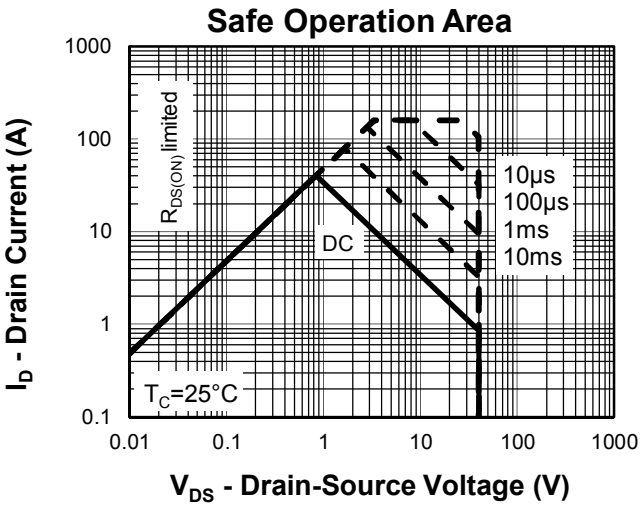
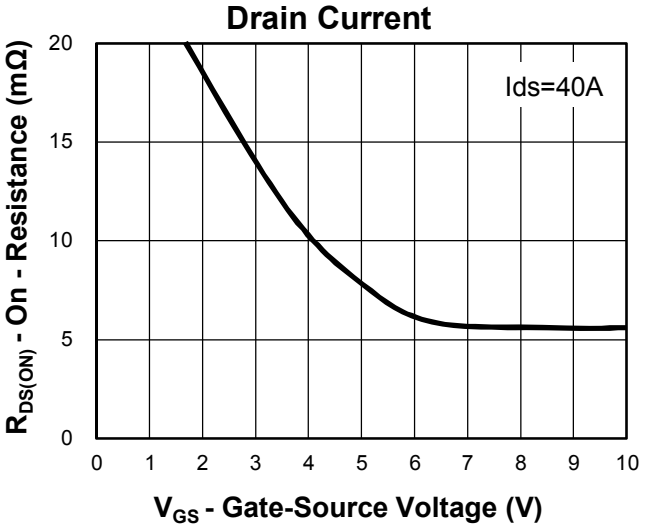
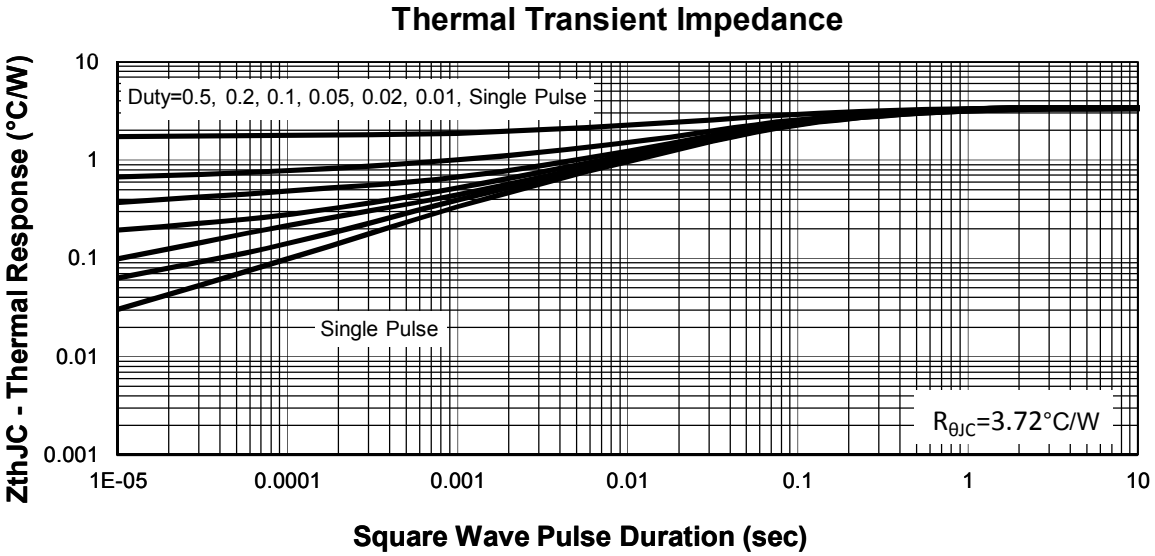


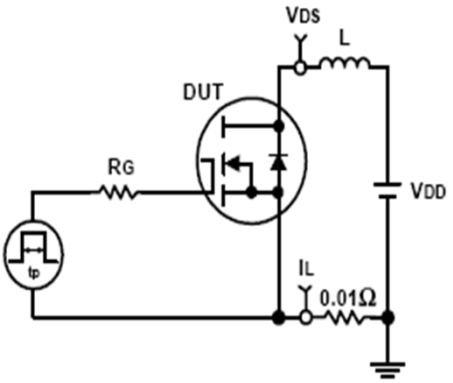


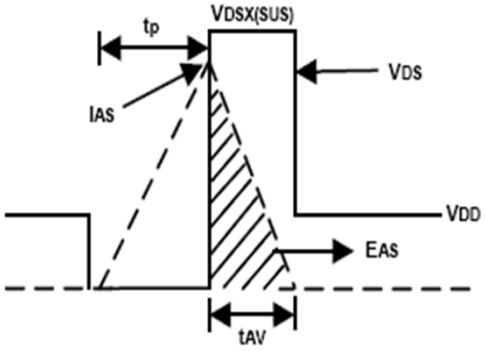




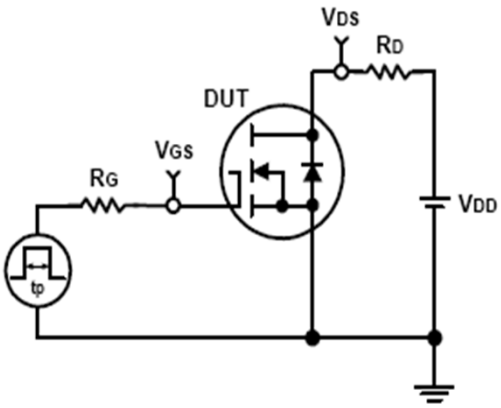


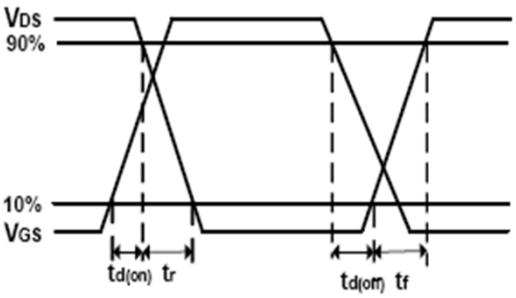
Avalanche Test Circuit and Waveforms





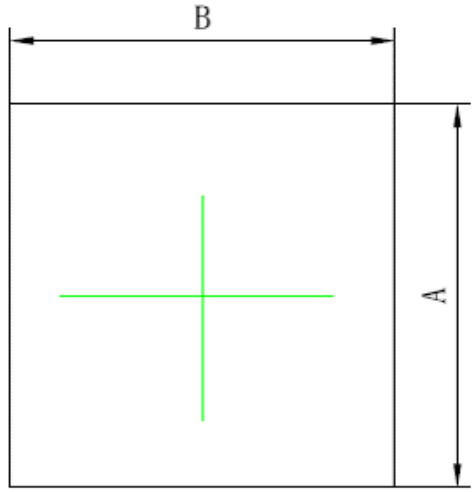
Switching Time Test Circuit and Waveforms

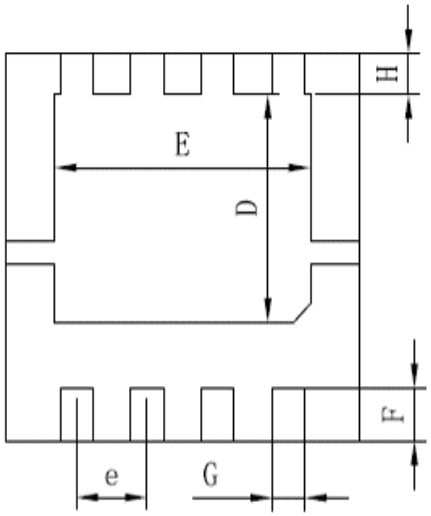




Package Information

■ **DFN3.3X3.3 Package information**





A	B	C	C1
3.25±0.05	3.25±0.05	0.8±0.05	0.2±0.02
C2	D	E	F
0.05Max	1.9±0.1	2.35±0.15	0.45±0.05
G	H	e	
0.3±0.05	0.35±0.05	0.65±0.05	
单位：mm