ETM61E-01

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Application Manual

Real Time Clock Module

RX8111CE

Product name	Product number
RX8111CE A	X1B000421000115
RX8111CE B	X1B000421000215

SEIKO EPSON CORPORATION

ETM61E Revision History

Rev No.	Date	Page	Description
01	29.Jan.2020		Release

INDEX

Low Power Real-time Clock Module with I²C Interface and Time Stamp Function

RX8111CE

- Built-in frequency adjusted 32.768 kHz crystal unit
- Interface Type : I²C (up to 400 kHz)
- Low current consumption at backup: 100 nA / 3.0 V Typ.
- Wide operating voltage range : 1.6 V to 5.5 V
- Wide time-keeper voltage range : 1.1 V to 5.5 V
- Auto power switching function : Automatically switches to backup power supply by monitoring the V_{DD} voltage.
- Time stamp function : 8times time-stamp,1/256 seconds with many selectable trigger.
- Time stamp memory can be used as users memory; 512 bit, 64 word × 8 bit
- Alarm interruption : Day, date, hour, minute, second
- The various functions include full calendar, seconds alarm, wakeup timer, and 32.768 kHz output
- Self monitoring function : Voltage detection, Crystal oscillation stop, etc.

The I²C-Bus is a trademark of NXP Semiconductors.

1. Overview

RX8111CE is a real-time clock module with integrated 32.768 kHz crystal oscillator and I²C interface. In addition to providing a calendar (year, month, date, day, hour, minute, second), this module provides other functions including time-stamp from 1/1024 second to year, alarm, wakeup timer, time update interruption, and 32.768 kHz output. Time stamp function can record maximum of 8 events. Using the backup battery charge control function and the interface power supply input pin, RX8111CE can support various power supply circuits. All of the functions mentioned above are offered in a thin and compact 3.2 x 2.5 ceramic package which could be used in various applications requiring small footprints.

2. Block Diagram

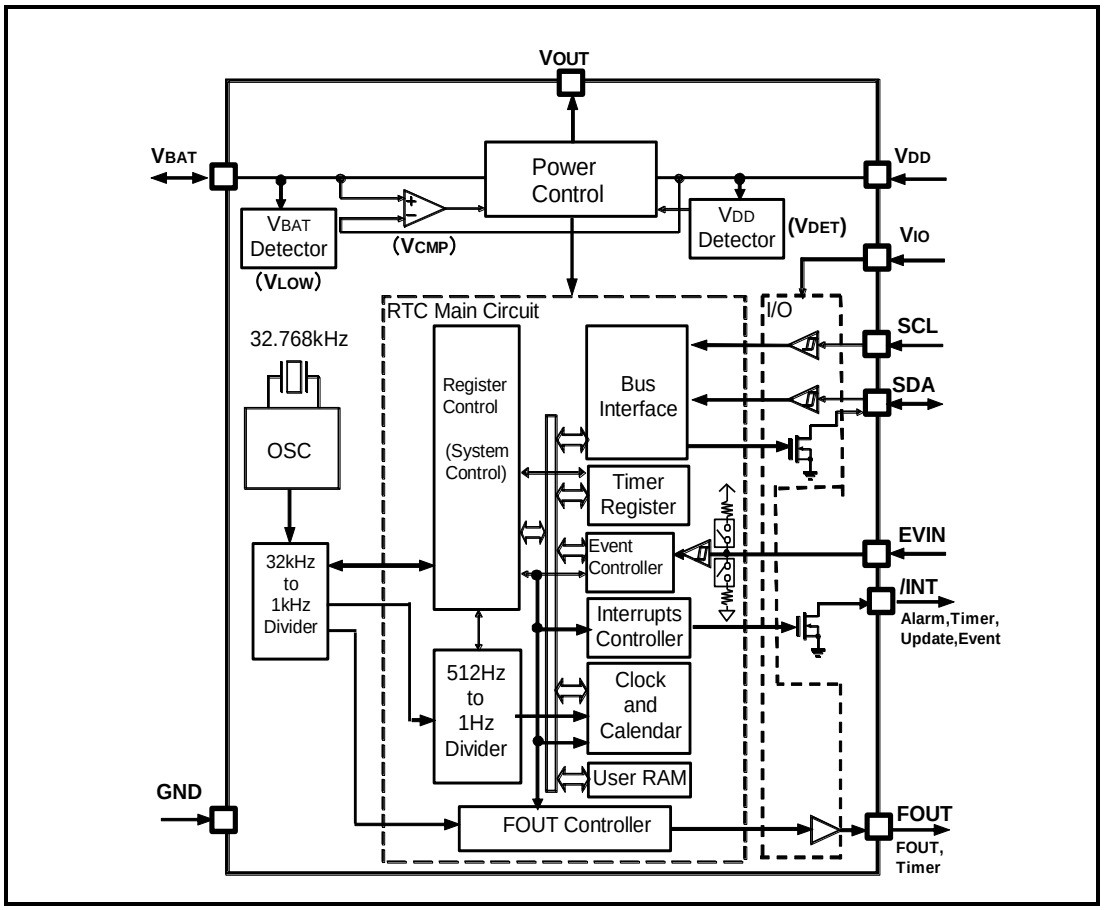


Figure 1 Block Diagram

3. Terminal Description

3.1. Terminal Connections

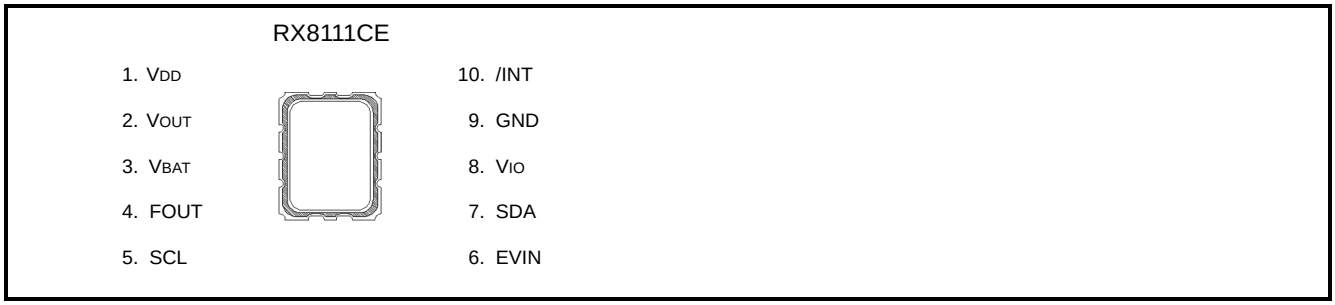


Figure 2 Package Pin layout

3.2. Pin Functions

Table 1 Pin Description

Signal name	I/O	Function
SCL	Input	Serial clock input pin.
SDA	Bi-directional	Data input and output pin.
EVIN	Input	Trigger input for Time stamp request. Built-in the programmable pull-up/down resister. Input detection is available in backup mode. The reference of the input level is V_{OUT} voltage. Note, there is not it with a V_{IO}. An input chattering filter rate is selectable. When not using EVIN, connect EVIN to V_{DD} or GND; don't leave EVIN pin floating.
FOUT	Output	Frequency output pin (CMOS) (frequency selection: 32.768 kHz, 1024 Hz, 1 Hz) When output is stopped, the FOUT pin is High impedance.
/INT	Open-Drain Output	This pin is used to output alarm signals, timer signals, time update signals, and other signals. This pin is an N-ch open drain
V_{DD}	–	Power-supply pin Possible to supply different voltage from V_{IO}
V_{IO}	–	Interface power supply pin Input to supply the voltage same as a host
V_{OUT}	–	Internal voltage output pin Connect bypass capacitor of 1.0 µF
V_{BAT}	–	This is a power supply pin for backup battery Connect an EDLC, a secondary battery, a primary battery In the backup voltage range, supplied to IC, from this pin
GND	–	Ground pin

Note: Be sure to connect a bypass capacitor rated at least 0.1 µF between V_{DD} and GND.
For the input terminal except EVIN, it is permitted for the input to be 5.5 V regardless of the V_{IO} voltage.
For the Open-Drain pin, it is permitted for the pull-up to be 5.5 V regardless of the V_{IO} voltage.

4. Connection Example

4.1. Battery Switchover connection Examples

Note. When connecting an outside power supply or a large-sized battery to V_{BAT}, install bypass capacitors more than 0.1 μF in a V_{BAT} terminal if necessary.
As for each of bypass-capacitor, Install nearest in each of pin as much as possible.

EX.1 V_{IO} and V_{DD} are different.

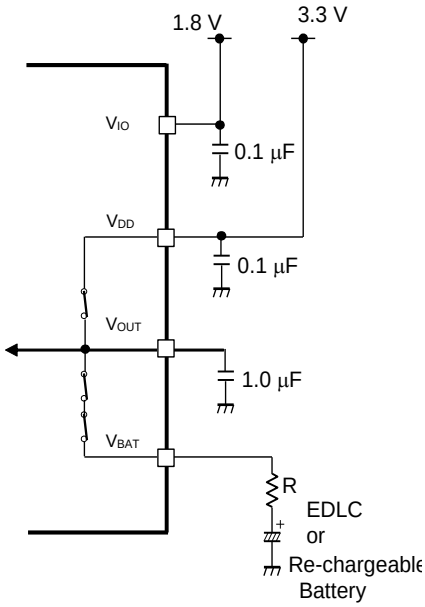


Figure 3 Connection example 1

Ex.2 V_{IO} and V_{DD} are the same.

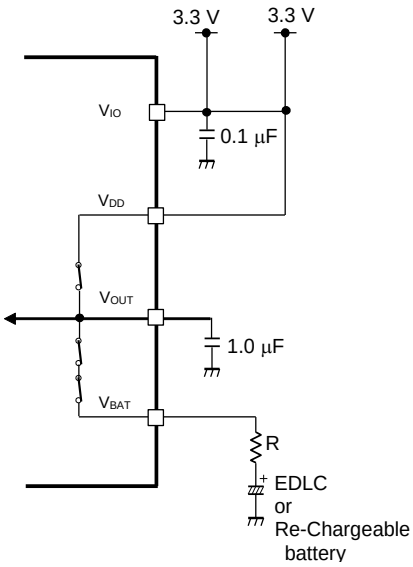


Figure 4 Connection example 2

Ex.3 Connecting a Non RE-Chargeable battery

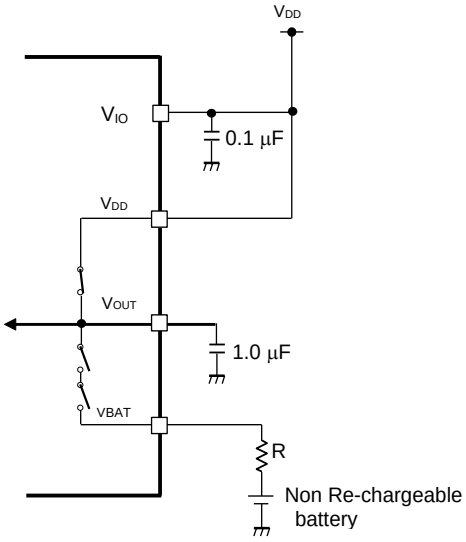
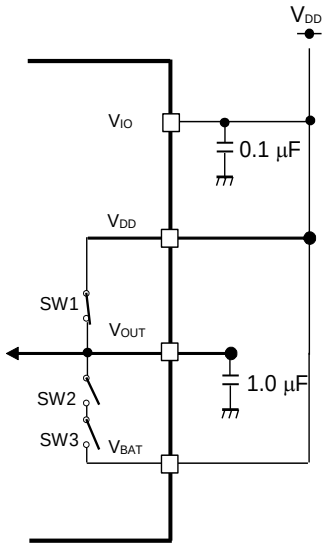


Figure 5 Connection example3

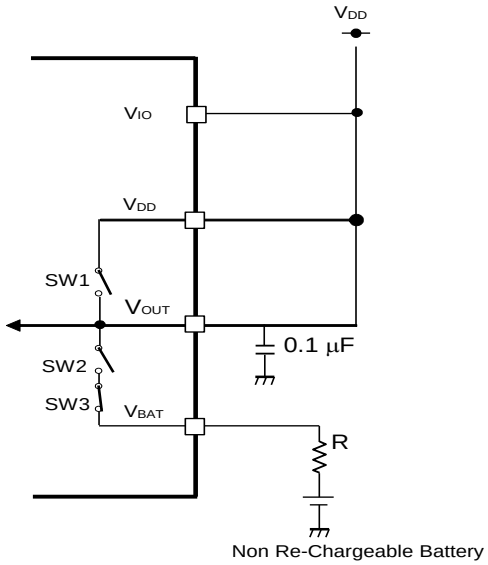
Ex.4 Not using power-switch function



INIEN = 0, CHGEN = 0, SWSEL1,0 = 10b

Figure 6 Connection Example 4

Ex.5 Connecting a Non Re-Chargeable battery



INIEN = 0, CHGEN = 0, SESEL1,0 = 01b

Figure 7 Connection example 5

5. External Dimensions / Marking Layout

5.1. External Dimensions

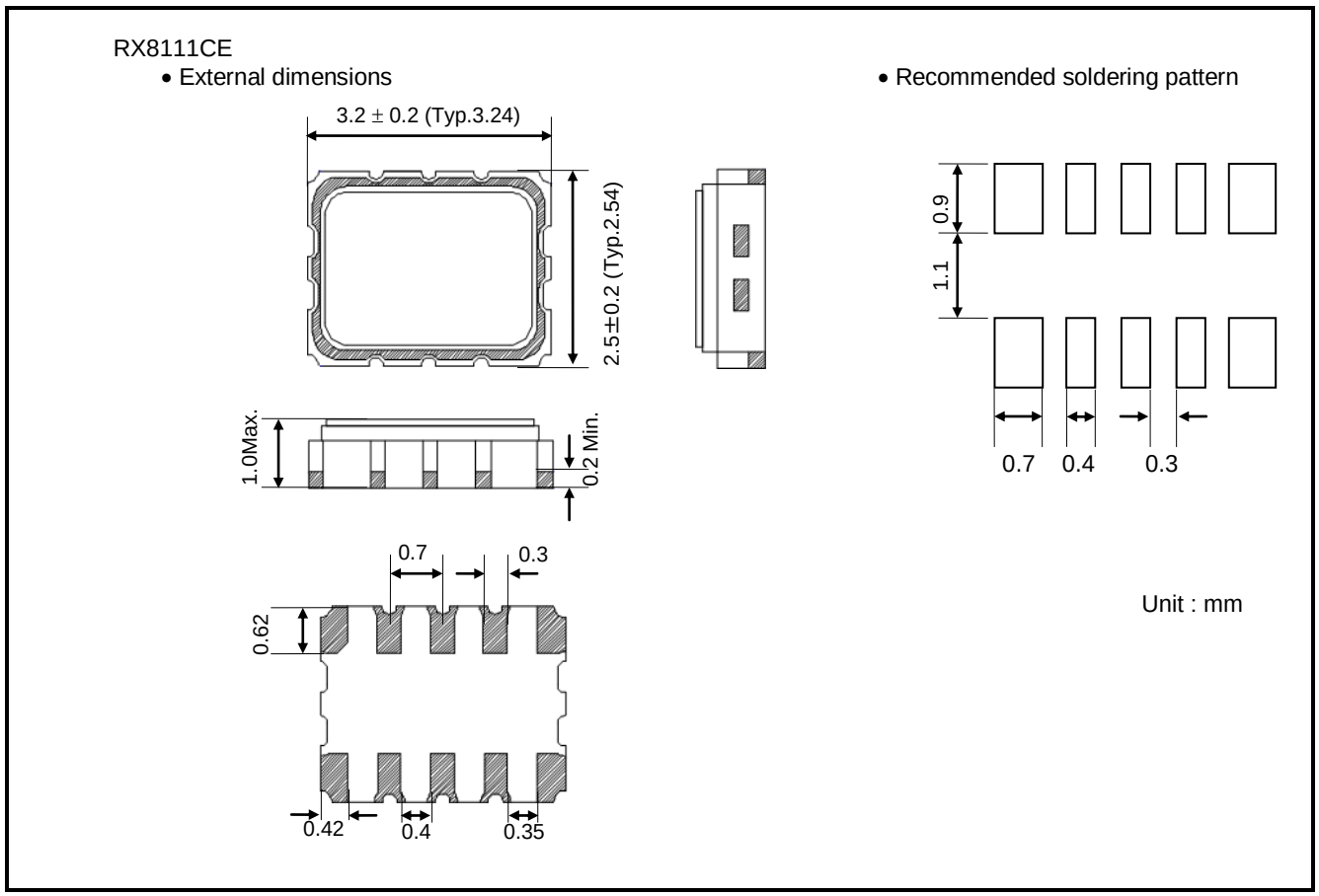
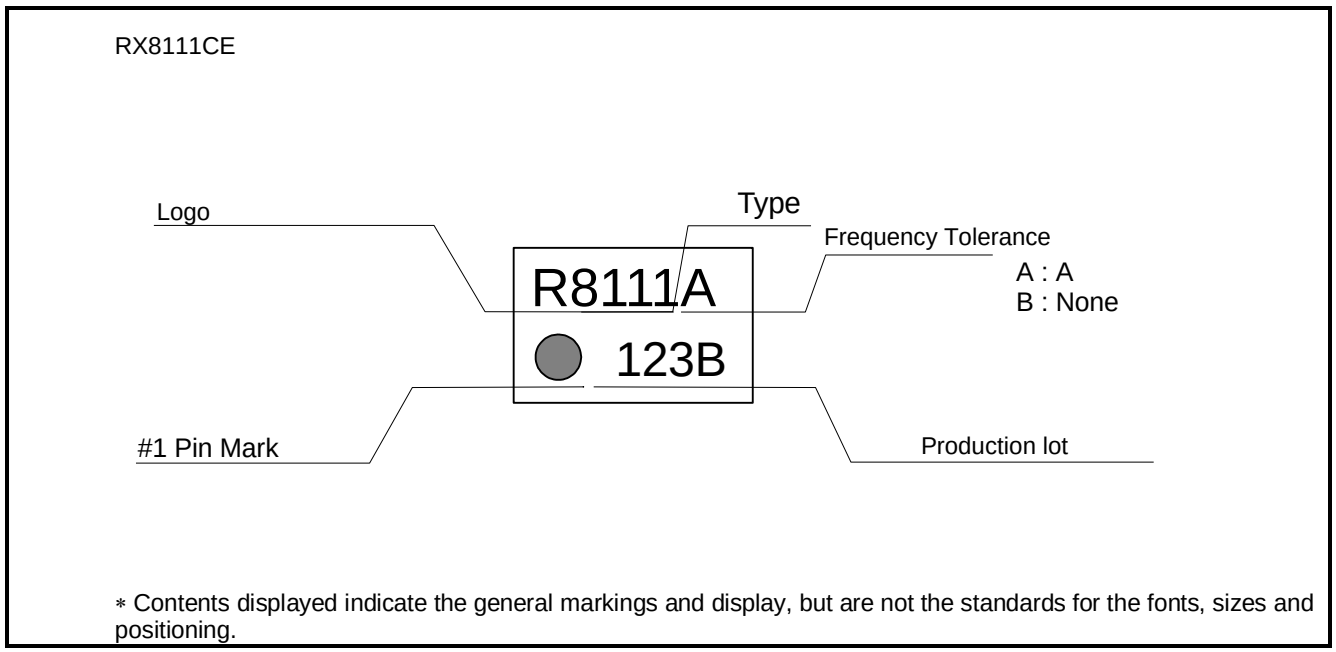


Figure 8 External dimensions

5.2. Marking Layout



∗ Contents displayed indicate the general markings and display, but are not the standards for the fonts, sizes and positioning.

Figure 9 Marking Layout

6. Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings

GND=0V

Item	Symbol	Condition	Rating	Unit
Operating supply Voltage	V_{DD}	–	–0.3 to +6.5	V
Operating supply Voltage	V_{OUT}	–	–0.3 to +6.5	V
Backup supply voltage	V_{BAT}	–	–0.3 to +6.5	V
Interface supply voltage	V_{IO}	–	–0.3 to +6.5	V
Input voltage 1	V_{IN1}	SCL, SDA	–0.3 to +6.5	V
Input voltage 2	V_{IN2}	EVIN	-0.3 to V_{OUT} + 0.3	V
Output voltage 1	V_{OUT1}	/INT, SDA	–0.3 to +6.5	V
Output voltage 2	V_{OUT2}	FOUT	-0.3 to V_{IO} + 0.3	V
Storage temperature	T_{STG}	When stored separately, without packaging	–55 to +125	°C

7. Recommended Operating Conditions

Table 3 Recommended Operating Conditions

Unless otherwise specified, $V_{BAT} = V_{DD} = V_{IO}$ = 1.6V ~ 5.5 V, Ta = -40 °C ~ +85 °C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating supply Voltage	V_{DD}	Supply from V_{DD}	1.25	3.0	5.5	V
Interface supply voltage	V_{IO}	V_{DD}=1.6 V ~ 5.5 V	1.6	3.0	5.5	V
Clock supply voltage	V_{CLK}	Supply from V_{BAT}	V_{VLF}	3.0	5.5	V
VLF detection voltage	V_{VLF}	V_{OUT} low detection Voltage	-	-	1.1	V
Operating temperature	Ta	No condensation	–40	+25	+85	°C

V_{CLK}: Min. is available by initializing in $V_{DD} \geq V_{DET1}$.
When first Power ON, for internal initializing, V_{DD} must be more than 1.45V: $+V_{DET1}$.

8. Frequency Characteristics

Table 4 Frequency Characteristics

Unless otherwise specified, $V_{BAT} = V_{DD} = V_{IO}$ = 1.6V ~ 5.5 V, Ta = -40 °C ~ +85 °C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation Frequency	fo			32.768		kHz
Frequency Tolerance	$\Delta f / f$	Ta = +25 °C V_{DD} = 3.0 V		A : ± 11.5 *1 B : ± 23.0 *2		$\times 10^{-6}$ $\times 10^{-6}$
Frequency/voltage characteristics	f/V	Ta = +25 °C V_{DD} = 1.1 V ~ 5.5 V	–2		+2	$\times 10^{-6}$ / V
Frequency/ Temperature characteristics	f_0-T_C	Ta = –20 °C ~ +70 °C V_{DD} = 3.0 V; +25 °C reference	–120		+10	$\times 10^{-6}$
Oscillation Start-up time	t_{STA}	V_{DD} = 1.6 V ~ 5.5 V			1.0	s
Aging	fa	Ta = +25 °C, V_{DD} = 3.0 V; First year	–5		+5	$\times 10^{-6}$ / year

*1 Equivalent to ±60 seconds per month deviation. *2 Equivalent to ±30 seconds per month deviation.

9. Electrical Characteristics

9.1. DC Characteristics

9.1.1.DC Characteristics 1

Table 5 DC Characteristics

Unless otherwise specified, V_{BAT} = V_{DD} = V_{IO} = 1.6 V ~ 5.5 V, Ta = -40 °C to +85 °C

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Current consumption 1	I_{DD}	SCL = SDA = High, FOUT = OFF, /INT = OFF V_{DD} = V_{OUT} = V_{BAT} = V_{IO} = 3.0 V -40 °C ~ +85 °C CHGEN = 0b, INIEN = 0b			100	450	nA
Current consumption 2	I_{32k}	SCL = SDA = High FOUT = 32.768 kHz, /INT = OFF V_{DD} = V_{IO} = 3.0 V, -40 °C ~ +85 °C FOUT pin CL = 15 pF CHGEN = 0b INIEN = 1b			2.0	3.0	µA
Current consumption 3	I_{BAT}	SCL = SDA = Low FOUT = OFF, /INT = OFF V_{BAT} = 3.0V V_{DD} = V_{IO} = 0.0			110	450	nA
Detection voltage of V_{DD} rise up	$+V_{DET1}$	Switch voltage of V_{DD} from V_{BAT}		1.25	1.35	1.45	V
Detection voltage of V_{DD} fall down	$-V_{DET1}$	Switch voltage of V_{BAT} from V_{DD}		1.20	1.30	1.40	V
Detection voltage of V_{BAT} low	V_{LOW}	V_{BAT} low detection voltage		1.10		1.30	V
V_{OUT} voltage 1	V_{VOUT1}	V_{DD} = 3.0V I_{OUT} = 1 mA			V_{DD}-0.06		V
V_{OUT} voltage 2	V_{VOUT2}	V_{BAT} = 3.0V I_{OUT} = 0.1 mA			V_{BAT}-0.02		V
High Input voltage	V_{IH}	SCL, SDA		0.8 × V_{IO}		5.5	V
		EVIN		0.8 × V_{OUT}		V_{OUT} + 0.3	V
Low Input voltage	V_{IL}	SCL, SDA		GND − 0.3		0.2 × V_{IO}	V
		EVIN		GND − 0.3		0.2 × V_{OUT}	
High Output voltage	V_{OH1}	FOUT	V_{IO} = 5.0 V, I_{OH} = -1 mA	4.5		5.0	V
	V_{OH2}		V_{IO} = 3.0 V, I_{OH} = -1 mA	2.2		3.0	
	V_{OH3}		V_{IO} = 3.0 V, I_{OH} = -100 µA	2.9		3.0	
Low output voltage	V_{OL1}	FOUT	V_{IO} = 5.0 V, I_{OL} = 1 mA	GND		GND+0.5	V
	V_{OL2}		V_{IO} = 3.0 V, I_{OL} = 1 mA	GND		GND+0.8	
	V_{OL3}		V_{IO} = 3.0 V, I_{OL} = 100 µA	GND		GND+0.1	
	V_{OL4}	/INT	V_{IO} = 5.0 V, I_{OL} = 1 mA	GND		GND+0.25	V
	V_{OL5}		V_{IO} = 3.0 V, I_{OL} = 1 mA	GND		GND+0.4	
	V_{OL6}	SDA	V_{IO} ≥ 2.0 V, I_{OL} = 3 mA	GND		GND+0.4	V
Input leakage current	I_{LK}	Input pin, V_{IN} = V_{IO} or GND		−0.5		0.5	µA
	IL_{KPD}	EVIN pin, V_{IN} = GND		−0.5		0.5	
Output leakage current	I_{OZ}	Output pin, V_{OUT} = V_{IO} or GND		−0.5		0.5	µA
V_{BAT} from V_{DD} Off leak current	I_{SW1}	V_{BAT} = 5.0 V, V_{DD} = 0.0 V				50	nA
V_{OUT} from V_{BAT} Off leak current	I_{SW2}	V_{BAT} = 5.0 V, V_{OUT} = 0.0 V				50	nA
V_{DD} from V_{BAT} Off leak current	I_{SW23}	V_{BAT} = 5.5 V, V_{OUT} = 3.3 V				50	nA
SW ON current of V_{OUT} from V_{DD}	I_{SWON1}	SW ON of V_{DD} and V_{OUT} ΔV = −0.1 V, V_{OUT} = 5.5 V, V_{DD} = 5.4 V ΔV = −0.1 V, V_{OUT} = 3.0 V, V_{DD} = 2.9 V R_{SWON1} = 20 Ω ~ 100 Ω		1	-	5	mA
SW ON current of V_{OUT} from V_{BAT}	I_{SWON2}	SW ON of V_{BAT} and V_{OUT} ΔV = −0.1 V, V_{OUT} = 5.5 V, V_{BAT} = 5.4 V ΔV = −0.1V, V_{OUT} = 3.0 V, V_{BAT} = 2.9 V R_{SWON1} = 33 Ω ~ 200 Ω		0.5	-	3	mA

9.1.2. Chargeable Current Characteristics

Chargeable current characteristics to Battery. It is ON resistance of SW1, 2, 3.
The reference value of +25 °C Typ. samples.
Y axis = Charge current Ichg, X axis = Vdef = (V_{DD} – V_{BAT}).

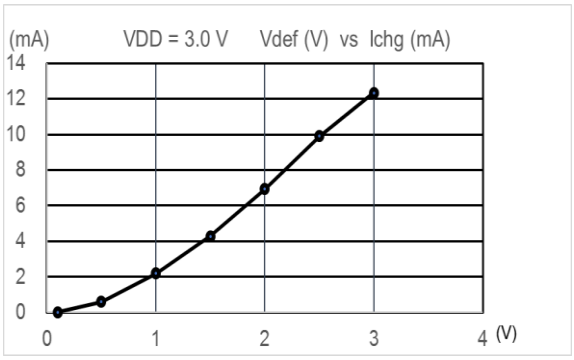


Figure 10 Chargeable current characteristics of V_{BAT} V_{DD} = 3.0 V

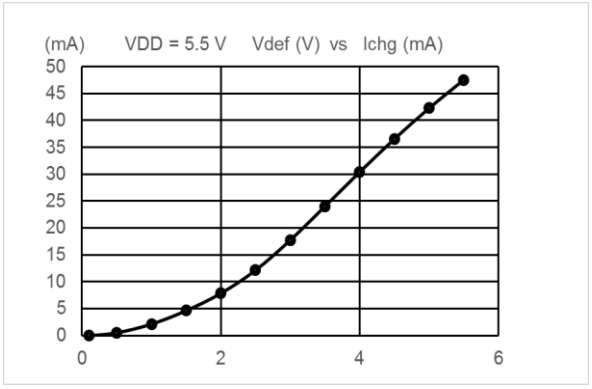


Figure 11 Chargeable current characteristics of V_{BAT} V_{DD} = 5.5V

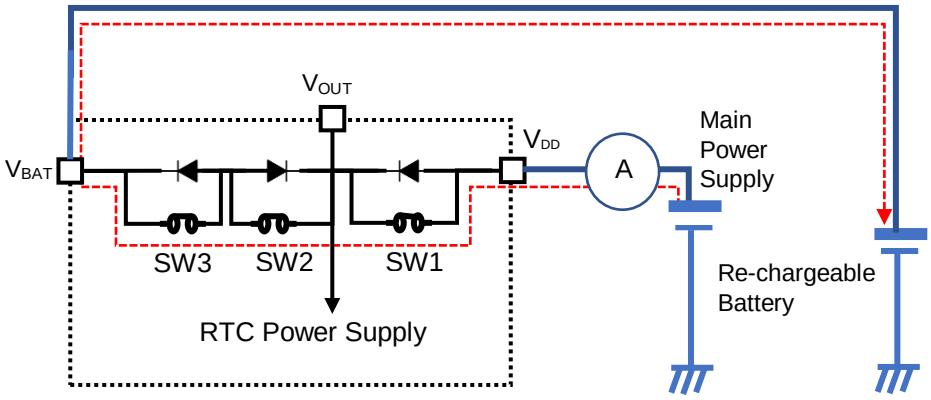


Figure 12 Circuit of charge to re-chargeable Battery.

9.1.3.Reference Value Of Switching Element.

Table 6 Reference value of switching element

Item	Characteristics	Condition
Current tolerance	40 mA Max.	SW1 = SW2 = SW3 = ON, +25 °C
Diode Vf	0.60 V / 1 mA Typ. 0.85 V / 10 mA Typ.	V_{DD} = 3.0 V, +25 °C
Diode IR	50 nA Max.	VR = 5.5 V, -40 °C to +85 °C

Charge current from V_{BAT} must be use less than 40 mA.

9.2. AC Characteristics

9.2.1. AC Characteristics 1

Table 7 AC Characteristics

Unless otherwise specified, 、GND = 0V, V_{IO} = 1.6 V to 5.5 V, Ta = -40 °C to +85 °C

Item	Symbol	SCL = 100 kHz (Standard-Mode)		SCL = 400 kHz (Fast-Mode)		Unit
		Min.	Max.	Min.	Max.	
SCL clock frequency	fSCL		100		400	kHz
Start condition setup time	tSU;STA	4.7		0.6		µs
Start condition hold time	tHD;STA	4.0		0.6		µs
Data setup time	tSU;DAT	250		100		ns
Data hold time	tHD;DAT	0		0		ns
Stop condition setup time	tSU;STO	4.0		0.6		µs
Bus idle time between start condition and stop condition	tBUF	4.7		1.3		µs
Time when SCL = "L"	tLOW	4.7		1.3		µs
Time when SCL = "H"	tHIGH	4.0		0.6		µs
Rise time for SCL and SDA	tr		1.0		0.3	µs
Fall time for SCL and SDA	tf		0.3		0.3	µs
Allowable spike time on bus	tSP		50		50	ns

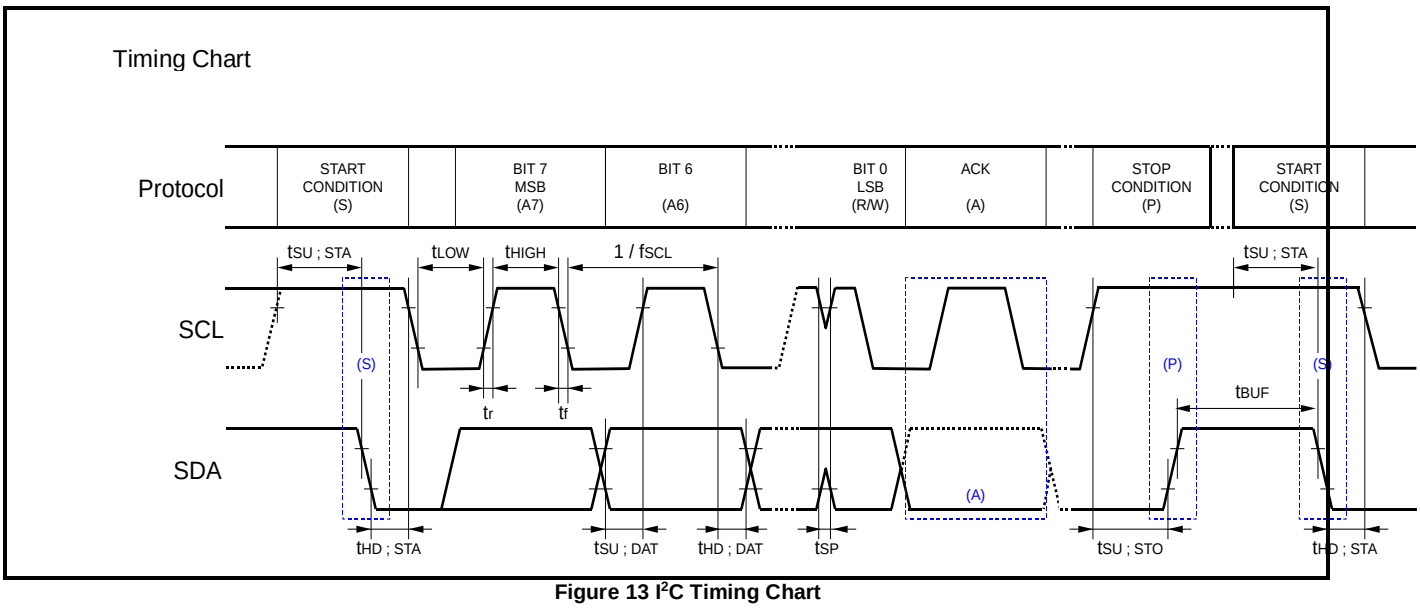


Figure 13 I²C Timing Chart

I²C interface is reset 2 seconds after slave address is received.
To restart serial communication, send START Condition again.
8bit data is latched at rising edge of SCL of ACK.
If communication is cancelled halfway of sending the 8bit, data is not written.

9.2.2. AC Characteristics 2

Table 8 FOUT duty

Unless otherwise specified, GND = 0 V, V_{IO} = 1.6 V ~ 5.5 V, Ta = –40 °C ~ +85 °C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
FOUT duty	Tw / t	Vth = 50% V_{IO}	40		60	%

10. Power Supply Sequence

10.1. Power Supply Sequence

This circuit is sensitive to power supply noise and supply voltage should be stabilized to avoid negative impact on the accuracy.
tR1 is needed for a proper power-on reset. If this power-on condition cannot be kept, it is necessary to send an initialization routine to the RTC by software.
In case of repeated ON/OFF of the power supply within short term, it is possible that the power-on reset will become unstable.
After power OFF, keep V_{DD} = V_{BAT} = GND for more than 10 seconds for a proper power-on reset.
When it is unstable, please initialize the RTC by the software.
Power-on-reset occurs on rising edge of V_{OUT} voltage.
Note: During first Power ON for internal initialization, V_{DD} must be over 1.45 V: $+V_{DET1}$.

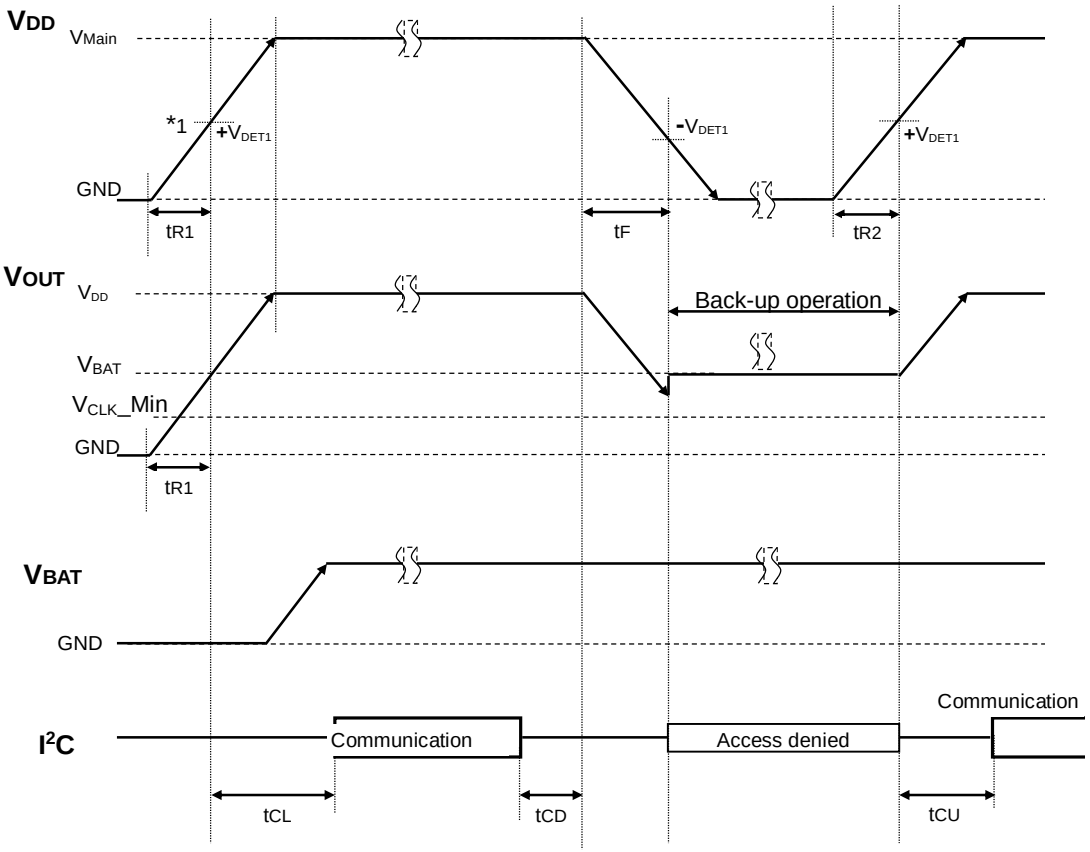


Figure 14 Power on Sequence

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Power supply rise time1	tR1	V_{OUT} rise time by V_{DD} or V_{BAT}.	3 V	0.1	-	10	ms / V
			5 V	0.5	-	10	ms / V
Access wait time. After initial power on.	tCL	After V_{DD} reach to $+V_{DET1}$		30	-	-	ms
Access disable hold time	tCD	After I^2C communication.		0	-	-	ms
Power supply fall time	tF	Time of $-V_{DET1}$ from, V_{DD} max.		1	-	-	ms / V
Power supply rise time2	tR2	V_{DD} reach to $+V_{DET1}$ From GND.		0.1	-	-	ms / V
Access wait time (Normal power on)	tCU	Waiting time before starting I^2C from Power-ON.		40	-	-	ms

Table 9 Power up down characteristics

10.2. The behavior and operation restriction at power-ON in RTC

Because most of the RTC registers are synchronized with the oscillation clock of the built-in crystal oscillator, the RTC does not work normally without the integrated oscillator stabilized. Please initialize the RTC at the time the power supply voltage returns (VLF = 1) after the oscillation is stabilized (after oscillation start time t_{STA}).
If intending to access the RTC after the main supply voltage returns, please note the following points:
1) Please begin to read VLFbit first.
2) When VLF returns "1", please initialize all registers. Please perform initial setting only t_{STA} (Oscillation start time), when the built-in oscillation is stable.
3) Access is prohibited within 40 ms the supply voltage exceeds min. V_{CLK} (Clock supply voltage (V_{DD} > 1.6 V)).

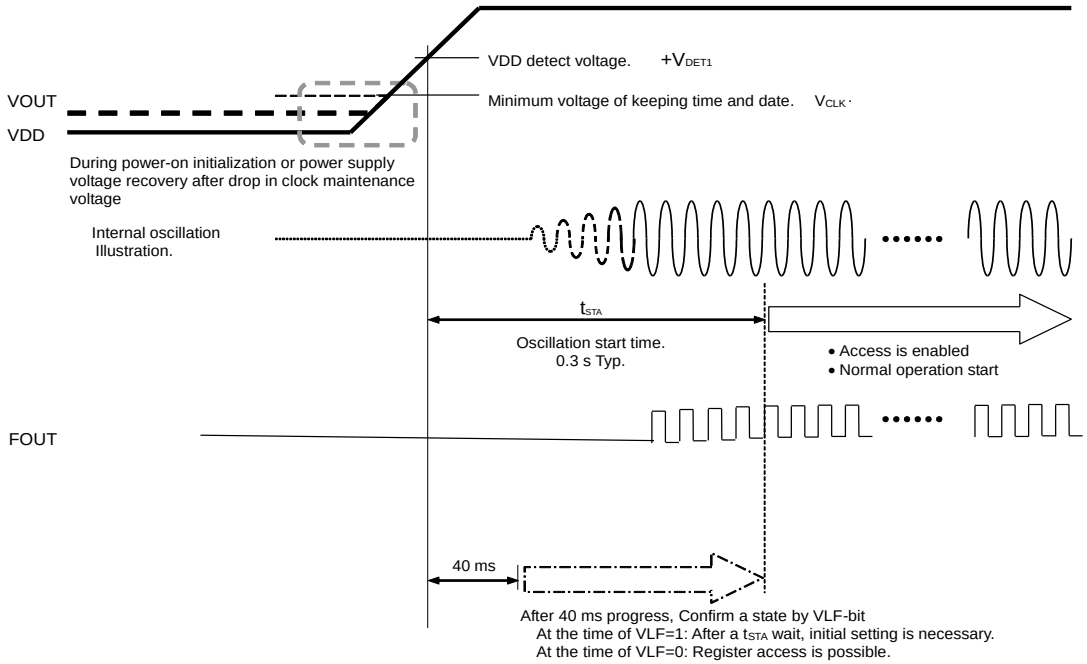


Figure 15 Oscillation start time chart (Power initial supply)

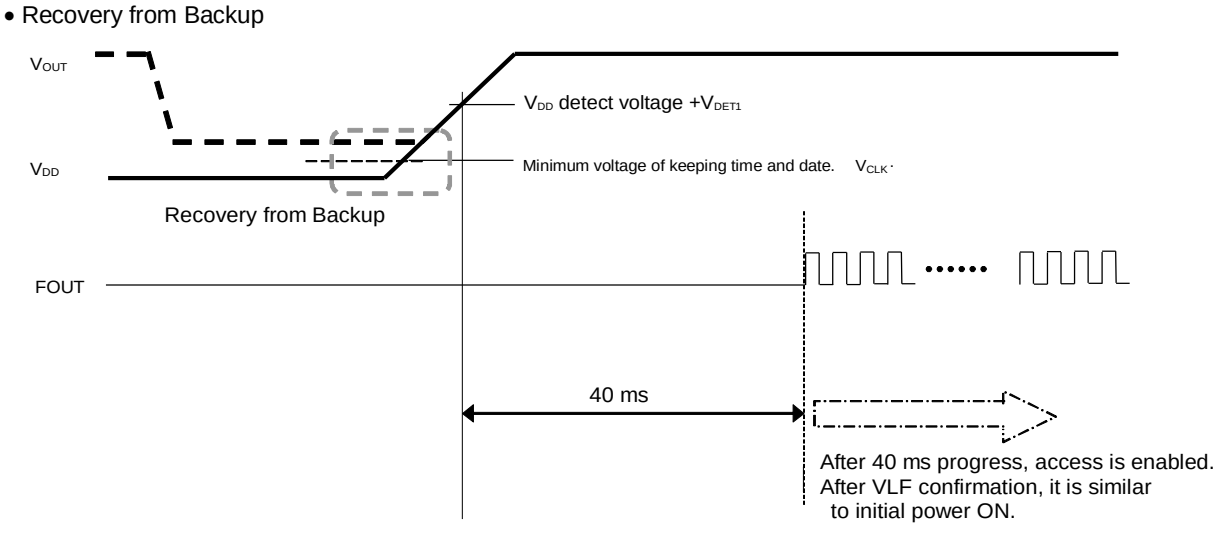


Figure 16 Oscillation start time chart (Backup resume)

10.3. Reset By Software

Software sequence for generating Power-on-reset

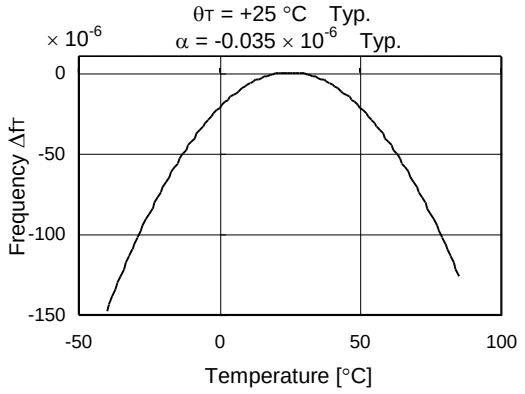
1) Power ON
2) Wait longer than 40 ms *1
3) Dummy reading *2
4) Readout VLF bit-1
5) Write 00h Address: Reg=32h *3 INIEN = 0b
6) Write 80h Address: Reg=3Fh TEST = 1
7) Write 6Ch Address: Reg=D0h
8) Write 03h Address: Reg=D1h
9) Write 10h Address: Reg=D2h
10) Write 20h Address: Reg=D3h
11) Wait more than 2 ms. released automatically *4

*1 When 40ms waiting time is so long time in your system, an another method.
Jump to step3 from step1.
At step4, when VLF is 1, write 0 to VLF. While VLF is 1, repeat reset to VLF and verify VLF is 0.
If VLF is cleared to 0, jump to step5. In this method, it have possibility this sequence is short than 40 ms.
After 40 ms, when VLF doesn't reset to 0, go to step5.
*2 Dummy reading. Any address is acceptable. In I^2C communication, ignore ACK / NACK signal from RX8111CE.
*3 Should be execute this command even if VLF is 0. Even if VLF is 1, it available after step5.
*4 2ms is time for RESET processing.
Note: Except using this RESET sequence, don't access to D0h from D3h, and never write 1 to a TEST- bit.

11. Reference information

11.1. Reference Data

(1) Example of frequency and temperature characteristics



[Finding the frequency stability]

1. Frequency and temperature characteristics can be approximated using the following equations.

$\Delta f_T = \alpha (\theta_T - \theta_X)^2$

- Δf_T : Frequency deviation in any temperature
- α [1 / °C^2] : Coefficient of secondary temperature (-0.035 ± 0.005) $\times 10^{-6}$ / °C^2
- θ_T [°C] : Ultimate temperature ($+25 \pm 5$ °C)
- θ_X [°C] : Any temperature

2. To determine overall clock accuracy, add the frequency precision and voltage characteristics.

$\Delta f/f = \Delta f/fo + \Delta f_T + \Delta f_V$

- $\Delta f/f$: Clock accuracy (stable frequency) in any temperature and voltage.
- $\Delta f/fo$: Frequency tolerance
- Δf_T : Frequency deviation in any temperature.
- Δf_V : Frequency deviation in any voltage.

3. How to find the date difference

Date Difference = $\Delta f/f \times$ 86400 seconds.

∗ For example: $\Delta f/f = 11.574 \times 10^{-6}$ is an error of approximately 1 second/day.

Figure 17 Frequency vs Temperature characteristics

12. Application Notes

1) Notes on handling

This module uses a C-MOS IC to realize low power consumption. Carefully note the following cautions when handling.

(1) Static electricity

While this module has built-in circuitry designed to protect it against electrostatic discharge, the chip could still be damaged by a large discharge of static electricity. Containers used for packing and transport should be constructed of conductive materials. In addition, only soldering irons, measurement circuits, and other such devices which do not leak high voltage should be used with this module, which should also be grounded when such devices are being used.

(2) Noise

If a signal with excessive external noise is applied to the power supply or input pins, the device may malfunction or "latch up." In order to ensure stable operation, connect a filter capacitor (preferably ceramic) of greater that 0.1 μF as close as possible to the power supply pins. Also, avoid placing any device that generates high level of electronic noise near this module.

(3) Voltage levels of input pins

When the voltage of out of the input voltage specifications range input into an input terminal constantly, a penetration electric current occurs. Thus, current consumption increases very much. This causes Latch-up, and there is the case that, as a result, a built-in IC is destroyed. Please use an input terminal according to input voltage specifications.
Furthermore, please input the V_{DD} or GND most recent voltage as much as possible.

(4) Handling of unused pins

Disposal of unused input terminals. When an input terminal is open state, it causes increase of a consumption electric current and the behavior that are instability. Please fix an unused input terminal to the voltage that is near to V_{DD} or GND.

2) Notes on packaging

(1) Soldering heat resistance.

If the temperature within the package exceeds +260 °C, the characteristics of the crystal oscillator will be degraded and it may be damaged. The reflow conditions within our reflow profile is recommended. Therefore, always check the mounting temperature and time before mounting this device. Also, check again if the mounting conditions are later changed.

(2) Mounting equipment

While this module can be used with general-purpose mounting equipment, the internal crystal oscillator may be damaged in some circumstances, depending on the equipment and conditions. Therefore, be sure to check this. In addition, if the mounting conditions are later changed, the same check should be performed again.

(3) Ultrasonic cleaning

Depending on the usage conditions, there is a possibility that the crystal oscillator will be damaged by resonance during ultrasonic cleaning. Since the conditions under which ultrasonic cleaning is carried out (the type of cleaner, power level, time, state of the inside of the cleaning vessel, etc.) vary widely, this device is not warranted against damage during ultrasonic cleaning.

(4) Mounting orientation

This device can be damaged if it is mounted in the wrong orientation. Always confirm the orientation of the device before mounting.

13. Overview of Functions and Description Of Registers

Note. The initialization of registers is necessary about the unused function too.

13.1. Overview Of Functions

1) Clock Function

This function is used to set and read out second, minute, hour, day, month, year (to the last two digits), and date data.
Any (two-digit) year that is a multiple of 4 is treated as a leap year and calculated automatically as such until the year 2099. Also "60" sec writing is available for leap second.
At the start of a I^2C communication, the time and clock counting stops (which causes loss of time), and clock starts automatically again at the end of the I^2C communication.

2) Wake-up Timer Interrupt Function

The wake-up timer interrupt function generates an interrupt event periodically at any fixed cycle set between 244.14 μs and 32 years. When an interrupt event is generated, the /INT pin goes to low level (Low) and "1" is set to the TF bit to report that an event has occurred.
The timer data can be read even timer is running. The timer operates in both timer pause and running, so this function realizes a cumulative timer, wake-up timer etc.

3) Alarm Interrupt Function

The alarm interrupt function generates interrupt events for alarm settings such as date, day, hour, and minute settings. When an interrupt event occurs, the AF bit value is set to "1" and the /INT pin goes to low level to indicate that an event has occurred.

4) Lower Operation Voltage Detection Function (VLF)

Lower voltage of V_{OUT} terminal can be detected
During power on initialization or recovery of backup this function judges the clock data reliability.
If lower voltage is detected power on reset function moves this RTC device to initial condition.

5) Lower Battery Backup Voltage Detection Function (VLOW)

Lower voltage of V_{BAT} terminal can be detected

6) Crystal Oscillation Stop Detection Function (XST)

RTC inner crystal oscillation stop can be detected.

7) Clock Output Function (FOUT)

Either 32.768 kHz,1024 Hz or 1 Hz clock is available at FOUT terminal.
Wake-up timer interrupt function available if FOUT function is not used.

8) Time Stamp Function

The function can be used, for example, to record the time of system software updates, battery replacements, and system alerts.
Time-stamps are stored even when power is switched over to the alternative battery source, contributing to system robustness.
8 times stamped from year to 1/256 seconds.
The time stamp trigger inputs from EVIN pin, self-monitoring and I^2C software command.

9) User RAM

Built-in 8bit × 64word (512bit) RAM for general purpose memory or Time Stamp memory.
It selectable for user's RAM or Time Stamp memory.

13.2. Register Table

13.2.1. Register Table

Table 9 Register Table (1)

Address Hex	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
10	SEC	**z**	40	20	10	8	4	2	1
11	MIN	**z**	40	20	10	8	4	2	1
12	HOUR	**z**	**z**	20	10	8	4	2	1
13	WEEK	**z**	6	5	4	3	2	1	0
14	DAY	**z**	**z**	20	10	8	4	2	1
15	MONTH	**z**	**z**	**z**	10	8	4	2	1
16	YEAR	80	40	20	10	8	4	2	1
17	MIN Alarm	AE	40	20	10	8	4	2	1
18	HOUR Alarm	AE	•	20	10	8	4	2	1
19	WEEK Alarm	AE	6	5	4	3	2	1	0
	DAY Alarm		•	20	10	8	4	2	1
1A	Timer Counter 0	128	64	32	16	8	4	2	1
1B	Timer Counter 1	32768	16384	8192	4096	2048	1024	512	256
1C	Timer Counter 2	8388608	4194304	2097152	1048576	524288	262144	131072	65536
1D	Extension Register	FSEL1	FSEL0	USEL	TE	WADA	ETS	TSEL1	TSEL0
1E	Flag Register	POR	**z**	UF	TF	AF	EVF	VLF	XST
1F	Control Register	**z**	**z**	UIE	TIE	AIE	EIE	**z**	STOP

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
20h	Time Stamp 1/1024S	--	--	--	--	--	--	1/512	1/1024
21h	Time Stamp 1/256S	1/2	1/24	1/8	1/16	1/32	1/64	1/128	1/256
22h	Time Stamp SEC	**z**	40	20	10	8	4	2	1
23h	Time Stamp MIN	**z**	40	20	10	8	4	2	1
24h	Time Stamp HOUR	**z**	**z**	20	10	8	4	2	1
25h	Time Stamp WEEK	**z**	6	5	4	3	2	1	0
26h	Time Stamp DAY	**z**	**z**	20	10	8	4	2	1
27h	Time Stamp MONTH	**z**	**z**	**z**	10	8	4	2	1
28h	Time Stamp YEAR	80	40	20	10	8	4	2	1
29h	Status Stamp	**z**	**z**	VLOW	VCMP	VDET	**z**	XST	**z**
2Ah	No Function	**z**	**z**	**z**	**z**	**z**	**z**	**z**	**z**
2Bh	EVIN Setting	EHL	ET1	ET0	PDN	PU1	PU0	OVW	-
2Ch	SEC Alarm	AE	40	20	10	8	4	2	1
2Dh	Timer Control	**z**	**z**	**z**	**z**	TBKON	TBKE	TMPIN	TSTP
2Eh	Time Stamp control 0	**z**	**z**	**z**	**z**	**z**	**z**	**z**	COMTG
2Fh	Command Trigger	**z**	**z**	**z**	**z**	**z**	**z**	**z**	**z**

After the initial power-up (from 0 V) or in case the VLF bit returns "1" , make sure to initialize all registers, before using the RTC.
Be sure to avoid entering incorrect date and time data, as clock operations are not guaranteed when the data or time data is incorrect.
Any bit marked with "**z**" should be used with a value of "0" after initialization. (Not writable)
Any bit marked with "•" is a RAM bit that can be used to read or write any data.
Any bit marked with' -- 'is Not writable. Read result is unkown.
The above table shows only the user registers. Due to functional reasons, RTC has different registers not mentioned above table which are programmed by the manufactorer. Please make sure to only access above mentioned user registers.
By read/write to register of No-Function, other finction are not affected.

Table 10 Register Table (2)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
30h	No Function	**z**	**z**	**z**	**z**	**z**	**z**	**z**	**z**
31h	No Function	**z**	**z**	**z**	**z**	**z**	**z**	**z**	**z**
32h	Power Switch Control	CHGEN	INIEN	**z**	**z**	SWSEL1	SWSEL0	SMPT1	SMPT0
33h	Status Monitor	**z**	EVIN	**z**	**z**	VCMP	**z**	VLOW	**z**
34h	Time Stamp Control 1	**z**	**z**	**z**	**z**	**z**	EISEL	TSCLR	TSRAM
35h	Time Stamp Control 2	●	**z**	**z**	**z**	ECMP	EVDET	EVLOW	EXST
36h	Time Stamp Control 3	**z**	**z**	**z**	TSFULL	TSEMP	TSAD2	TSAD1	TSAD0
37h	No Function	**z**	**z**	**z**	●	**z**	**z**	**z**	●
38h - 3Dh	No Function	**z**	**z**	**z**	**z**	**z**	**z**	**z**	**z**
3Eh	No Function	-	-	-	-	-	-	-	-
3Fh	TEST	TEST	**z**	**z**	**z**	**z**	**z**	**z**	**z**

Address Hex	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
40,50,60,70	Time stamp 1/256 s	1/2	1/4	1/8	1/16	1/32	1/64	1/128	1/256
41,51,61,71	Time Stamp SEC	●	40	20	10	8	4	2	1
42,52,62,72	Time Stamp MIN	●	40	20	10	8	4	2	1
43,53,63,73	Time Stamp HOUR	●	●	20	10	8	4	2	1
44,54,64,74	Time Stamp DAY	●	●	20	10	8	4	2	1
45,55,65,75	Time Stamp MONTH	●	●	●	10	8	4	2	1
46,56,66,76	Time Stamp YEAR	80	40	20	10	8	4	2	1
47,57,67,77	Status stamp	●	●	VLOW	VCMP	VDET	●	XST	●
48,58,68,78	Time stamp 1/256 s	1	2	4	8	16	32	64	128
49,59,69,79	Time Stamp SEC	●	40	20	10	8	4	2	1
4A,5A,6A,7A	Time Stamp MIN	●	40	20	10	8	4	2	1
4B,5B,6B,7B	Time Stamp HOUR	●	●	20	10	8	4	2	1
4C,5C,6C,7C	Time Stamp DAY	●	●	20	10	8	4	2	1
4D,5D,6D,7D	Time Stamp MONTH	●	●	●	10	8	4	2	1
4E,5E,6E,7E	Time Stamp YEAR	80	40	20	10	8	4	2	1
4F,5F,6F,7F	Status stamp	●	●	VLOW	VCMP	VDET	●	XST	●

After the initial power-up (from 0 V) or in case the VLF bit returns "1", make sure to initialize all registers, before using the RTC.
The TEST bit (3Fh bit7) is used by the manufacturer for testing. Be sure to set "0" for this bit when writing.
∗ Be sure to write "0" by initializing before using the clock module. Afterward, be sure to set "0" when writing.
Be sure to avoid entering incorrect date and time data, as clock operations are not guaranteed when the data or time data is incorrect.
Any bit marked with **"z**" should be used with a value of "0" after initialization. (Not writable)
Any bit marked with "●" is a RAM bit that can be used to read or write any data.
Any bit marked wit' -- 'is Not writable. Read result is unkown.
The above table shows only the user registers. Due to functional reasons, RTC has different registers not mentioned above table which are programmed by the manufactorer. Please make sure to only access above mentioned user registers.
Even if it is done Read/Write access as for “No Function”, a function else has no influence.
When not using Week data, It is not necessary for Week register to be initialized.
By read/write to register of No-Function, other functions are not affected.

13.2.2. Register Initial Value After Power on Reset

This table describes initial values after power on reset.
Note: Registers marked “X” should be initialized to 0, except time stamp area.

Table 11 Register Initial value (1)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
10h	SEC	X	X	X	X	X	X	X	X
11h	MIN	**0**	X	X	X	X	X	X	X
12h	HOUR	**0**	**0**	X	X	X	X	X	X
13h	WEEK	**0**	X	X	X	X	X	X	X
14h	DAY	**0**	**0**	X	X	X	X	X	X
15h	MONTH	**0**	**0**	**0**	X	X	X	X	X
16h	YEAR	X	X	X	X	X	X	X	X
17h	MIN Alarm	**1**	X	X	X	X	X	X	X
18h	HOUR Alarm	**1**	X	X	X	X	X	X	X
19h	WEEK Alarm	**1**	X	X	X	X	X	X	X
	DAY Alarm		X	X	X	X	X	X	X
1Ah	Timer Counter 0	X	X	X	X	X	X	X	X
1Bh	Timer Counter 1	X	X	X	X	X	X	X	X
1Ch	Timer Counter 2	X	X	X	X	X	X	X	X
1Dh	Extension Register	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
1Eh	Flag Register	**1**	**0**	**0**	**0**	**0**	**0**	**1**	X
1Fh	Control Register	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
20h	Time Stamp 1/1024S	**0**	**0**	**0**	**0**	X	X	X	X
21h	Time Stamp 1/256S	X	X	X	X	X	X	X	X
22h	Time Stamp SEC	**0**	X	X	X	X	X	X	X
23h	Time Stamp MIN	**0**	X	X	X	X	X	X	X
24h	Time Stamp HOUR	**0**	**0**	X	X	X	X	X	X
25h	Time Stamp WEEK	**0**	X	X	X	X	X	X	X
26h	Time Stamp DAY	**0**	**0**	X	X	X	X	X	X
27h	Time Stamp MONTH	**0**	**0**	**0**	X	X	X	X	X
28h	Time Stamp YEAR	X	X	X	X	X	X	X	X
29h	Status Stamp	**0**	**0**	X	X	X	**0**	X	**0**
2Ah	No Function	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
2Bh	EVIN Setting	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
2Ch	SEC Alarm	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
2Dh	Timer Control	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
2Eh	Time Stamp control 0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
2Fh	Command Trigger	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

X : Undefined. 0 or 1
0 : Reset state
1 : Set state

Table 12 Register Initial value (2)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
30h	No Function	0	0	0	0	0	0	0	0
31h	No Function	0	0	0	0	0	0	0	0
32h	Power Switch Control	0	0	0	0	0	1	0	0
33h	EVIN Monitor	0	X	0	0	0	0	0	0
34h	Time Stamp Control 1	0	0	0	0	0	0	0	0
35h	Time Stamp Control 2	0	0	0	0	0	0	0	0
36h	Time Stamp Control 3	0	0	0	0	1	1	1	1
37h	No Function	0	0	0	0	0	0	0	0
38h ~ 3Dh	No Function	0	0	0	0	0	0	0	0
3Eh	No Function	X	X	X	X	X	X	X	X
3Fh	TEST	0	0	0	0	0	0	0	0

Address Hex	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
40, 50, 60, 70	Time Stamp 1/256S	X	X	X	X	X	X	X	X
41, 51, 61, 71	Time Stamp SEC	X	X	X	X	X	X	X	X
42, 52, 62, 72	Time Stamp MIN	X	X	X	X	X	X	X	X
43, 53, 63, 73	Time Stamp HOUR	X	X	X	X	X	X	X	X
44, 54, 64, 74	Time Stamp WEEK	X	X	X	X	X	X	X	X
45, 55, 65, 75	Time Stamp DAY	X	X	X	X	X	X	X	X
46,56, 66, 76	Time Stamp Year	X	X	X	X	X	X	X	X
47,57, 67, 77	Status Stamp	X	X	X	X	X	X	X	X
48, 58, 68, 78	Time stamp 1/256S	X	X	X	X	X	X	X	X
49, 59, 69, 79	Time Stamp SEC	X	X	X	X	X	X	X	X
4A, 5A, 6A, 7A	Time Stamp MIN	X	X	X	X	X	X	X	X
4B,5B, 6B, 7B	Time Stamp HOUR	X	X	X	X	X	X	X	X
4C,5C, 6C, 7C	Time Stamp DAY	X	X	X	X	X	X	X	X
4D,5D, 6D, 7D	Time Stamp MONTH	X	X	X	X	X	X	X	X
4E,5E, 6E, 7E	Time Stamp YEAR	X	X	X	X	X	X	X	X
4F,5F, 6F, 7F	Status Stamp	X	X	X	X	X	X	X	X

X : Undefined. 0 or 1
0 : Reset state
1 : Set state

13.3. Description Of Registers

13.3.1. Clock and Calendar Counter (10h ~ 16h)

This is counter registers from a second to a year.
Please refer to [14.1 Clock calendar explanation] for the details.

13.3.2. Wake-up Timer (Down Counter) (1Ah ~ 1Ch, 2Dh)

Wake-up timer(down counter) data is read and stored in this register., along with TE, TF, TIE, TSEL1, TSEL0, TBKON, TBKEbit.
If user does not use this function, TIE,TE should be reset to ”0. The counter data is unknown.
Please refer to 14.2 Wake-up Timer. for the details.

13.3.3. Alarm Registers (17h ~ 19h)

The alarm interrupt function is used, along with the AIE, AF, and WADA bits, to set alarms for specified date, day, hour, and minute values. If user does not use this function, AIE should be reset to ”0. The data is unknown.
Please refer to 14.3 Alarm Interrupt. for the details.

13.3.4. Function-Related Register (1Dh ~ 1Fh)

1) FSEL1, FSEL0 bit

A combination of the FSEL1 and FSEL0 bits are used to select the frequency to be output.
If customer does not use this function, FESL1, FSEL0 should be set to ”1”.
Please refer to 14.6 FOUT Function

2) USEL, UF, UIE bit

This bit is used to specify either "second update" or "minute update" as the update generation timing of the time update interrupt function.
If customer does not use this function, USEL, UIE should be reset to”0. UF do not care.”.
Please refer to [14.4. Update interrupt function] for the details.

3) TE, TF, TIE, TSEL1, TSEL0, TSTP, TBKON, TBKE, TMPIN bit

These bits are used to control operation of the wake-up timer interrupt function.
If customer does not use this function, (TE, TIE, TSTP, TMPIN) should be (0,0,0,0), TSEL1, TSEL0(1,0). TF do not care.
Please refer to [14.2 Wake-up timer interrupt function] for the details.

4) WADA, AF, AIE bit

These bits are used to control operation of the alarm interrupt function.
If customer does not use this function, WADA should be “1”, AIE“0”. AF do not care.
Please refer to [14.3. Alarm interrupt function] for the details.

5) ETS, EVF, EIE bit

These bits are used to control operation of the time stamp function.
If customer does not use this function, ETS, EIE should be reset to “0”. EVF do not care.
Please refer to [14.8. Time Stamp function] for the details.

6) VLF, POR, XST bit

These bits are used to detect RTC inner status and recording.
Ex. During power on resetting , lower voltage detection makes VLF bit “1”.
Please refer to [14.5. RTC inner status detection function] for the details.

7) STOP bit

This bit is to stop a timekeeping operation. In the case of “STOP bit = 1":
All the update of timekeeping (year, month, day, week, hour, minute, second, 1/128, 1/512) operation and the calendar operation stops. With it, an update interrupt event does not occur at an alarm interrupt and the time stamp data is to be stopping condition. (Please refer to 14.8.5)
The part of the fixed-cycle timer interrupt function stops.
A count stops the source clock setting of the timer in case of "64 Hz, 1 Hz, 1 min, 1 h".
(In case of 4096 Hz, it does not stop.)
The effect of STOP bit to FOUT functions.
When STOP = "1", 32.768 kHz and 1024 Hz output is possible. But 1 Hz output is disabled.
4) Switchover function cannot work in order that the V_{DD} voltage drop detection stops even if a main power supply falls.

13.3.5. Battery Backup Switchover Function Related Register (32h)

Please refer to 14.7 Battery Backup Switchover function for the details.

1) CHGEN bit
Setting of backup battery charge control (ON/OFF).

2) INIEN bit
Setting of a power switchover function (ON/OFF).

3) SMPT1, SMPT0 bit
Operation time setting of a voltage detector circuit for each power supply pin.

4) SWSEL1, SWSEL0 bit
Operation voltage detector circuit during battery backup switchover function disable.

13.3.6. Time Stamp Register

Please refer to 14.8 Time Stamp function for the details.

1) Time Stamp, Status recording register (20h ~ 29h, 40h ~ 7Fh)
In case of event occasion, time stamp (1/1024 sec ~ Yea) and inner status are recorded into these registers.

2) EVIN terminal control register (2Bh)
Setting of EVIN terminal.

3) Command Trigger, Time Stamp Control register (2Eh ~ 2Fh)
It is used for time stamp trigger timing via I^2C bus.

4) Time Stamp Trigger Control Register (35h)
It is used for time stamp trigger except EVIN.

13.3.7. Operation Status Detection Register (33h)

Please refer to 14.5 Operation Status Detection function for the details.-

1) EVIN bit
EVIN terminal detection voltage level H/L

2) VCMP bit
VCMP Comparison result

3) VLOW bit
VLOW Detection result

13.3.8. User Register (40h ~ 7Fh)

User can use this area as user's RAM by setting 34h TSRAM bit "0".

14. How to use

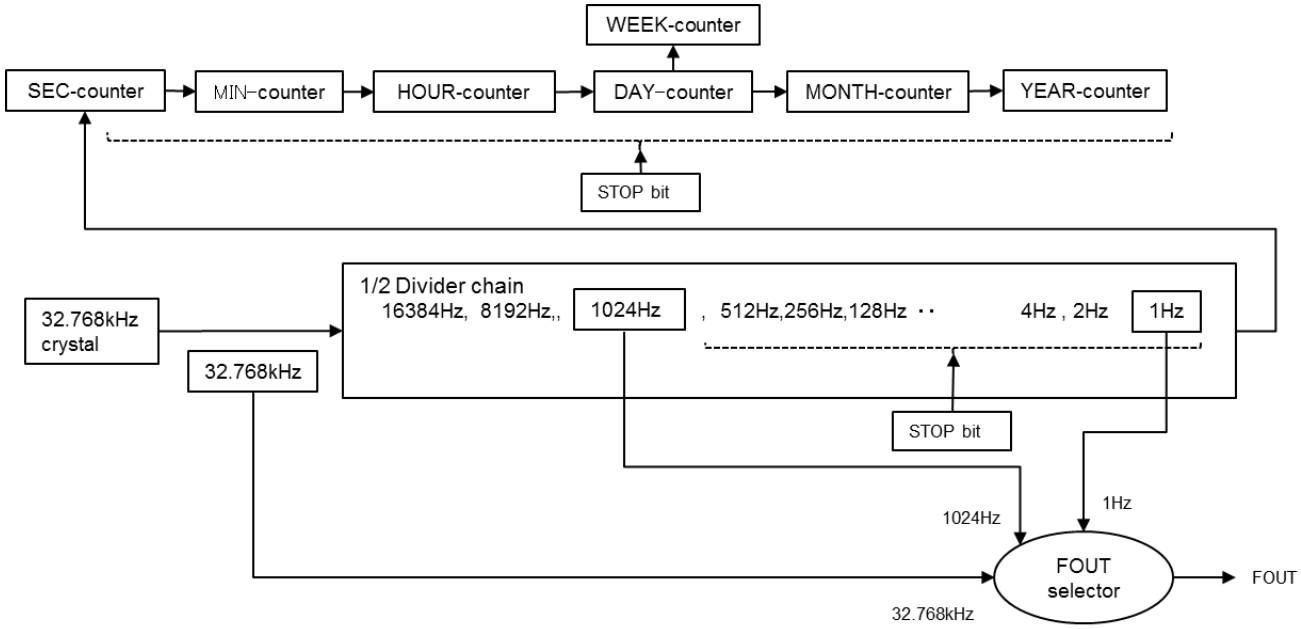


Figure 18 Basic (32.768 kHz oscillation, counter, FOUT) Function

14.1. Clock Calendar Function

At the time of a communication start, the Clock & Calendar data are fixed (hold the carry operation), and it is automatically revised at the end of the communication. Therefore, it is recommended that the access to a clock calendar has continuous access by the auto increment function.
At the moment of current time reading, STOP bit should be “0”.

Table 13 Time, calendar setting example

Example ’88 February 29 (Sun) 17:39:45 (leap year)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
10h	SEC	0	1	0	0	0	1	0	1
11h	MIN	0	0	1	1	1	0	0	1
12h	HOUR	0	0	0	1	0	1	1	1
13h	WEEK	0	0	0	0	0	0	0	1
14h	DAY	0	0	1	0	1	0	0	1
15h	MONTH	0	0	0	0	0	0	1	0
16h	YEAR	1	0	0	0	1	0	0	0

Note With caution that writing non-existent time data may interfere with normal operation of the clock counter
Note Time starts at the moment of STOP bit operation (H →L timing)

14.1.1. Clock Counter

1) [SEC], [MIN] register
These registers are 60-base BCD counters. When update signals were generated from a lower counter, a upper counter is one incremented.. At the timing when the lower register changes from 59 to 00, carry is generated to the higher register and thus incremented.
When writing is performed to [SEC] register, Internal-count-down-chain less than one second (512 Hz ~ 1 Hz) is cleared to 0.

2) [HOUR] register
This register is a 24-base BCD counter (24-hour format). These registers are incremented at the timing when carry is generated from a lower register.

3) Leap second adjustment
For leap second adjustment, user can write “60” into SEC counter, after 1 second SEC counter is to be set “00”.
Normally second counter counts up “59” to “00”.

14.1.2. Week Counter

The day (of the week) is indicated by 7 bits, bit 0 to bit 6.
The day data values are counted as: Day 01h → Day 02h → Day 04h → Day 08h → Day 10h → Day 20h → Day 40h → Day 01h → Day 02h, etc.
It is incremented when carry is generated from the HOUR register. This register does not generate carry to a higher register. Since this register is not connected with the YEAR, MONTH and DAY registers, it needs to be set again with the matching day of the week if any of the YEAR, MONTH or DAY registers have been changed.
When not use Week data, It is not necessary for Week register to be initialized.
Do not set "1" to more than one day at the same time.

Table 14 Setting example of the week register value

Day	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Data
Sunday	0	0	0	0	0	0	0	1	01 h
Monday	0	0	0	0	0	0	1	0	02 h
Tuesday	0	0	0	0	0	1	0	0	04 h
Wednesday	0	0	0	0	1	0	0	0	08 h
Thursday	0	0	0	1	0	0	0	0	10 h
Friday	0	0	1	0	0	0	0	0	20 h
Saturday	0	1	0	0	0	0	0	0	40 h

14.1.3. Calendar Counter

1) [DAY], [MONTH] register
The DAY register is a variable (between 28-base and 31-base) BCD counter that is influenced by the month and the leap year. The MONTH register is a 12-base BCD counter triggered by carry over of the day register.

Table 15 DAY, MONTH register

		Jan.	Feb.	Mar	Apr.	May	June	July	Aug.	Sep.	Oct.	Nov.	Dec.
Days	Normal year	31	28	31	30	31	30	31	31	30	31	30	31
	Leap year		29										

2) [YEAR] register

This register is a BCD counter for years 00 to 99.
The leap year is automatically determined and influences the DAY register.
This RTC processes following years as leap years: 00,04,08,12, 96.
User software correction is needed in the years 2100, 2200, 2300 as they are common years.

Definition of leap years
Leap year : year divisible by 4, year divisible by 400
Ex. 2000, 2004, 2008, 2012, 2096, 2400, 2800,
Common year: year indivisible by 4, year divisible by 100
Ex. 2001, 2002, 2003, 2005, 2099, 2100, 2200, 2300, 2500,,

14.2. Wake-up Timer Interrupt Function

The wake-up timer interrupt function generates an interrupt event periodically at any fixed cycle set between 244.14 μs and 31.9 years. This function can stop at one time and is available as an accumulative timer.
After the interrupt occurs, the /INT status is automatically cleared .

14.2.1. Related registers for function of wake-up timer interrupt function

Table 16 Wake-up interrupt timer register

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1Ah	Timer Counter 0	128	64	32	16	8	4	2	1
1Bh	Timer Counter 1	32768	16384	8192	4096	2048	1024	512	256
1Ch	Timer Counter 2	8388608	4194304	2097152	1048576	524288	262144	131072	65536
1Dh	Extension Register	FSEL1	FSEL0	USEL	TE	WADA	ETS	TSEL1	TSEL0
1Eh	Flag Register	POR	z	UF	TF	AF	EVF	VLF	XST
1Fh	Control Register	z	z	UIE	TIE	AIE	EIE	z	STOP
2Dh	Timer Control	z	z	z	z	TBKON	TBKE	TMPIN	TSTP

Before entering operation settings, we recommend first clearing the TE bit to "0" .
When the fixed-cycle timer function is not being used, the fixed-cycle Timer Counter0,1 register can be used as a RAM register. In such cases, stop the fixed-cycle timer function by writing "0" to the TE and TIE bits.

1) Down counter for wake-up interrupt timer Timer Counter 2, 1, 0

This register is used to set the default (preset) value for the counter. Any count value from 1 (000001h) to 16777216 (FFFFFFh) can be set.
Be sure to write "0" to the TE bit before writing the preset value.

When TE = 0, read out data of timer counter is default (Preset) value. And when TE = 1, read out data of timer counter is just counting value. But, when access to timer counter data, counting value is not held.
Therefore, for example, perform twice read access to obtain right data, and a way to adopt the case that two data accorded is necessary.

2) TSEL1, TESL0 bit

This combination decides the source clock of count down period.
The source clock selection should be done after TE bit setting to “0”.

Table 17 TSEL bit, selection of source clock

TSEL1 (bit 1)	TSEL0 (bit 0)	Source clock		Auto reset time (tRTN)
0	0	4096 Hz	Once per 244.14 μs	122 μs
0	1	64 Hz	Once per 15.625 ms	7.813 ms
1	0	1 Hz	Once per 1 second	7.813 ms
1	1	1/60 Hz	Once per minute	7.813 ms

The /INT pin's auto reset time (tRTN) varies as shown above according to the source clock setting.
The first countdown shortens than a source clock.

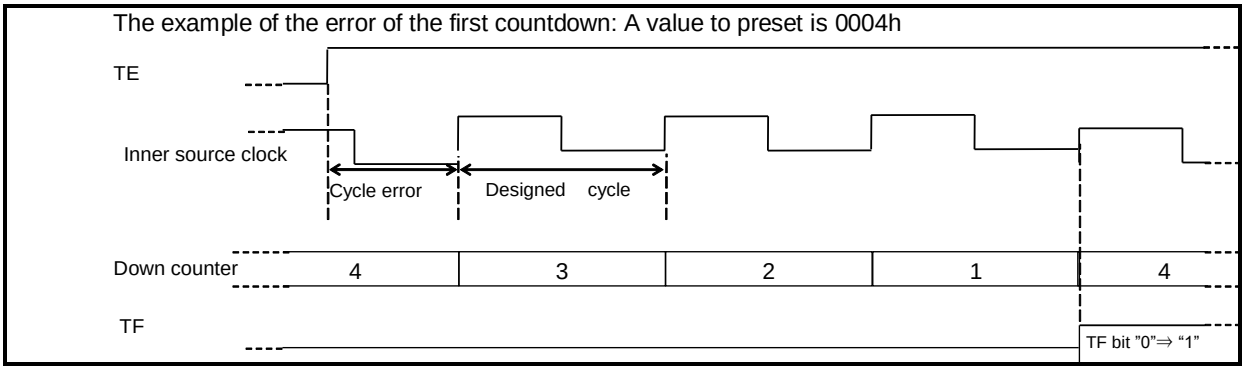


Figure 18 Wake-up timer initial sequence (cycle error)

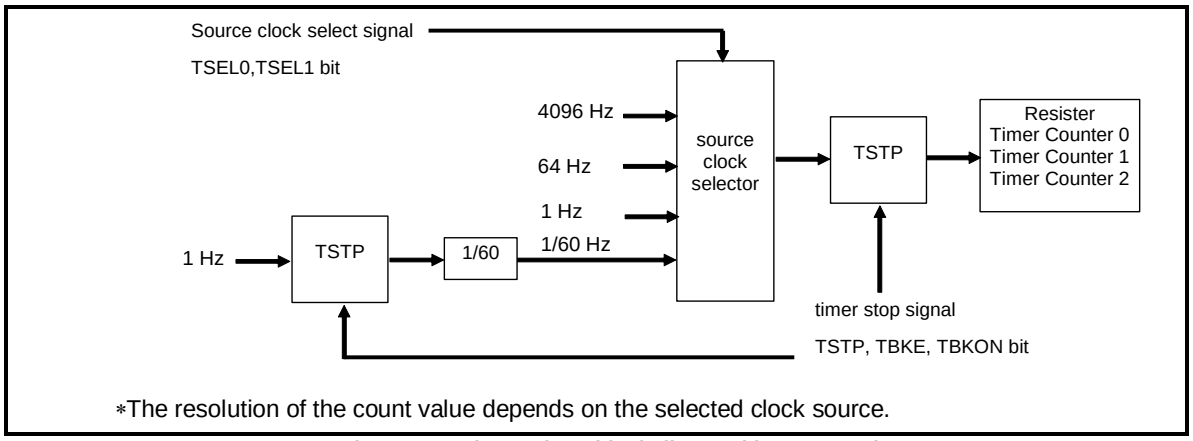


Figure 19 Wake-up timer block diagram(timer source)

3) TE bit (Timer Enable)

The bit controls wake-up timer start / stop.

Table 18 TE bit (Timer Enable)

TE	Data	Description
Write	0	Stops wake-up interrupt timer interrupt function. Clearing this bit to zero does not enable the /INT low output status to be cleared (to Hi-Z).
	1	Starts wake-up interrupt timer interrupt function. The countdown that starts when the TE bit value changes from "0" to "1" always begins from the preset value.

4) TF bit (Timer Flag)

This is a flag bit that retains the result when a wake-up timer interrupt event is detected.

Table 19 TF bit (Timer Flag)

TF	Data	Description
Write	0	The TF bit is cleared to zero to prepare for the next status detection Clearing this bit to zero is not enable the /INT low output status to be cleared (to Hi-Z).
	1	Invalid (writing “1” will be ignored)
Read	0	–
	1	Wake-up timer interrupt events are detected. (Result is retained until this bit is cleared to zero.)

5) TIE bit (Timer Interrupt Enable)

This bit is used to control output of interrupt signals from the /INT pin when a wake-up timer interrupt event has occurred.

Table 20 TIE bit (Timer Interrupt Enable)

TIE	Data	Description
Write	0	1) When a wake-up timer interrupt event occurs, an interrupt signal is not generated. 2) When a wake-up timer interrupt event occurs, the interrupt signal is canceled (/INT status changes from low to Hi-Z).
	1	When a wake-up timer interrupt event occurs, an interrupt signal is generated (/INT status changes from Hi-Z to low).

6) TBKON, TBKE bit (Timer Backup ON, Timer Backup/normal Enable)

When TBKE = ”1”,This function selects the operation time with the main power supply or the operation time with the backup power supply. The count value is accumulated.

Table 21 TBKON, TBKE bit (Timer Backup ON, Timer Backup/normal Enable)

operation	TBKE	TBKON	Description
Write	0	X	This setting counts normal mode and backup mode.
	1	0	This setting counts it at time of normal mode(V_{DD} operation)
		1	This setting counts it at time of backup mode (V_{BAT} operation)

7) TMPIN bit (Timer PIN)

FOUT terminal can be allocate as wake-up timer interrupt output. To use wake-up timer interrupt output, FSEL1,0 should be (0,0) because this output has logical OR output of FOUT and wake-up timer interrupt.

Table 22 TMPIN bit (Timer PIN)

TMPIN	Data	Description
Write	0	FOUT terminal works as /INT of wake-up timer interrupt.
	1	Normal FOUT port

8) TSTP bit (Timer Stop)

This bit is used to stop wake-up timer count down.

Table 23 TSTP bit (Timer Stop)

TE	**STOP**	**TBKE**	**TSTP**	Description
1	0	0	0	Writing a "0" to this bit cancels stop status (restarts timer counts down). The reopening value of the countdown is a stopping value
			1	Count stops.
		1	X	Setting of TSTP value becomes invalid, and the count does not stop even if set it in TSTP = "1".
	1	X	X	The count stops at the time of the setting of 64 Hz, 1 Hz,1/60 Hz.
0	X	X	X	It doesn't start counting

14.2.2. Wake-up timer start timing

Counting down of the fixed-cycle timer value starts at the rising edge of the SCL (ACK output) signal that occurs when the TE value is changed from "0" to "1".

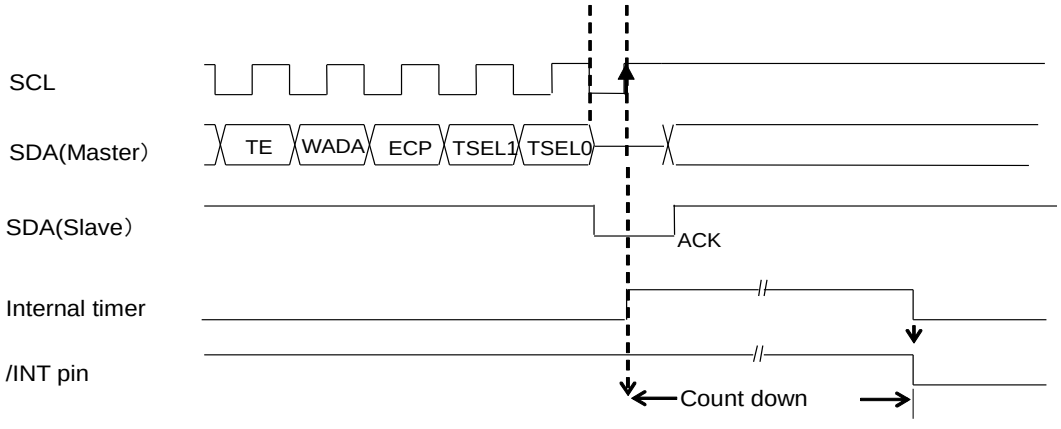


Figure 19 Wake-up timer start sequence

14.2.3. Wake-up timer interrupt interval

The combination of the source clock selection and wake-up timer value interruption interval, as shown in the following table. When counter setting is all 0, counter doesn't work.

Table 24 Wake-up timer interrupt cycles

Timer Counter setting 1 ~ 16777216	Source clock			
	4096 Hz TSEL1, 0 = 0, 0	64 Hz TSEL1, 0 = 0, 1	1 Hz TSEL1, 0 = 1, 0	1/60 Hz TSEL1, 0 = 1, 0
0	–	–	–	–
1	244.14 μs	15.625 ms	1 s	1 min
•	•	•	•	•
410	100.10 ms	6.406 s	410 s	410 min
•	•	•	•	•
3840	0.9375 s	60.000 s	3840 s	3840 min
•	•	•	•	•
4096	1.0000 s	64.000 s	4096 s	4096 min
•	•	•	•	•
16777216	1.13 h	72.81 h	4660 h	31.9 Year

14.2.4. Diagram of wake-up timer interrupt function

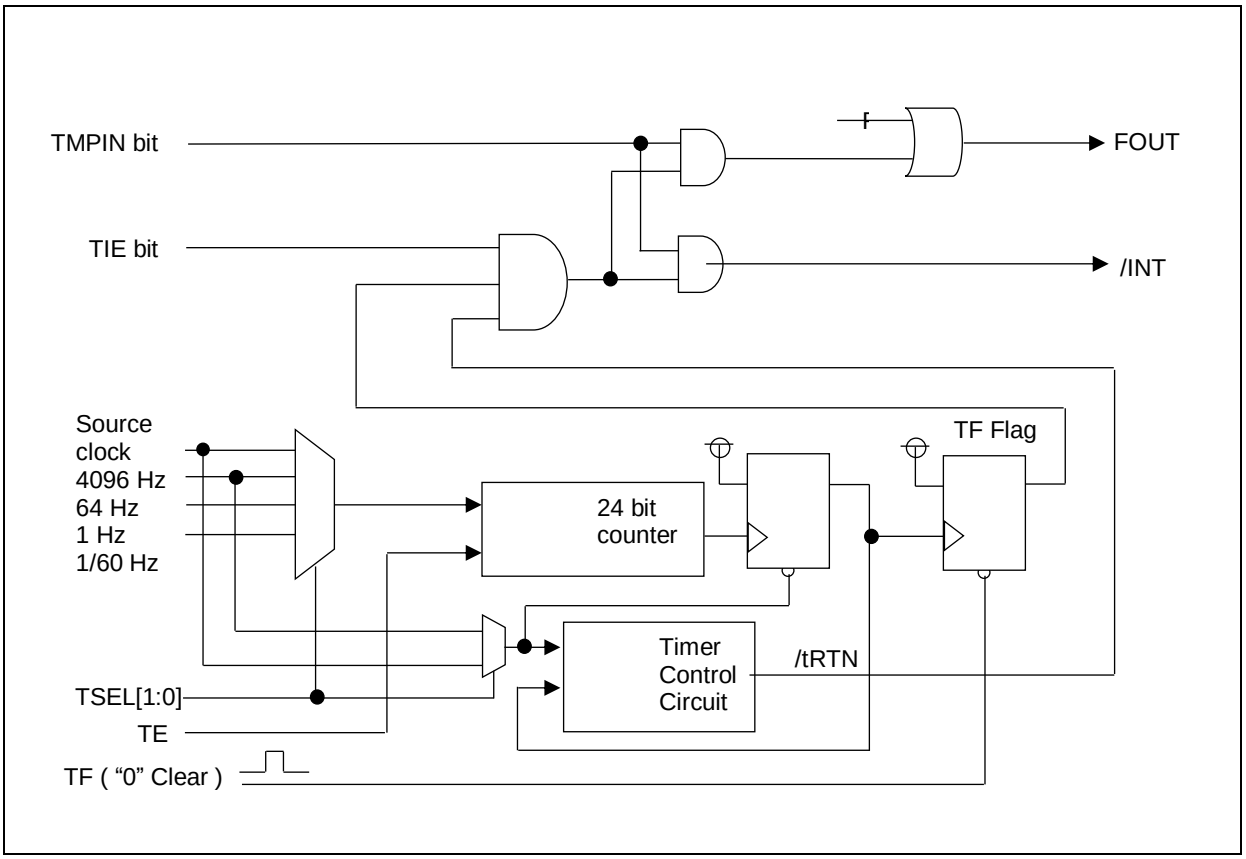


Figure 20 Wake-up timer block diagram

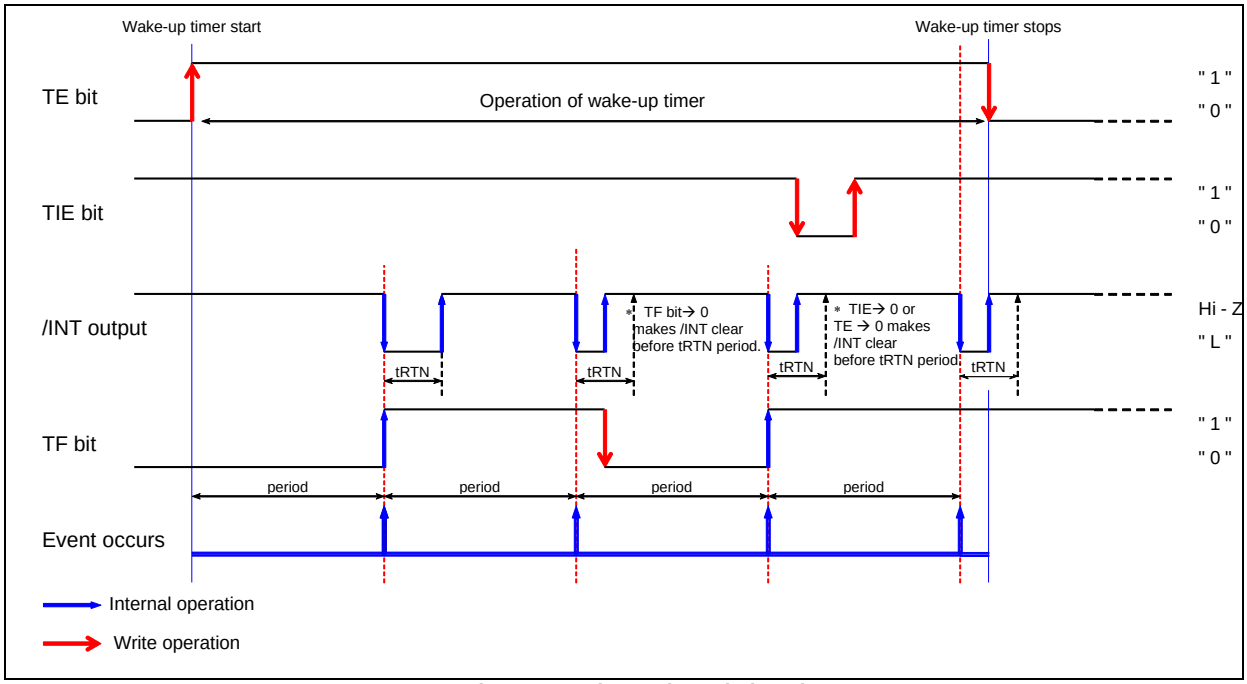


Figure 21 Wake-up timer timing chart

After wake-up counter interrupt, pre-set data is re-loaded to counter. Count down repeats from pre-set value.
By setting TE, "0" → "1" wake-up counter starts counting down.
Pre-set value count down is available by setting TE "0" → "1" only.

14.3. Alarm Interrupt Function

The alarm interrupt function generates interrupt events for alarm settings such as date, day, hour, and minute settings. When an interrupt event occurs, the AF bit value is set to "1" and the /INT pin goes to low level to indicate that an event has occurred. This RTC retains the status of /INT = “L” until intentional resetting.

14.3.1. Related registers for Alarm interrupt functions.

Table 25 Alarm Interrupt register

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
2Ch	SEC Alarm	**AE**	40	20	10	8	4	2	1
17h	MIN Alarm	**AE**	40	20	10	8	4	2	1
18h	HOUR Alarm	**AE**	•	20	10	8	4	2	1
19h	WEEK Alarm	**AE**	6	5	4	3	2	1	0
	DAY Alarm		•	20	10	8	4	2	1
1Dh	Extension Register	FSEL1	FSEL0	USEL	TE	WADA	ETS	TSEL1	TSEL0
1Eh	Flag Register	POR	**z**	UF	TF	AF	EVF	VLF	XST
1Fh	Control Register	**z**	**z**	UIE	TIE	AIE	EIE	**z**	STOP

Before setup of Alarm, settings, it is recommended be clears AIE bit by 0 for prevent hardware interrupts from occurring inadvertently. When the STOP bit value is 1 alarm interrupt events do not occur. When the alarm interrupt function is not being used, the Alarm registers (Reg – 17h to 19h, 2Ch) can be used as a RAM register.
In such cases, be sure to write "0" to the AIE bit.

1) Alarm registers

The minute, hour, day and date when an alarm interrupt event will occur is set using this register and the WADA bit.
In the WEEK alarm /Day alarm register (Reg – 19h), the setting selected via the WADA bit determines whether WEEK alarm data or DAY alarm data will be set. If WEEK has been selected via the WADA bit, multiple days can be set (such as Monday, Wednesday, Friday, Saturday).
Unwanted alarm term is decided by setting respective AE bit =”1”. If AE is set to “1”, this alarm term becomes inactive.
Ex. WEEK Alarm / DAY Alarm (19h) = 80h (AE = ”1”) hour, minute, second alarm active week, day alarm inactive
Setting all AE bit “1” makes every one second alarm exceptionally. The result is reflected in AF bit.
Alarm event does not occur even user set alarm time to current time. Coming next time matching (alarm time = current time) can occur the event.

2) WADA bit (Week Alarm / Day Alarm Select)

The alarm interrupt function uses either "Day" or "Week" as its target. The WADA bit is used to specify either WEEK or DAY as the target for alarm interrupt events.

Table 26 WADA bit (Week Alarm / Day Alarm Select)

WADA	Data	Description
Write	0	Sets WEEK as target of alarm function
	1	Sets DAY as target of alarm function

3) AF bit (Alarm Flag)

When this flag bit value is already set to "0", occurrence of an alarm interrupt event changes it to "1". When this flag bit value is "1", its value is retained until a "0" is written to it.

Table 27 AF bit (Alarm Flag)

AF	Data	Description
Write	0	Clearing this bit to zero enables /INT low output to be canceled (/INT remains Hi-Z) when an alarm interrupt event has occurred.
	1	Invalid (writing “1” will be ignored).
Read	0	–
	1	Alarm interrupt events are detected. (Result is retained until this bit is cleared to zero.)

4) AIE bit (Alarm Interrupt Enable)
This bit is used to control output of interrupt signals from the /INT pin when an Alarm interrupt event has occurred.

Table 28 AIE bit (Alarm Interrupt Enable)

AIE	Data	Description
Write	0	1) When an alarm interrupt event occurs, an interrupt signal is not generated or is canceled (/INT status remains Hi-Z). 2) When an alarm interrupt event occurs, the interrupt signal is canceled (/INT status changes from low to Hi-Z).
	1	When an alarm interrupt event occurs, an interrupt signal is generated (/INT status changes from Hi-Z to low).

The AIE bit is only output control of the /INT terminal. It is necessary to clear an AF flag to cancel alarm.

14.3.2. Examples of alarm settings

Example of alarm settings when "Week" has been specified (and WADA bit = "0")

Table 29 WEEK alarm example 1

Week is specified WADA bit = "0"	bit 7 AE	bit 6 S	bit 5 F	bit 4 T	bit 3 W	bit 2 T	bit 1 M	bit 0 S	HOUR Alarm	MIN Alarm	SEC Alarm
Monday through Friday, at 7:00 AM 1 minute (60 sec) alarm	0	0	1	1	1	1	1	0	07 h	00h	AE bit = 1
Every Saturday and Sunday, for 30 minutes each hour Hour value is ignored	0	1	0	0	0	0	0	1	AE bit = 1	30 h	00h
Every day, at 6:59:30 AM	0 1	1 X	1 X	1 X	1 X	1 X	1 X	1 X	18 h	59 h	30h

X : don't care

1) Example of alarm settings when "Day" has been specified (and WADA bit = "1")

Table 30 WEEK alarm example 2

Day is specified WADA bit = "1"	bit 7 AE	bit 6 ●	bit 5 20	bit 4 10	bit 3 08	bit 2 04	bit 1 02	bit 0 01	HOUR Alarm	MIN Alarm	SEC Alarm
First of each month, at 7:00 AM 1 minute (60sec) alarm Second value is ignored	0	0	0	0	0	0	0	1	07 h	AE bit " 1 "	AE bit = 1
15th of each month, for 30 minutes each hour Hour value is ignored	0	0	0	1	0	1	0	1	AE bit = 1	30 h	00h
Every day, at 6:59:30 PM	1	X	X	X	X	X	X	X	18 h	59 h	30h

X : don't care

14.3.3. Diagram of alarm interrupt function

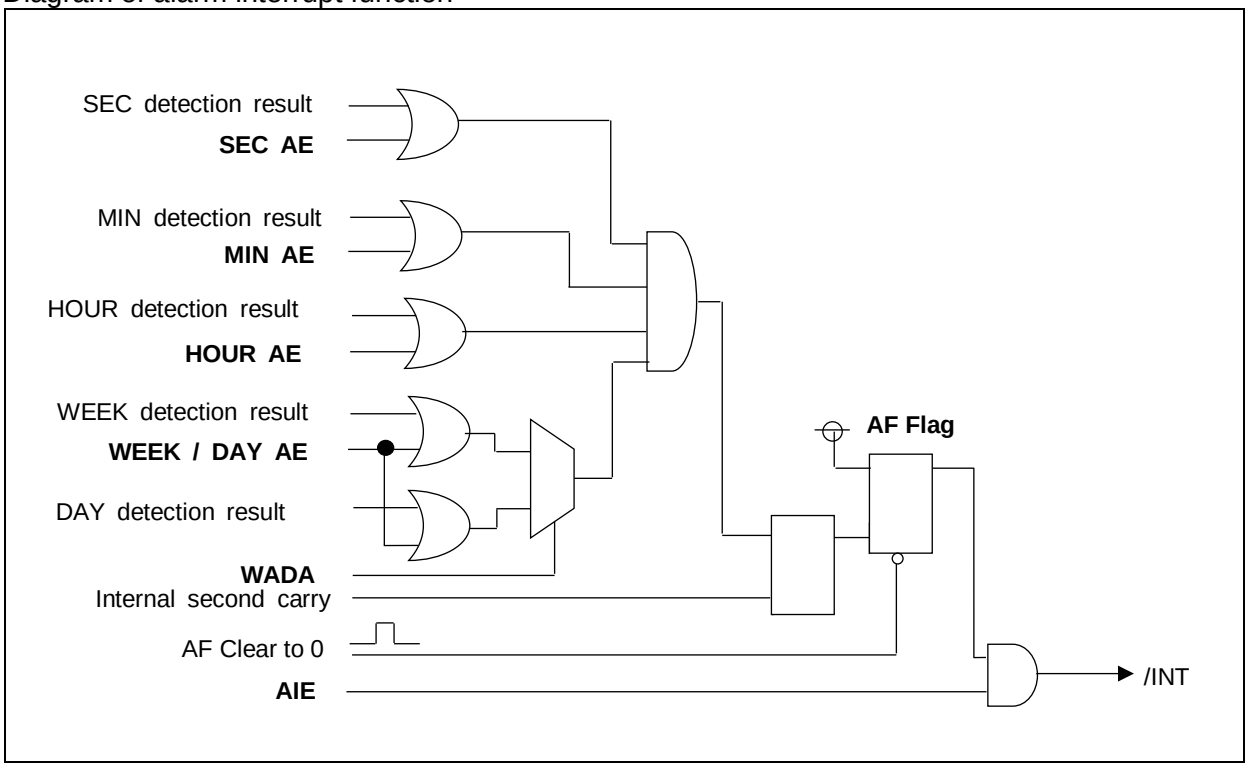


Figure 22 Alarm interrupt block diagram

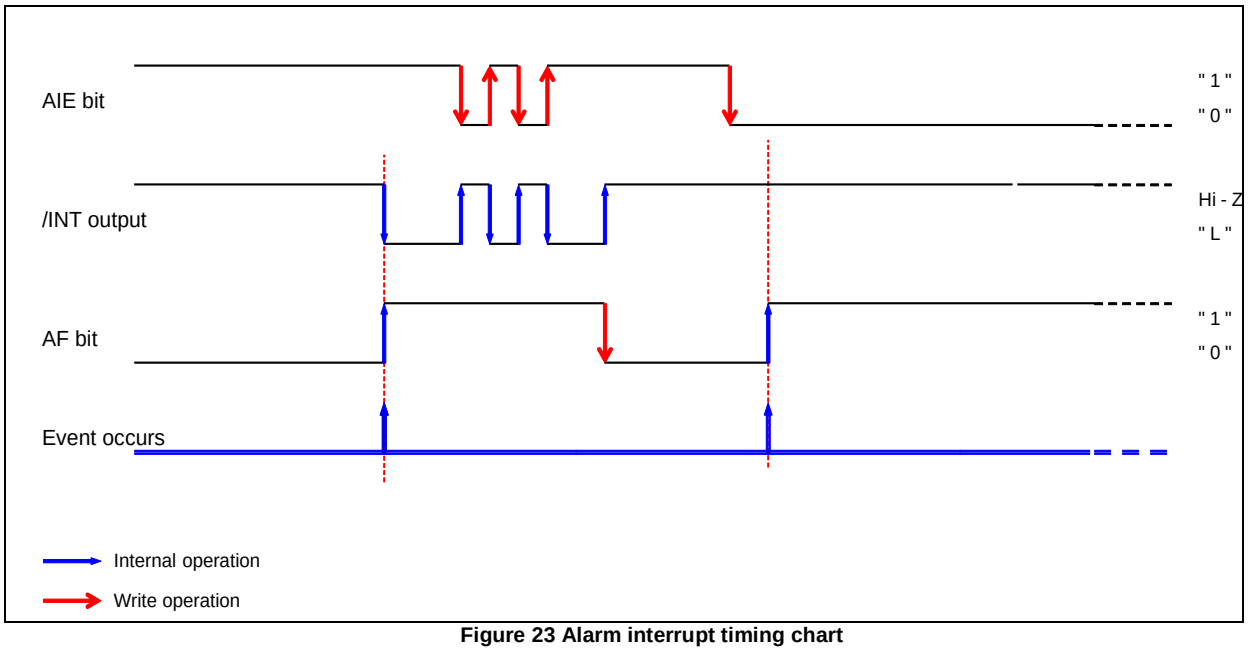


Figure 23 Alarm interrupt timing chart

14.4. Time Update Interrupt Function

The time update interrupt function generates interrupt in one-second or one-minute intervals which are synchronized to the update of the second or minute time register of the RTC. When an interrupt event is generated, this /INT status is automatically cleared (/INT status changes from low level to Hi-Z 7.57 ms after the interrupt occurs).

14.4.1. Related registers for time update interrupt functions.

Table 31 Time update interrupt register

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1Dh	Extension Register	FSEL1	FSEL0	USEL	TE	WADA	ETS	TSEL1	TSEL0
1Eh	Flag Register	POR	**z**	UF	TF	AF	EVF	VLF	XST
1Fh	Control Register	**z**	**z**	UIE	TIE	AIE	EIE	**z**	STOP

Before entering settings for operations, it is recommended writing a "0" to the UIE bit to prevent hardware interrupts from occurring inadvertently while entering settings.
When the STOP bit value is "1" time update interrupt events do not occur.
Although the time update interrupt function cannot be fully stopped, if "0" is written to the UIE bit, the time update interrupt function can be prevented from changing the /INT pin status to low.
Time update interrupt function cannot be inactive. User can set /INT output inactive.

1) USEL bit (Update Interrupt Select)

This bit is used to select "second" update or "minute" update as the timing for generation of time update interrupt events.

Table 32 USEL bit (Update Interrupt Select)

USEL	data	Description
Write / Read	0	Selects "second update" (once per second) as the timing for generation of interrupt events
	1	Selects "minute update" (once per minute) as the timing for generation of interrupt events

2) UF bit (Update Flag)

This flag bit value changes from "0" to "1" when a time update interrupt event occurs.

Table 33 UF bit (Update Flag)

UF	data	Description
Write	0	Clearing this bit to zero enables /INT low output to be canceled (/INT remains Hi-Z) when a time update interrupt event has occurred.
	1	Invalid.
Read	0	–
	1	Time update interrupt events are detected. (The result is retained until this bit is cleared to zero.)

3) UIE bit (Update Interrupt Enable)

This bit selects whether to generate an interrupt signal or to not generate it.

Table 34 UIE bit (Update Interrupt Enable)

UIE	data	Description
Write / Read	0	1) Does not output an interrupt signal when a time update interrupt event occurs. 2) interrupt output of only time update event is cancelled.
	1	When a time update interrupt event occurs, an interrupt signal is generated (/INT status changes from Hi-Z to low). Earliest 7.57 ms after the interrupt occurs, the /INT is released automatically (/INT status changes from low to Hi-Z).

14.4.2. Time update interrupt function diagram

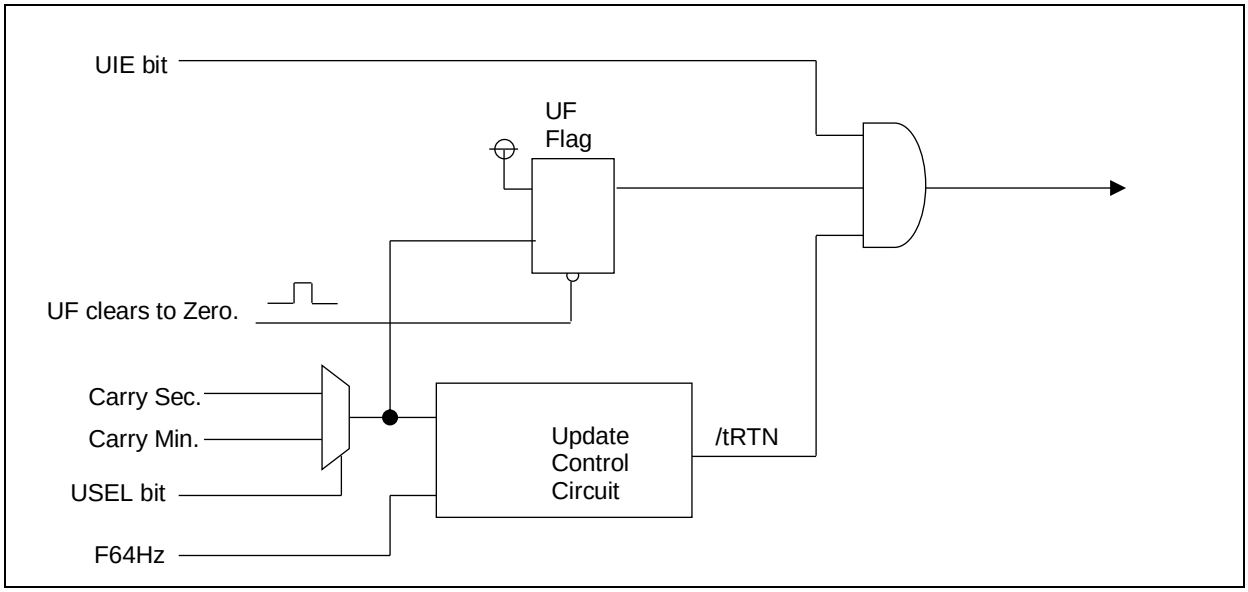


Figure 24 Time Update Interrupt block diagram

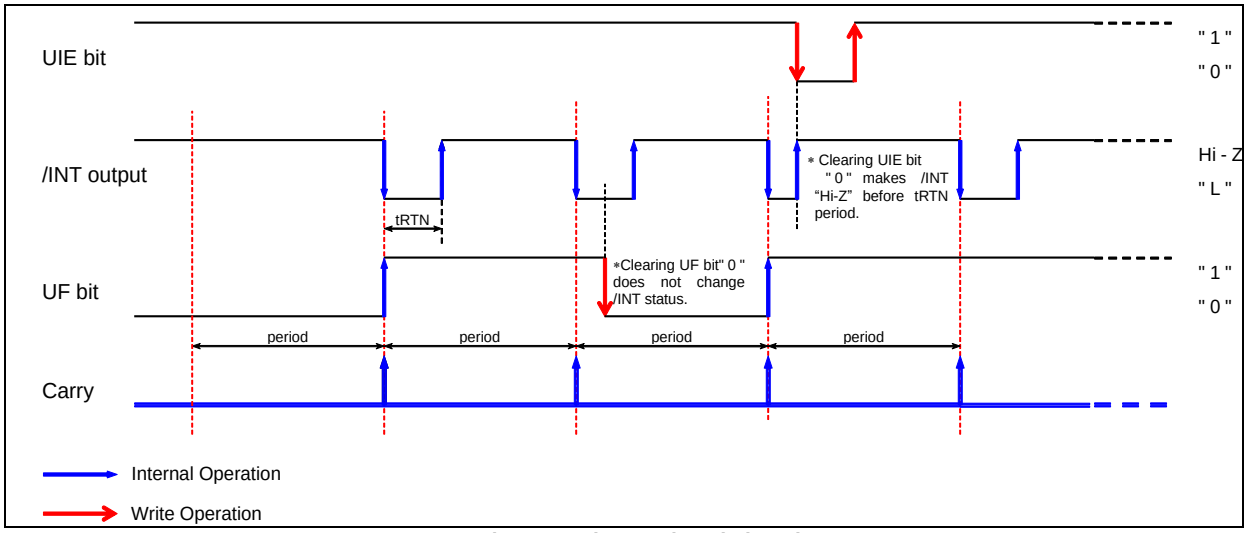


Figure 25 Time Update timing chart

14.5. RTC self monitoring Detection

These bits are flag bit of each of functions of RTC.
It is a flag bit that detects the state of this product and holds the result.

- POR Power ON Reset detection
- VLF Detects Internal Voltage Low.
- XST Oscillation stop detection.
- EVIN Event input status.
- VCMP Battery Charge status.
- VLOW bit Battery Low.

14.5.1. Related registers for RTC internal status detection

Table 35 RTC Internal status detection registers

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1Eh	Flag Register	**POR**	**z**	UF	TF	AF	EVF	**VLF**	**XST**
33h	Status Monitor	**z**	**EVIN**	**z**	**z**	**VCMP**	**z**	**VLOW**	**z**

1) POR bit (Power On Reset)
This bit records power on reset operation.

Table 36 POR bit (Power On Reset)

POR	Data	Description
Write	0	The POR bit is cleared to 0 and waiting for the next power on reset detection
	1	Invalid (writing “1” will be ignored)
Read	0	No power on reset detection
	1	Power on reset is detected. The result remains until clearing “0”. All registers are set into default condition by power on rest.

2) VLF bit (Voltage Low Flag)
This bit is reflected with status of POR or XST.

Table 37 VLF bit (Voltage Low Flag)

VLF	Data	Description
Write	0	The VLF is cleared to 0 and waiting for next low voltage detection.
	1	Invalid (writing “1” will be ignored)
Read	0	Oscillation status is normal, RTC register data are valid.
	1	Either power on reset or X’tal oscillation stop is detected. The result remains until clearing “0”. User can check the RTC status and initialize by software.(At power on timing etc.)

3) XST bit (X’tal Oscillation Stop)
This bit records RTC internal crystal oscillation stop status.
Time stamp function is not active if there is no oscillation; it will be active once oscillation begins
∗when oscillation stopped longer than 10 ms, XST is set to 1. This bit is not cleared to “0” by power on reset.

Table 38 XST bit (X’tal Oscillation Stop)

XST	Data	Description
Write	0	The XST is cleared to 0 and waiting for next oscillation stop detection.
	1	Invalid (writing “1” will be ignored)
Read	0	No RTC internal crystal oscillation stop detection
	1	RTC internal crystal oscillation stop is detected. The result remains until clearing “0”.

4) EVIN bit (Input level monitor of EVIN terminal)
This bit monitored EVIN terminal input voltage High / Low.

Table 39 EVIN bit (EVIN Level)

EVIN	Data	Description
Read	0	EVIN terminal input voltage Low level
	1	EVIN terminal input voltage High level

5) VCMP bit
User can monitor the status of VCMP during the period that battery is being recharged.

Table 40 VCMP bit (VCMP)

VCMP	Data	Description
Read	0	$V_{BAT} < V_{DD}$ Recharging
	1	$V_{BAT} > V_{DD}$ Recharging suspended SW2:OFF

6) VLOW bit
User can monitor the result of VLOW (battery backup lower voltage) .

Table 41 VLOW bit (VLOW)

VLOW	Data	Description
Read	0	$V_{BAT} > V_{LOW}$
	1	$V_{BAT} < V_{LOW}$

14.6. FOUT function (Clock output function)

The clock signal can be output via the FOUT pin. In case of inactive pin output becomes Hi-Z.

14.6.1. FOUT control register

Table 42 FOUT control register

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1Dh	Extension Register	**FSEL1**	**FSEL0**	USEL	TE	WADA	ETS	TSEL1	TSEL0

FOUT pin can be terminated as wake-up timer too. When FOUT function is needed, TMPIN should be “0” and /INT pin should be wake-up timer interrupt output.

14.6.2. FOUT function table

1) FSEL1,FSEL0 bit

Table 43 FSEL register

FSEL1	FSEL0	Output
0	0	32.768 kHz Output
0	1	1024 Hz Output
1	0	1 Hz Output
1	1	OFF

At the time of the initial power-on, “0” is set to FSEL1, FSEL0.
Note: The effect of STOP bit to FOUT functions.
When STOP = "1", 32.768 kHz and 1024 Hz output is possible.
But 1 Hz output is disabled.

14.7. Battery backup switchover function

14.7.1. Description of Battery backup switchover function

There are three kinds of detection, switchover functions.
1) V_{DD} voltage detection (VDET) comparison between V_{DD} voltage and V_{DET1} (INIEN register control)
2) V_{BAT} recharge detection (VCMP) comparison between V_{BAT} voltage and V_{DD} voltage (CHGEN register control).
3) V_{BAT} voltage detection (VLOW) comparison between V_{BAT} voltage and V_{LOW} voltage (EVLOW register control)

V_{DD} voltage detection and V_{BAT} recharge detection are shown in Figure 31 and Figure 32.
The detection, switchover function is composed from diodes ,switch and comparator between V_{DD} and V_{BAT}.
The RTCs backup function is built in a way to prevent reverse current flow from V_{BAT} to V_{DD}.

There are two kinds of operation modes:
1) Normal mode power supply from V_{DD}
2) Backup mode power supply from V_{BAT}
In backup mode FOUT pin becomes Hi-Z, I^2C input enable (SDA, SCL: Hi-Z).

VLF detection (VLF bi"0" → "1） makes battery backup switchover related register to default.

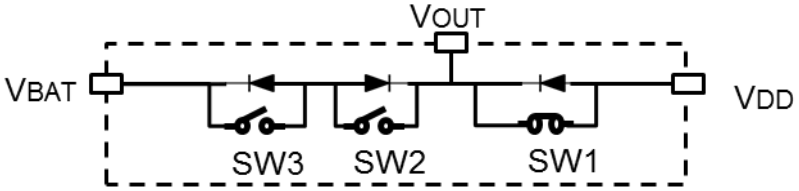


Figure 26 Battery Backup switchover function block diagram

14.7.2. Battery backup switchover related register

Table 44 Battery backup switchover related register

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
32h	Power Switch Control	CHGEN	INIEN	**z**	**z**	SWSEL1	SWSEL0	SMPT1	SMPT0

1) CHGEN bit (Charge Enable)

SW (V_{BAT} pin－V_{OUT} pin) automatic control

Table 45 CHGEN bit (Charge Enable)

CHGEN	Data	Description
Write / Read	0	MOS SW: OFF (Default setting) Recharge inactive
	1	MOS SW: automatic control Recharge active

To set CHGEN active User should set INIEN to "1".

2) INIEN bit (Initial Enable)

By setting INIEN to "1" automatic MOS SW control works and CHGEN bit control becomes available
When INIEN bit is "1", I^2C bus active/inactive control is available based on comparison result V_{DD} and V_{DET1}.

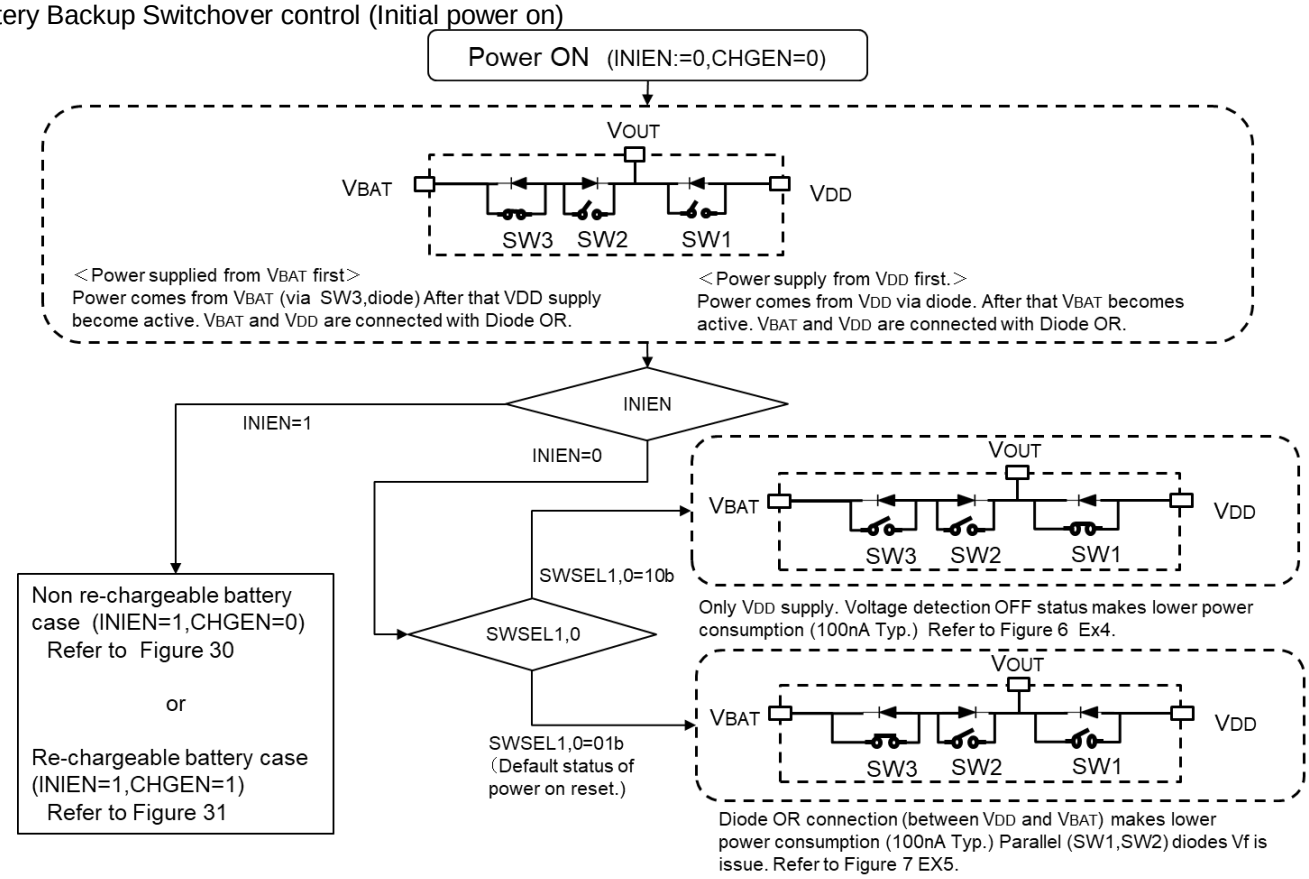
Table 46 INIEN bit (Initial Enable)

INIEN	Data	Description
Write / Read	0	MOS SW control inactive (Default setting)
	1	CHGEN bit setting become active. V_{DD} voltage low detection makes I^2C bus inactive and SDA,SCL become Hi-Z.

3) INIEN bit (Initial Enable)

This bit is used for enabling/disabling VLOW function as well as for controlling time stamp operation.
(Please refer to 14.8.6 for the detail)
Battery Backup Switchover control (Initial power on)

4) Battery Backup Switchover control (Initial power on)



Please refer 4. Connection Example. Figure6 and Figure7

Figure 27 Battery Backup Switchover Control (Initial power on)

5) Non re-chargeable battery control (INIEN: 1, CHGEN: 0)

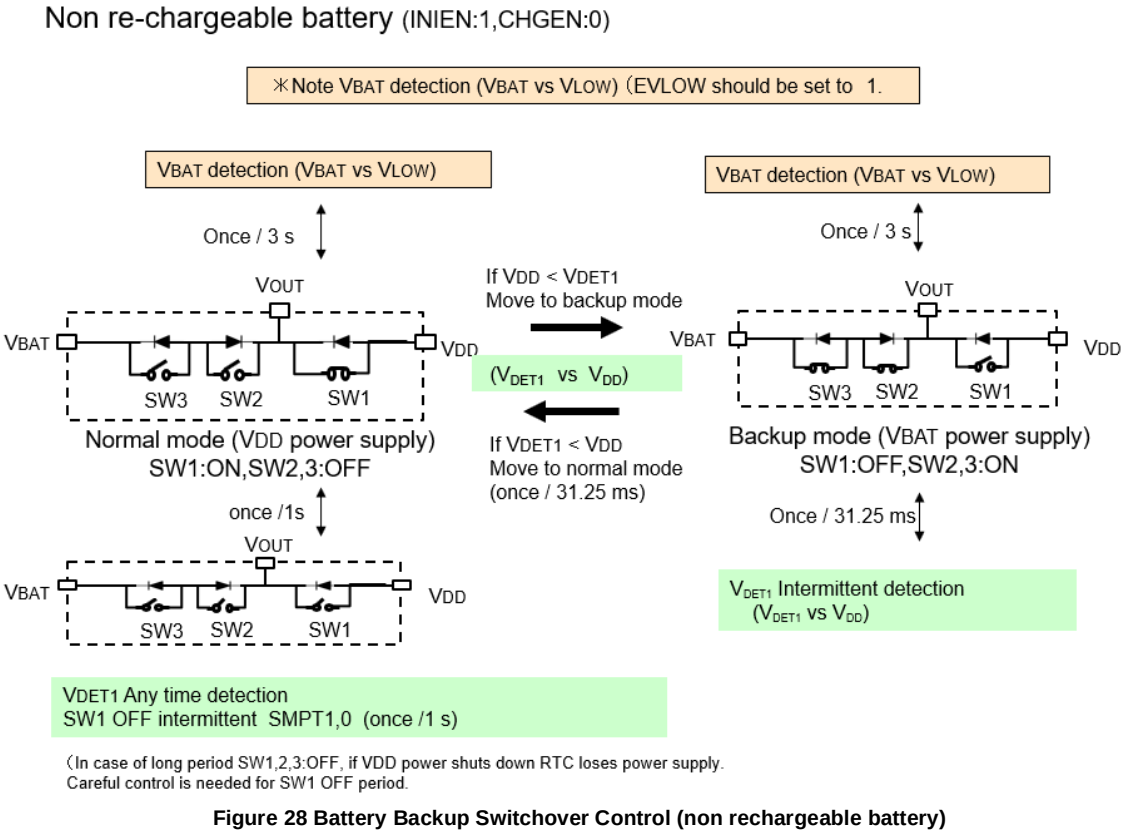


Figure 28 Battery Backup Switchover Control (non rechargeable battery)

6) Re-chargeable battery control (INIEN:1, CHGEN:1)

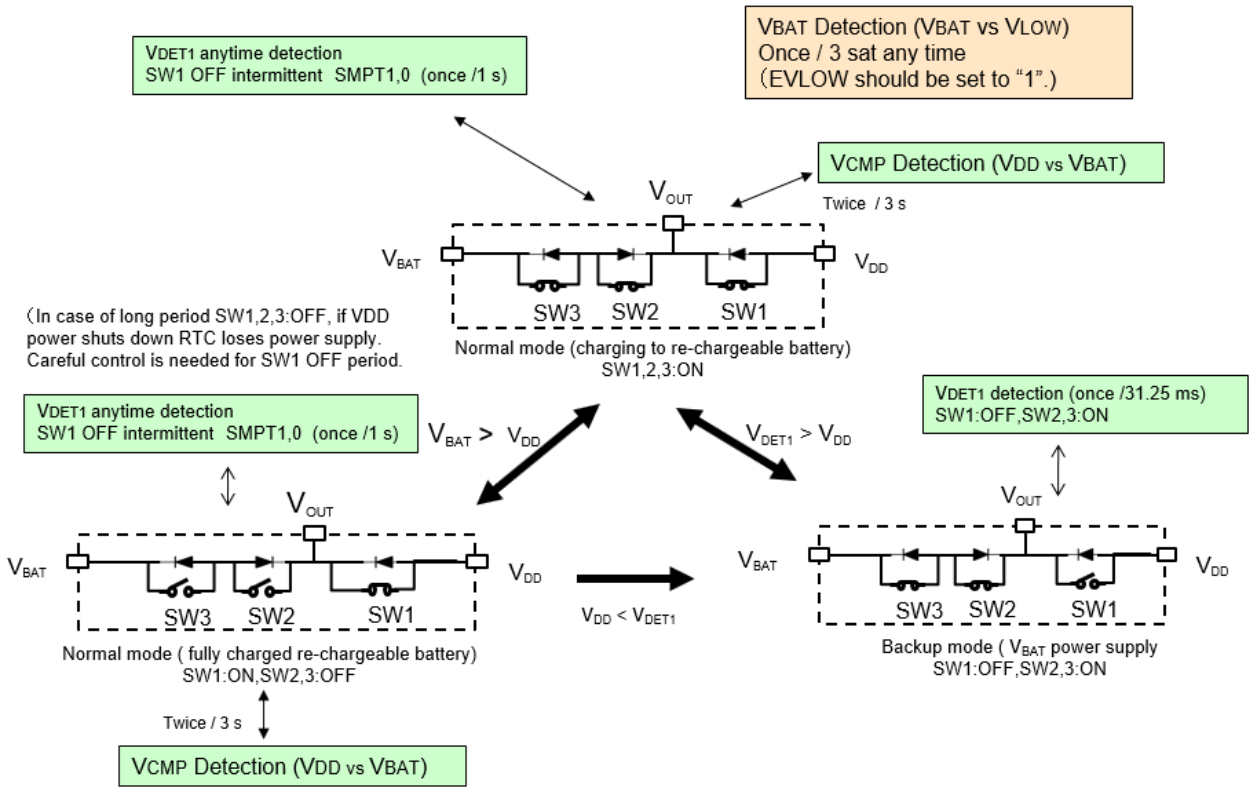


Figure 29 Battery Backup Switchover Control (rechargeable battery)

7) V_{DD} voltage detection register SMPT1, SMPT0 bit

Battery switchover functions managed by V_{DD} voltage low detection (V_{DET1}). This detection is checking voltage anytime with setting SW1(V_{DD}- ~ V_{OUT}) ON/OFF intermittently.

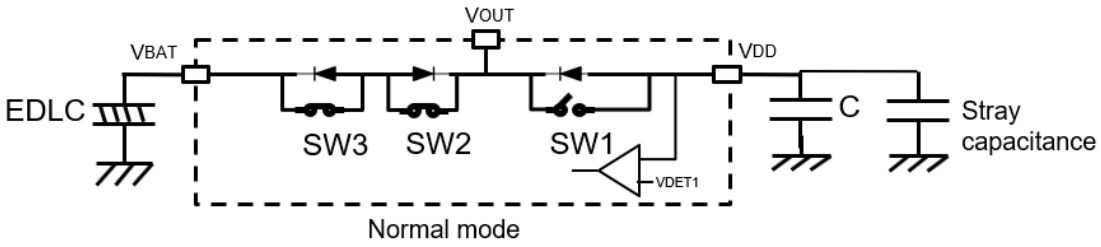
These two bits control SW1 OFF period and user can check much precision voltage by preventing reverse current from V_{BAT} to V_{DD} when main V_{DD} shuts down.

V_{DD} voltage low detection (V_{DET1}) is active anytime, so lower voltage detection moves RTC into backup mode immediately regardless SW1 OFF time.

These SW1 OFF occur every second.

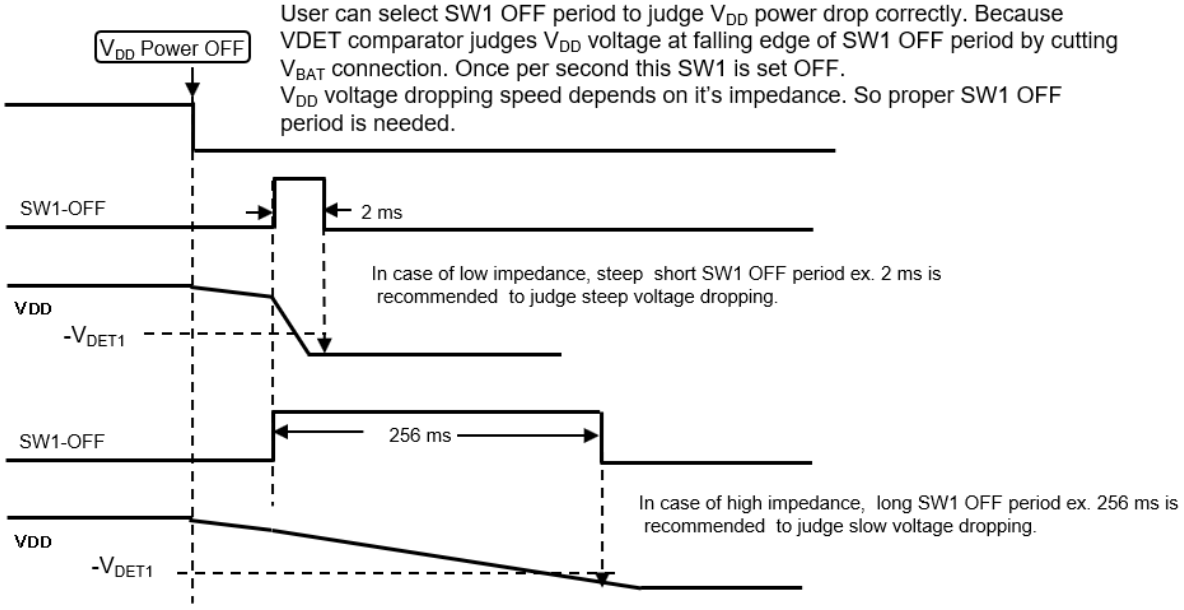
Table 47 SMPT bit (Sample Time)

SMPT1	SMPT 0	SW1 OFF period	remarks
0	0	Always ON	Default
0	1	2 ms	
1	0	128 ms	
1	1	256 ms	



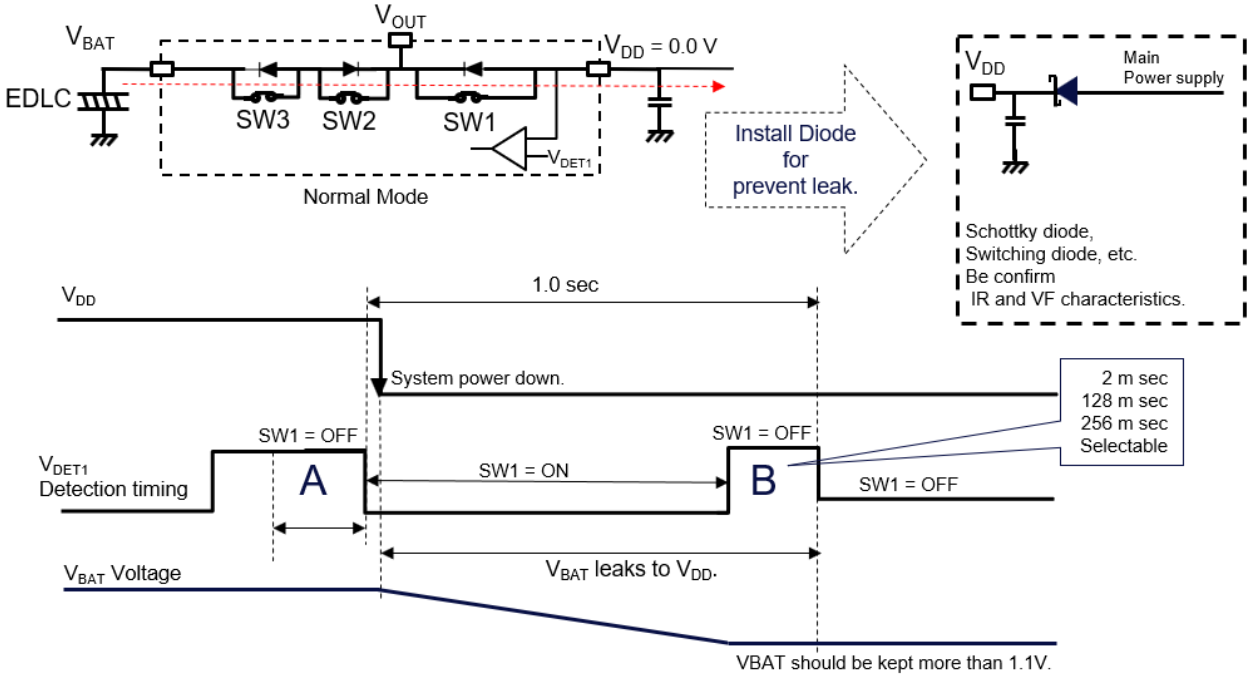
Normal mode

User can select SW1 OFF period to judge V_{DD} power drop correctly. Because VDET comparator judges V_{DD} voltage at falling edge of SW1 OFF period by cutting V_{BAT} connection. Once per second this SW1 is set OFF.
V_{DD} voltage dropping speed depends on it's impedance. So proper SW1 OFF period is needed.



Note in using small EDLC.

Careful management of the power management parameters is needed esp.
when using small EDLCs in combination with short voltage detection times (long SW ON).
In case V_{DD} drops quickly after a voltage detection period (A), there is a current flow from the EDLC into V_{DD}.
(red dotted line in the graph below) till the next detection period (B), which discharges the EDLC.
To avoid this discharge of the EDLC, it is recommended to insert a Diode as shown below.



8) Battery Backup Switchover related register SWSEL1, SWSEL0 bit

If user do not use switchover function (INIEN = 0), these two registers can fix MOS SW setting.

Table 48 Battery Backup Switchover SW register

INIEN	SWSEL1	SWSEL0	SW3	SW2	SW1	I^2C Bus	Remarks
0	0	1	ON	OFF	OFF	OFF	Default
	1	0	OFF	OFF	ON	OFF	
	0	0	ON	OFF	OFF	OFF	
1	1	1					Prohibited
	Other than (1,1)		Automatic control			ON	

9) Voltage detection intermittent timing

Table 49 Voltage detection timing

Power Supply	Normal mode			Backup mode
	V_{DD} drive (CHGEN=1, INIEN=1)	V_{DD} drive (CHGEN=0, INIEN=1)	V_{DD} drive (CHGEN=0, INIEN=0)	V_{BAT}drive
V_{DD} detection V_{DET1}	anytime	anytime	suspended	Once a 31.25 ms
V_{DD} vs V_{BAT} V_{CMP}	Twice a 3.0 s	suspended	suspended	Suspended
V_{BAT} detection V_{LOW}	Once a 3.0 s	once a 3.0 s	once a 3.0 s	Once a 3.0 s

V_{LOW} If results (continuous 2 times) are same, that is reflected to V_{LOW}.

14.8. Time Stamp Function

14.8.1. Outline of Time Stamp function

There are three factors for time stamp operation

1) EVIN pin signal detection
2) RTC internal status detection
3) Command trigger by I^2C read command (2Fh reading)

Time stamp events are recoded into RAM up to maximum of 8 times. (Refer to Figure 31)
/INT pin interrupt output is available when time stamp event occurs. These operation can also work in backup mode. RTC internal status can be recorded while stamp record ,time (1/128 sec, SEC, MIN, HOUR, DAY, MONTH, YEAR, Status Stamp）.

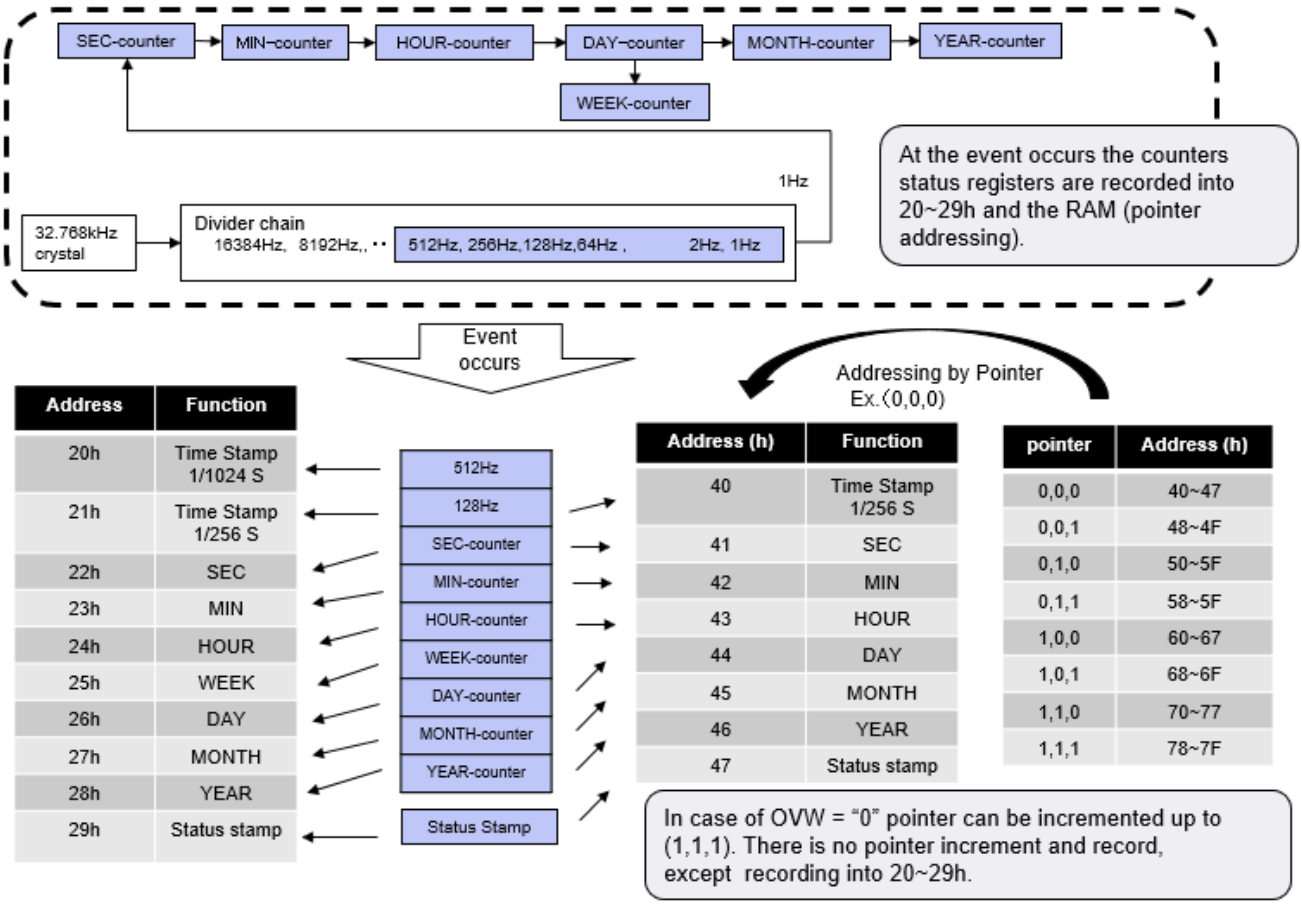


Figure 31 Time Stamp function

14.8.2. Time Stamp related register

Table 50 Time Stamp function register

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1Dh	Extension Register	FSEL1	FSEL0	USEL	TE	WADA	**ETS**	TSEL1	TSEL0
1Eh	Flag Register	POR	**z**	UF	TF	AF	**EVF**	VLF	XST
1Fh	Control Register	**z**	**z**	UIE	TIE	AIE	**EIE**	**z**	STOP
2Bh	EVIN Setting	**EHL**	**ET1**	**ET0**	**PDN**	**PU1**	**PU0**	**OVW**	**-**
2Eh	Command Tigger control	**z**	**z**	**z**	**z**	**z**	**z**	**z**	**COMTG**
2Fh	Command Trigger	**z**	**z**	**z**	**z**	**z**	**z**	**z**	**z**
34h	Time Stamp Control 1	**z**	**z**	**z**	**z**	**z**	**EISEL**	**TSCLR**	**TSRAM**
35h	Time Stamp Control 2	**●**	**z**	**z**	**z**	**ECMP**	**EVDET**	**EVLOW**	**EXST**
36h	Time Stamp Control 3	**z**	**z**	**z**	**TSFUL**	**TSEMP**	**TSAD2**	**TSAD1**	**TSAD0**

14.8.3. Time stamp function triggered by EVIN pin input

Following registers control time stamp function triggered by EVIN pin input.

1) ETS bit (Enable Time Stamp)

This register controls time stamp (triggered by EVIN pin input) ON/OFF. Also, user can use chattering prevention function. User should be aware that chattering prevention results in the worse resolution. (refer to ET1, ET0bit.)

Table 51 ETS bit (Enable Time Stamp)

ETS	Data	Description
Write / Read	0	Time Stamp function OFF
	1	Time Stamp function ON

Refer to RTC internal status trigger time stamp function registers respectively.

2) EVF bit (Event Flag)

This register is be set to “1” when event occurs.

Table 52 EVF bit (Event Flag)

EVF	Data	Description
Write	0	In case /INT: ”L” output, it is set to Hi-Z.
	1	Invalid (writing “1” will be ignored)
Read	0	–
	1	EVIN input is detected. The result remains until clearing to “0”.

3) EIE bit (Event Interrupt Enable)

This register control /INT interrupt output at the moment of the event (EVF, "0" → "1").

Table 53 EIE bit (Event Interrupt Enable)

EIE	Data	Description
Write	0	1) No /INT interrupt output (/INT = Hi-Z) 2) Releasing /INT interrupt output (/INT = "L" → Hi-Z)
	1	/INT interrupt output (/INT = Hi-Z → " L")

4) EHL bit (EVIN High/Low)

This register controls EVIN input voltage level.
Longer EVIN input than chattering prevention cycle is detected.

Table 54 EHL bit (EVIN High/Low)

EHL	Data	Description
Write / Read	0	Triggered by Low level voltage
	1	Triggered by High level voltage

5) ET1, ET0 bit

These bits select chattering filter period of input from EVIN.

Table 55 ET bit selection

ET1 (bit 6)	ET0 (bit 5)	cycle	When EVIN chattering filter function is used, correct data of sub seconds is not stored in following register bits.
0	0	No chattering filter. *1	All sub seconds data are valid.
0	1	3.9 ms (256 Hz)	1 / 1024 s Bit 0 of 20h.
1	0	15.6 ms(64 Hz)	1 / 1024 s Bit0,1 of 20h. 1 / 256 s Bit 0 of 21h. 1 / 256 s Bit 0 of 40h, 50h, 60h, 70h, 48h, 58h, 68h, 78h.
1	1	125 ms (8 Hz)	1 / 1024 s Bit0, 1, 2, 3, of 20h. 1 / 256 s Bit0 of 21h 1 / 256 s Bit 0, 1, 2, 3 of 40h, 50h, 60h, 70f, 48h, 58h, 68h, 78h.

No chattering filter. EVIN detection is done with approximate 1 μs.

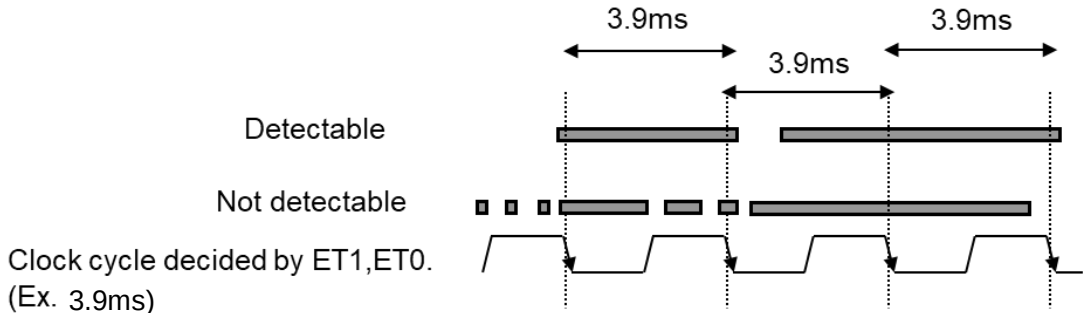


Figure 32 EVIN chattering prevention function

6) PDN,PU1,PU0 bit (Pull Down Select, Pull Up Select)

These registers controls EVIN pin input internal Pull-up/Pull-down resistor value.
Pull-up resistor is connected to V_{OUT}, Pull-down resistor to GND.

Table 56 PDN,PU register (Pull Down Select, Pull Up Select)

Condition	PDN	PU1	RU0	Resistor value, status
No connection	0	0	0	Hi-Z
Pull-up	0	0	1	500 kΩ
	0	1	0	1 MΩ
	0	1	1	10 MΩ
Pull-down	1	0	0	500 kΩ
No connection	1	1	0	Don't select these combinations. EVIN changed to Hi-Z.
	1	0	1	
	1	1	1	

7) OVW bit (Over Write)

This register controls time stamp update.

Table 57 OVW bit (Over Write)

OVW	Data	Description
Write	0	Time stamp records 8 times, then no more time stamp update. Pointer moves from pointer(0,0,0) → pointer(0,0,1) - - - → pointer(1,1,1) and stops
	1	Time stamp records more than 8 times continuously. pointer(0,0,0) → pointer(0,0,1) - - - → pointer(1,1,1) → pointer(0,0,0) - - →

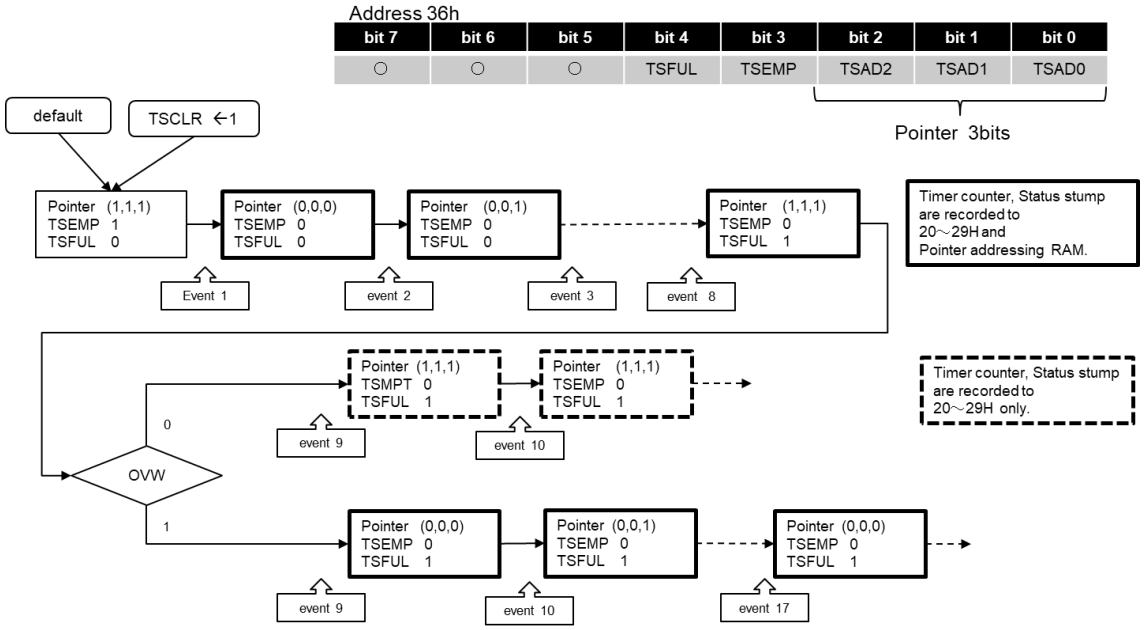


Figure 33 Operation of OVW, pointer

14.8.4. Time stamp function triggered by I²C access

An I²C access can trigger time stamp too.

1) COMTG bit

This register control Time stamp trigger by I²C access ON/OFF.

Table 58 COMTG bit (Command Trigger)

COMTG	Data	Description
Write	0	Time stamp trigger by I²C-Bus OFF
	1	Time stamp trigger by I²C-Bus ON RTC timer counter and internal status data are recorded into 20h~29h by I²C reading access from 2Fh. The read data of 2Fh is 00h. Also, multi access is available.

2) Time stamp access timing

Time stamp processing is done at ACK operation just after slave address sending (of command trigger reading).

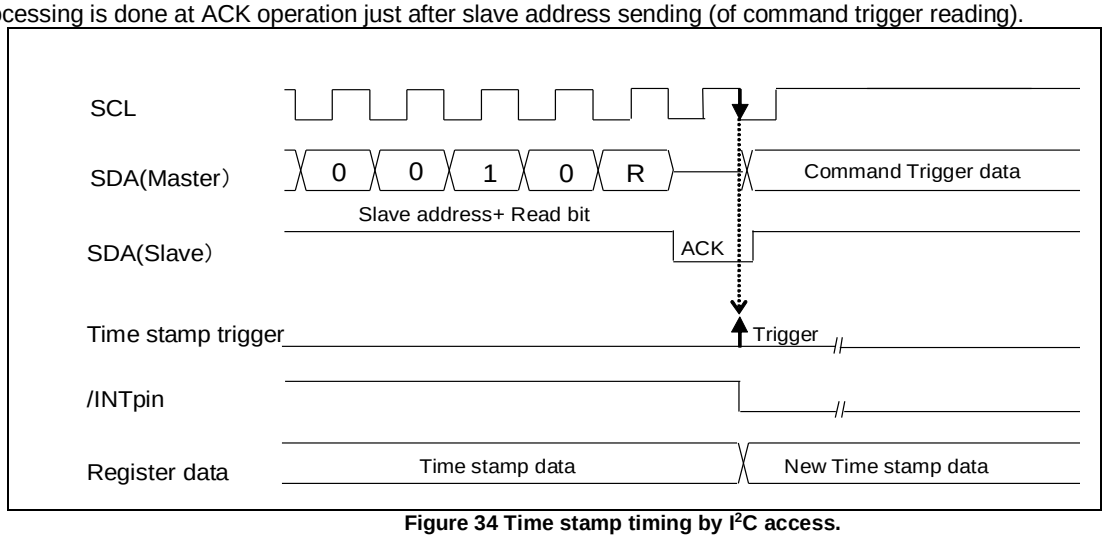
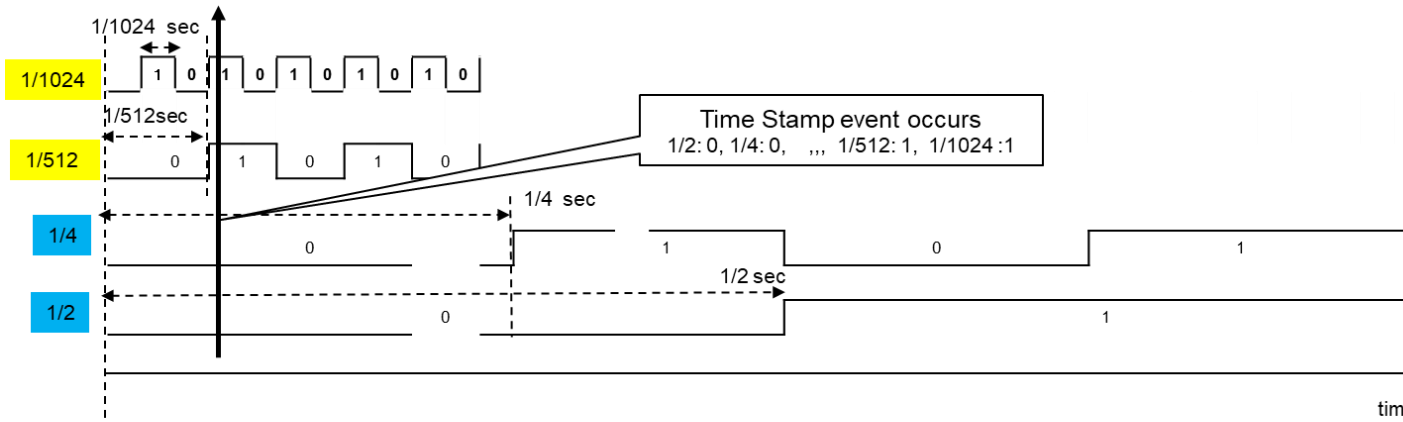
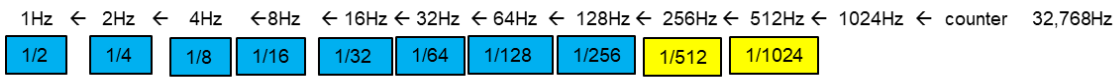


Figure 34 Time stamp timing by I²C access.

14.8.5. Time stamp stored register

At time stamp event occurs, following data is recorded. Refer to Figure 35
Note: In case of multiple time stamps, please refer to 14.8.6





address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
20h	--	--	--	--	--	--	1/512	1/1024
21h	1/2	1/4	1/8	1/16	1/32	1/64	1/128	1/256

address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Pointer address	1/2	1/4	1/8	1/16	1/32	1/64	1/128	1/256

Figure 35 Time stamp stored register (1/1024 s ~ 1 s)

Table 59 Time stamp stored register

Address	Function	Time stamp record
20h	Time Stamp 1/1024Sec	256 Hz, 512 Hz,
21h	Time Stamp 1/256Sec	1 Hz ~ 128 Hz
22h	Time Stamp Sec	sec
23h	Time Stamp Min	min
24h	Time Stamp Hour	hour
25h	Time Stamp Week	week
26h	Time Stamp Day	day
27h	Time Stamp Month	month
28h	Time Stamp Year	year
29h	Status Stamp	RTC internal status

Table 60 Status Stamp

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
29h	Status Stamp	z	z	VLOW	VCMP	VDET	z	XST	z

1) VLOW bit (Time Stamp VLOW)
This bit records the comparison result of V_{BAT} vs V_{LOW} at the moment of event.

Table 61 VLOW bit (Time Stamp VLOW)

VLOW	Data	Description
Read	0	$V_{BAT} > V_{LOW}$
	1	$V_{BAT} < V_{LOW}$

2) VCMP bit (Time Stamp VCMP)
This bit records the comparison result of V_{DD} vs V_{BAT} (VCMP status) at the moment of event.

Table 62 VCMP bit (Time Stamp VCMP)

VCMP	Data	Description
Read	0	$V_{DD} > V_{BAT}$
	1	$V_{DD} < V_{BAT}$

3) VDET bit (Time Stamp VDET)
This bit records the comparison result of V_{DD} vs V_{DET1} at the moment of event.

Table 63 VDET bit (Time Stamp VDET)

4) XST bit (Time Stamp X'tal Oscillation Stop)
This bit records either internal Crystal oscillation stop or not stop at the moment of event.

Table 64 **XST bit (Time Stamp X'tal Oscillation Stop)**

XST	Data	Description
Read	0	Normal Internal Crystal oscillation
	1	Internal Crystal oscillation stops

14.8.6. RTC internal event triggered time stamp, multiple times stamp

In addition to EVIN pin input triggered , the RTC time stamp can be triggered by internal event.
Also, time stamp events are continuously recoded into RAM up to maximum 8 times.
To avoid unwanted timestamp event, ETS register should be reset to 0 before reading time stamp data (2hf ~ 29h, 40h ~ 47h).
(Refer to Figure36)

Table 65 Related register for internal event triggered time stamp, multiple times stamp

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
34h	Time Stamp Control 1	z	z	z	z	z	EISEL	TSCLR	TSRAM
35h	Time Stamp Control 2	●	z	z	z	ECMP	EDET	EVLOW	EXST
36h	Time Stamp Control 3	z	z	z	TSFUL	TSEMP	TSAD2	TSAD1	TSAD0

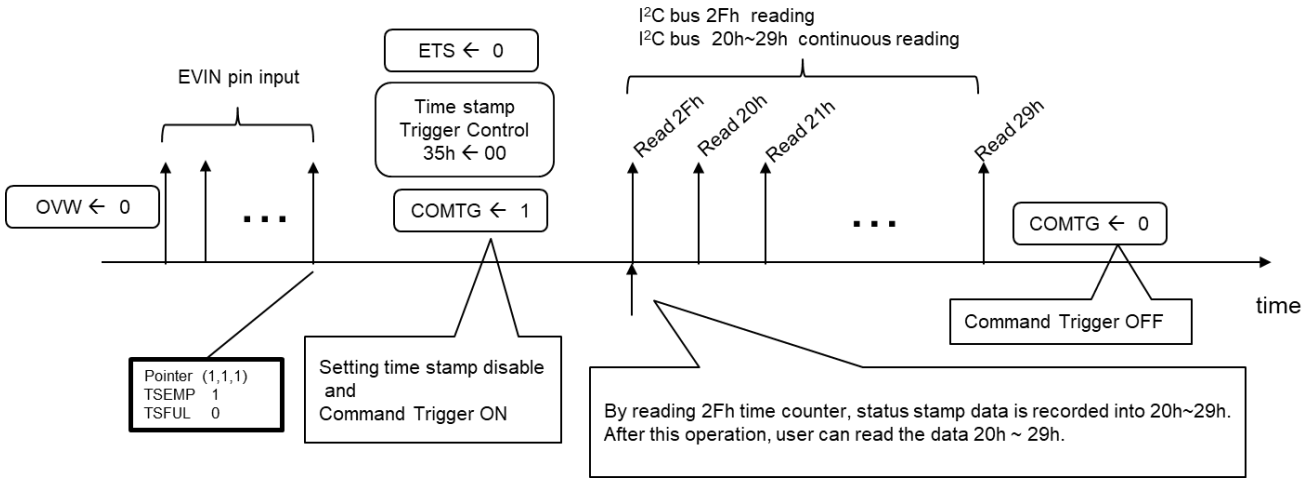


Figure 36 Avoiding EVIN pin input event, user read time stamp data.

(1) Time stamp by self monitor detection of RTC

1) ECMP bit (Enable VCMP)

This bit controls time stamp (VCMP) ON/OFF.

Table 66 ECMP bit (Enable VCMP)

ECMP	Data	Description
Write	0	No time stamp event even VCMP is detected.
	1	Time stamp event occurs. When $V_{BAT} > V_{DD}$ becomes true, under condition of charging to re-chargeable battery.

2) EVDET bit (Enable VDET)

This bit controls time stamp (VDET) ON/OFF.

When user set EVDET to "1", at least 31.25m sec time interval is needed after INIEN setting to "1". If user cannot set 31.25 ms interval, unreliable result will be obtained, in such case please ignore the result data. Also, if user used fixed SW combination, don't use this register. Refer to Figure 38

Table 67 EVDET bit (Enable VDET)

EVDET	Data	Description
Write	0	No time stamp event even V_{DET1} is detected.
	1	When RTC moves to backup mode, time stamp event occurs.

3) EVLOW bit (Enable VLOW)

This bit controls VLOW detection ON/OFF and time stamp (VLOW) ON/OFF. A common register for VLOW function and time stamp.

Table 68 EVLOW bit (Enable VLOW)

EVLOW	Data	Description
Write	0	No time stamp event and no VLOW detection.
	1	VLOW detection and time stamp event when VLOW is detected.

4) EXST bit (Enable X'tal Oscillation Stop)

This bit control time stamp (XST) trigger ON/OFF

Table 69 EXST bit (Enable X'tal Oscillation Stop)

EXST	Data	Description
Write	0	No time stamp event even when internal crystal oscillation stops.
	1	Time stamp event occurs when crystal oscillation stop is detected.

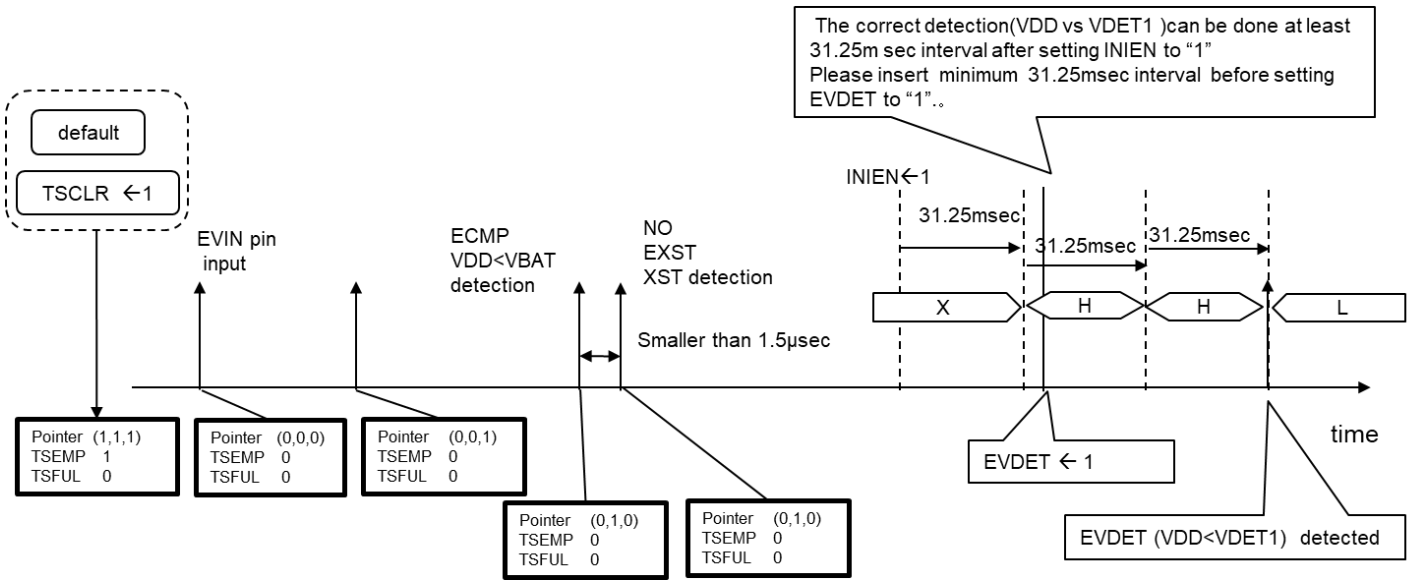


Figure 37 Careful timing process when RTC internal status trigger is used for time stamp

(2) Multiple time stamp is available with following registers management.
The record area (40h ~ 7Fh) all the time stamp is recorded except 1/1024 sec, WEEK.

1) TSRAM bit
This bit control RAM (40h~7Fh) the usage time stamp recording or normal RAM.

Table 70 TSRAM bit (Time Stamp Clear)

TSRAM	Data	Description
Write	0	40h~7Fh is used a normal (Read/Write enable) Time stamp data is recorded into 20h-28h at event timing.
	1	40h~7Fh is used a time stamp recording memory. (Read/Write enable) User can modify directly RAM data via I^2C if necessary.

2) TSCLR bit (Time Stamp Clear)
The operation of writing "1" to this bit makes address 36h clear to initialize and this bit be reset to "0" automatically.
Time stamp function should be disenabled by resetting ETS to "0" before this operation (Time stamp clear).

Table 71 TSCLR bit (Time Stamp Clear)

TSCLR	Data	Description
Write	0	Invalid (writing "0" will be ignored)
	1	Initializing address 36h register. TSFUL: 0, TSEMP: 1 TSAD2: 1, TSAD1: 1, TSAD0: 1 pointer (1,1,1)

3) EISEL bit (Event Interrupt Select)
This bit controls time stamp event interrupt selection.

Table 72 EISEL bit (Event Interrupt Select)

EISEL	Data	Description
Write	0	Every time stamp event triggering makes interrupt output.
	1	In case of 8 times record (of time stamp) interrupt output occurs.

(3) Multiple time stamp recording function

1) TSFUL bit (Time Stamp Full)
This bit is reflected by 8 times time stamp recording.

Table 73 TSFUL bit (Time Stamp Full)

TSFUL	Data	Description
Read	0	There is (are) empty RAM area.
	1	RAM area is fully occupied by 8 times time stamp recording.

2) TSEMP bit (Time Stamp Empty)
This bit is monitor bit of RAM empty.

Table 74 TSEMP bit (Time Stamp Empty)

TSEMP	Data	Description
Read	0	There is some data recording in the RAM area (40h ~ 7fh).
	1	There is no data recording in the RAM area (40h ~ 7fh).

3) TSAD2, TSAD1, TSAD0bit (Time Stamp Address)
This bits are monitor register of the latest time stamp RAM address.

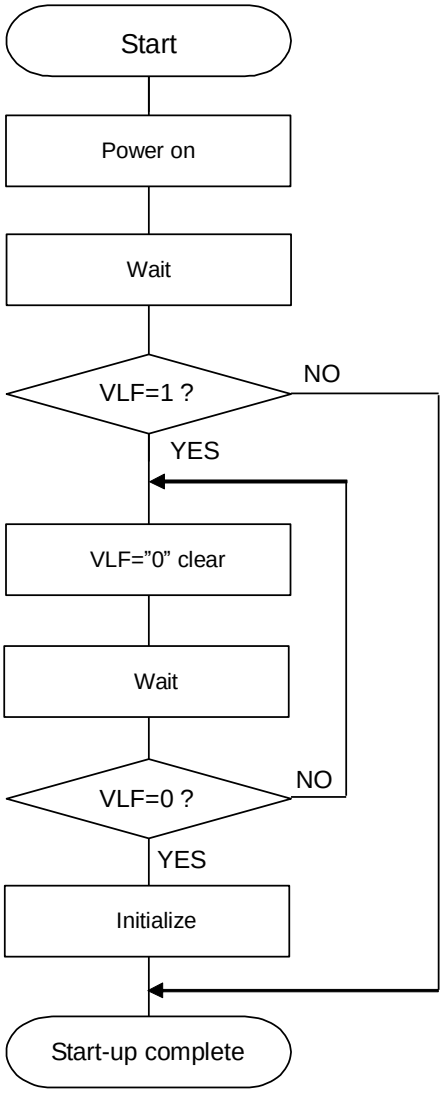
Table 75 TSDA bit (Time Stamp Address)

TSAD	TSAD2	TSAD1	TSAD0	Address pointer
Read	0	0	0	40h-47h
	0	0	1	48h-4Fh
	0	1	0	50h-57h
	0	1	1	58h-5Fh
	1	0	0	60h-67h
	1	0	1	68h-6Fh
	1	1	0	70h-77h
	1	1	1	78h-7F, default

14.9. Flow Chart

Below are examples of flow charts, but they are not necessarily applicable for every use-case and not necessarily the most effective process for individual applications. For effective processing, user can do multiple execution, change ordering, eliminate execution etc.
These flow should be optimization for suitable in each of system.

1) Power on initializing example



- At least 40 ms wait time is needed.
  So that it is stable RTC.
  40 ms is not oscillation startup time.

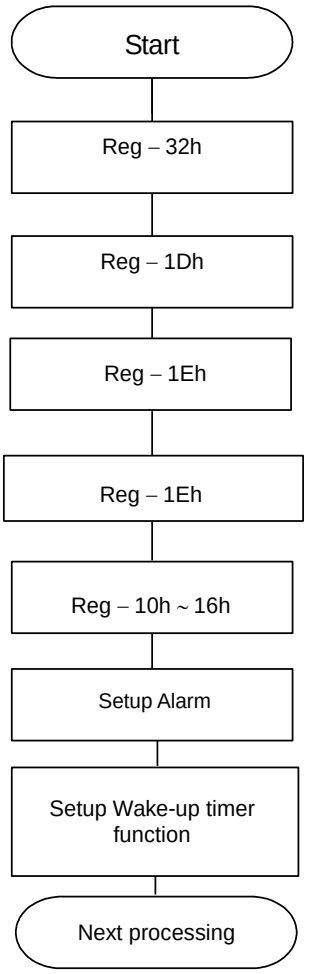
- When RTC returned from battery backup normally, VLF is 0. and after initial power On, VLF is 1.
- When VLF is 1, recommended initializing all register data.

- After internal oscillation start VLF can be cleared to "0".

- Waiting suitable time, in each of system.
  more than 300 ms is recommended

Figure 38 Example flow (power on initialization)

2) Initialization Ex1



- Setup of battery backup switchover function.
- Setup Timer function.
- Clear self monitoring Bits.
- Setup interruption output
- writes time and date.
- Setup Alarm function.
- Setup Wakeup Timer function.

Figure 39 Example flow (Initialization EX1)

3) Initialization Ex2 (only clock usage)

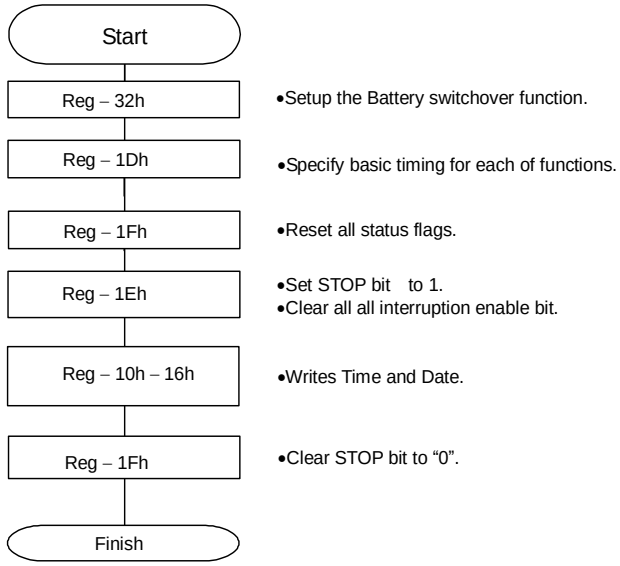


Figure 40 Example flow (Initialization Ex2 only clock usage)

4) Setup Clock and calendar example

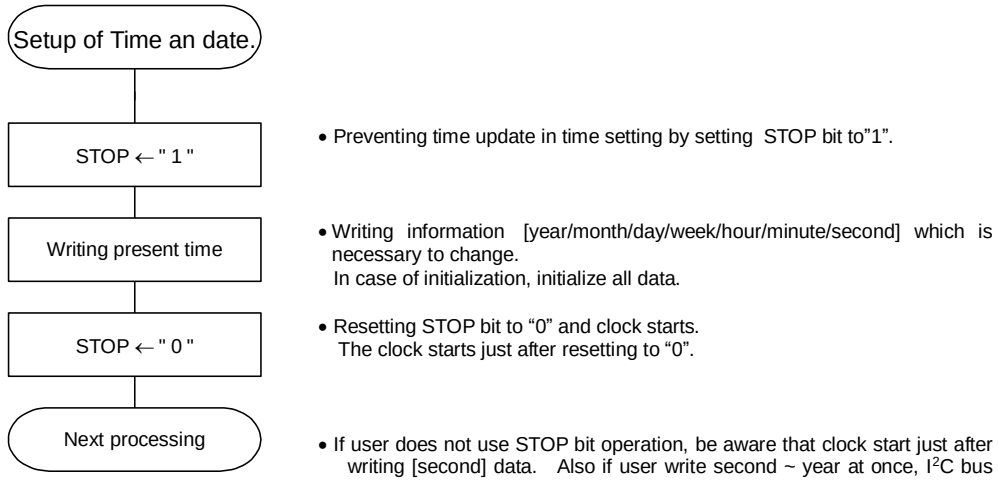


Figure 41 Example flow (Setting clock, calendar)

5) Reading clock, calendar example

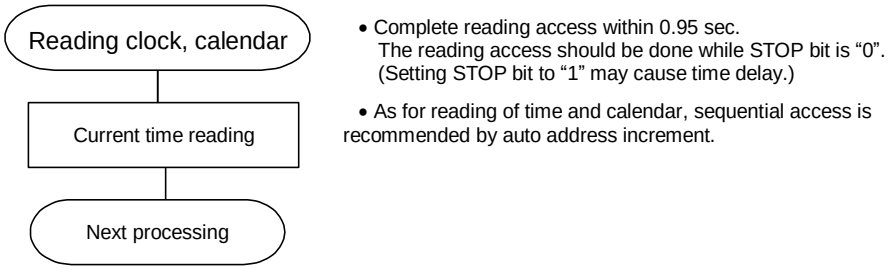
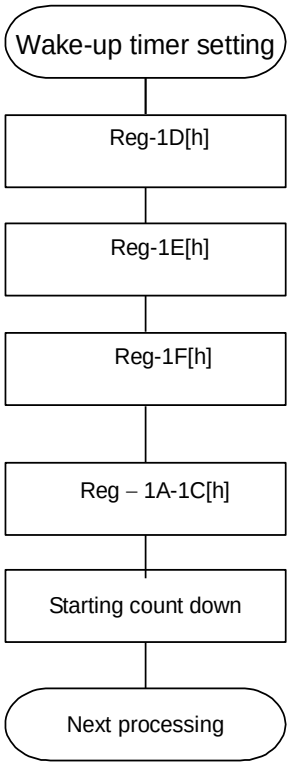


Figure 42 Example flow (Reading clock, calendar)

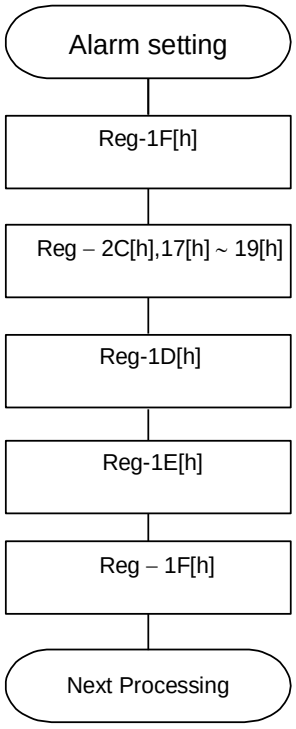
6) Setting wake-up timer interpunction example



- Clear TE bit to “0” to inactivate wake-up timer interruption.
- Set TSEL1, TSEL0 bit combination to count down period (source clock).
- Clear the TF-bit by zero.
- Set TIE to "1", for interruption output from INT-pin.
- write initial data to the Down counter.
- Set TE bit to “1” to start wake-up timer counter.
  Be aware that initial data should be pre-set to counter before starting.
- While TSTP is "1", timer countdown doesn't occur.
  When TSTP clears by 0, The Countdown timer works again.
  TSTP is useful for working time counter of machine, etc.

Figure 43 Example flow (Setting wake-up timer interrupt function)

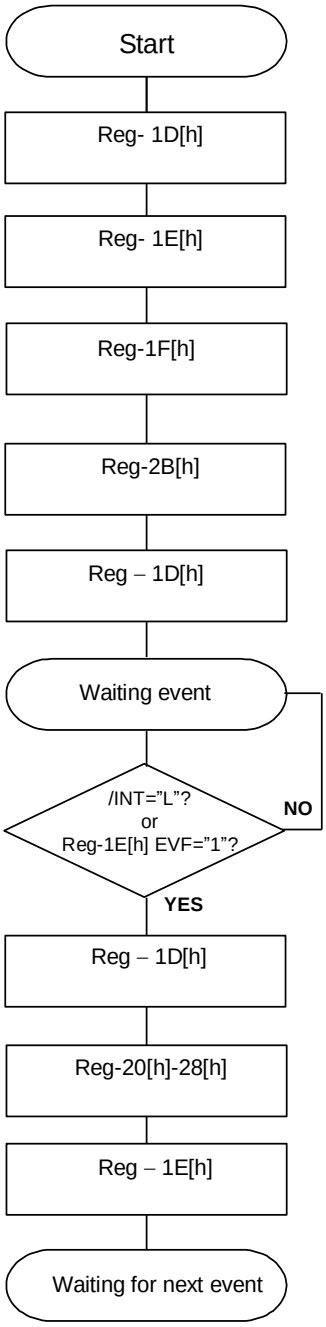
7) Setting Alarm Example



- Reset AIE bit to “0” to inactivate alarm interruption.
- Setup Alarm data.
- Specify week alarm or day alarm, by WADA bit.
- Clear AF-bit by "0".
- Set AIE bit to “1”, for outputs Alarm interruption from INT-pin.

Figure 44 Example flow (Setting alarm interrupt function)

8) Time stamp (one time recording) Example



- Clear ETS bit by "0" to inactivate time stamp function.
- Clear EVF bit by"0".
- Set EIE bit to "1" to activate time stamp interrupt function.
  An event makes /INT pin interruption output.
- Setup EVIN pin input pull-up/pull-down resistor combination.
- Set ETS bit to "1" to activate time stamp function.
- When event occurs EVF bit is set to "1", /INT pin becomes low as interrupt output.
- Reset ETS bit to "0" to inactivate time stamp function.
  The reason is to avoid unwanted time stamp during data reading.
- Reading time stamp data of event occur.
- Clears EVF bit to "0".

Figure 45 Example flow (Time stamp (one time recording))

9) Time stamp (1/1028 sec to 1/128 sec reading) Example

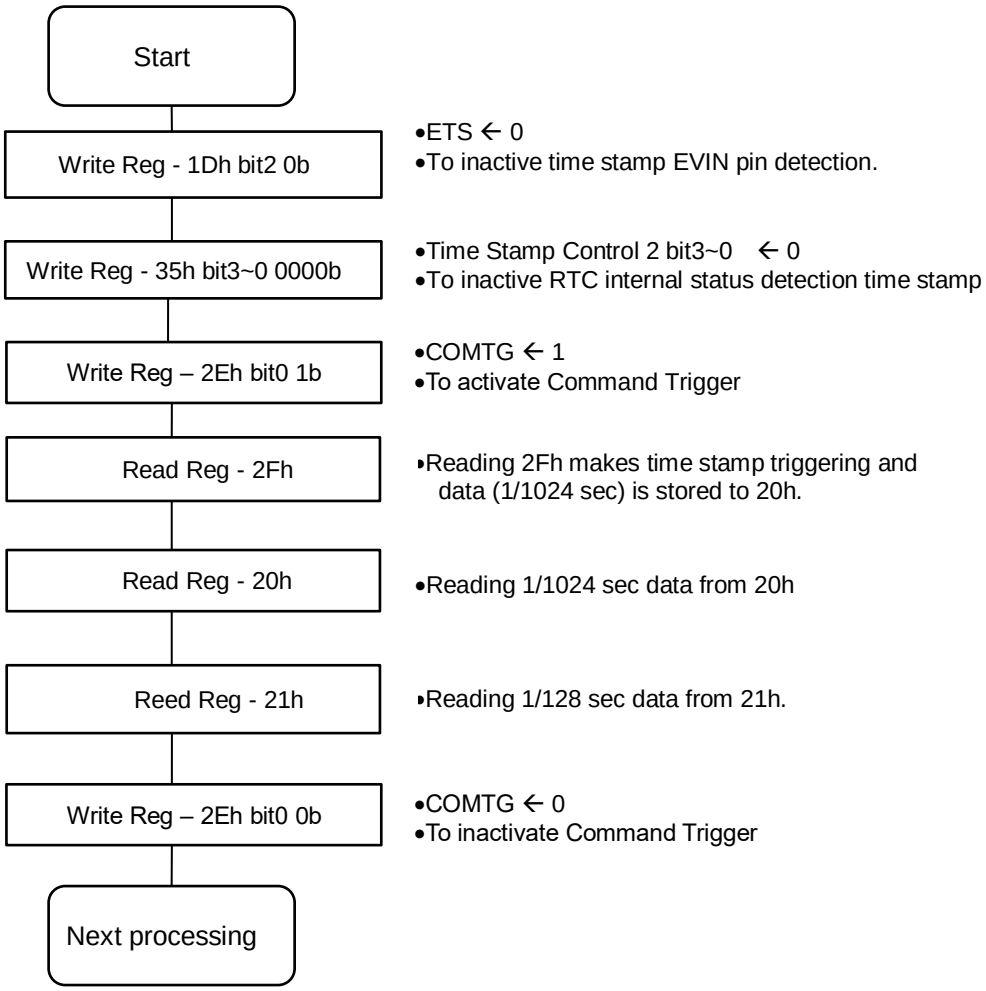


Figure 46 Example flow (Time stamp (1/1024 sec, 1/128 sec reading))

10) Time stamp (Year to 1/128 sec reading) Example

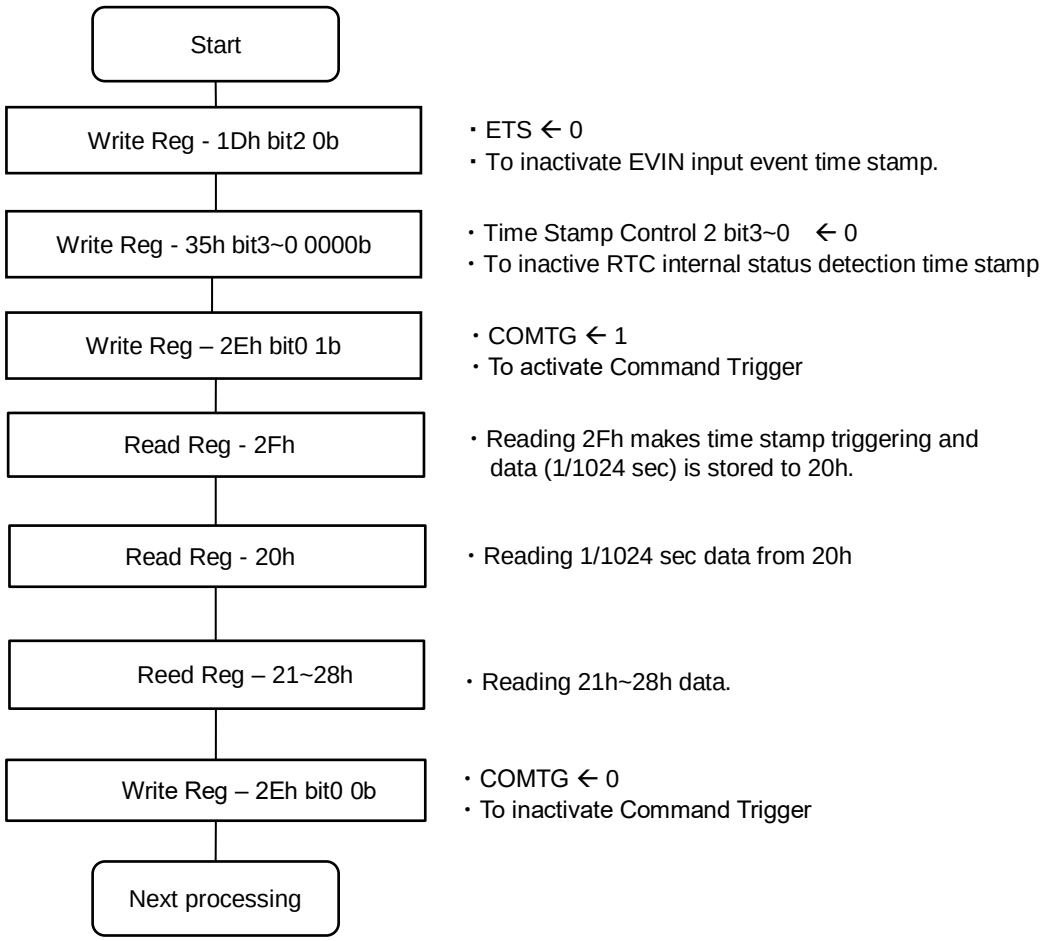


Figure 47 Example flow (Time stamp (Year to 1/128 data reading))

14.10. Reading/Writing Data via the I²C-Bus Interface

14.10.1. Overview of I²C-Bus

The I²C-Bus supports bi-directional communications via two signal lines: the SDA (data) line and SCL (clock) line. A combination of these two signals is used to transmit and receive communication start/stop signals, data transfer signals, acknowledge signals, and so on.

Both the SCL and SDA signals are held at high level whenever communications are not being performed.
The starting and stopping of communications is controlled at the rising edge or falling edge of SDA while SCL is at high level.

14.10.2. Data transfers

Data transfers are performed in 8-bit (1 byte) units once the START condition has occurred. There is no limit on the amount (bytes) of data that are transferred between the START condition and STOP condition.
(However, the transfer time must be no longer than 0.95 seconds.)

14.10.3. Starting and stopping I²C-Bus communications

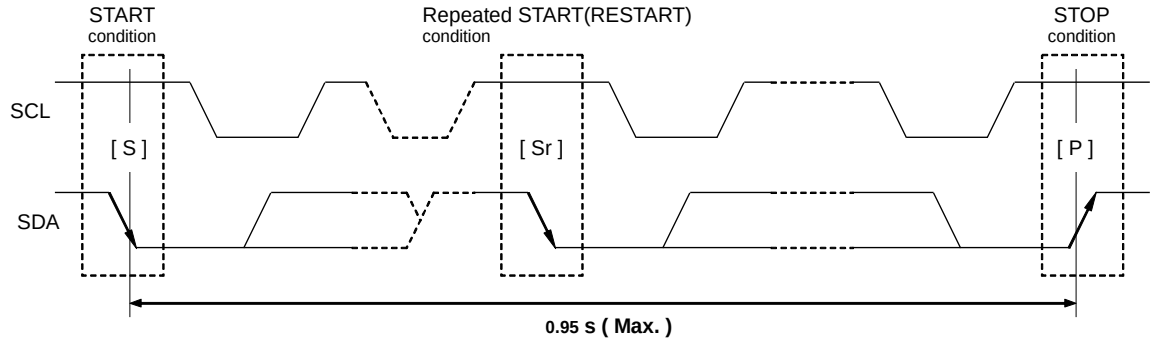


Figure 48 I²C-Bus start/stop timing

START condition, repeated START condition, and STOP condition

(1) START condition
The SDA level changes from high to low while SCL is at high level.

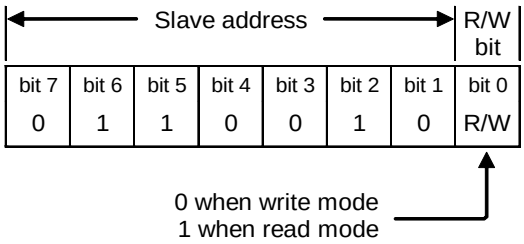
(2) STOP condition
This condition regulates how communications on the I²C-Bus are terminated.
The SDA level changes from low to high while SCL is at high level.

(3) Repeated START condition (RESTART condition)
In some cases, the START condition occurs between a previous START condition and the next STOP condition, in which case the second START condition is distinguished as a RESTART condition. Since the required status is the same as for the START condition, the SDA level changes from high to low while SCL is at high level.

When accessing this device, all communication from transmitting the start condition to transmitting the stop condition after access should be completed within 0.95 seconds. If communication requires 0.95 seconds or longer, the I²C-Bus interface is reset by the internal Bus timeout function.

14.10.4. Slave address

The I²C-Bus devices do not have any chip select or chip enable pins. All I²C-Bus devices are memorized with a fixed unique number in it. The chip selection on the I²C-Bus is executed, when the interface starts, the master device sends the required slave address to all devices on the I²C-Bus. The receiving device only reacts for interfacing, when the required slave address is agreed with its own slave address.
During in actual data transmission, the transmitted data contains the slave address and the data with R/W (read/write) bit.



14.10.5. System configuration

All ports connected to the I²C-Bus must be either open drain or open collector ports in order to enable AND connections to multiple devices.
SCL and SDA are both connected to the VIO line via a pull-up resistance. Consequently, SCL and SDA are both held at high level when the Bus is released (when communication is not being performed).

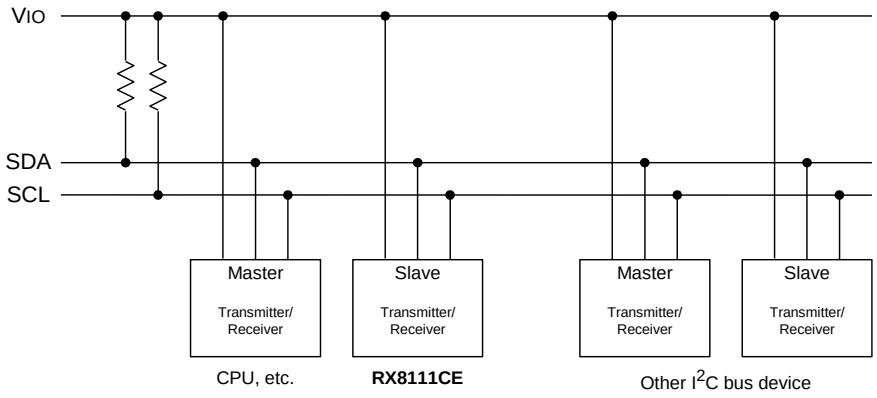


Figure 49 I²C-Bus connection

Any device that controls the data transmission and data reception is defined as a "Master".
and any device that is controlled by a master device is defined as a “Slave”.
The device transmitting data is defined as a “Transmitter” and the device receiving data is defined as a receiver”

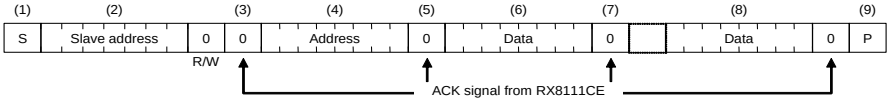
In the case of this RTC module, controllers such as a CPU are defined as master devices and the RTC module is defined as a slave device. When a device is used for both transmitting and receiving data, it is defined as either a transmitter or receiver depending on these conditions.

14.10.6. I²C-Bus protocol

In the following sequence descriptions, it is assumed that the CPU is the master and the RX8111CE is the slave.
Address specification write sequence
Since the RX8111CE includes an address auto increment function, once the initial address has been specified, the RX8111CE increments (by one byte) the receive address each time data is transferred.

Address circulation of auto increment function.	10h -> 1Fh -> 10h
	20h -> 2Fh -> 20h
	30h -> 3Fh -> 30h

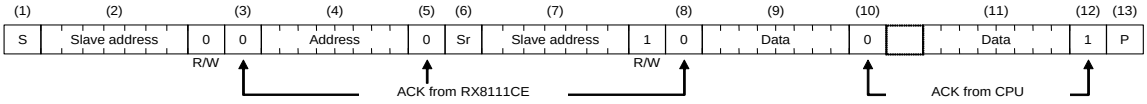
(1) CPU transfers start condition [S].
(2) CPU transmits the RX8111CE's slave address with the R/W bit set to write mode.
(3) Check for ACK signal from RX8111CE.
(4) CPU transmits write address to RX8111CE.
(5) Check for ACK signal from RX8111CE.
(6) CPU transfers write data to the address specified at (4) above.
(7) Check for ACK signal from RX8111CE.
(8) Repeat (6) and (7) if necessary. Addresses are automatically incremented.
(9) CPU transfers stop condition [P].



2) Address specification read sequence

After using write mode to write the address to be read, set read mode to read the actual data.

(1) CPU transfers start condition [S].
(2) CPU transmits the RX8111CE's slave address with the R/W bit set to write mode.
(3) Check for ACK signal from RX8111CE.
(4) CPU transfers address for reading from RX8111CE.
(5) Check for ACK signal from RX8111CE.
(6) CPU transfers RESTART condition [Sr] (in which case, CPU does not transfer a STOP condition [P]).
(7) CPU transfers RX8111CE's slave address with the R/W bit set to read mode.
(8) Check for ACK signal from RX8111CE (from this point on, the CPU is the receiver and the RX8111CE is the transmitter).
(9) Data from address specified at (4) above is output by the RX8111CE.
(10) CPU transfers ACK signal to RX8111CE.
(11) Repeat (9) and (10) if necessary. Read addresses are automatically incremented.
(12) CPU transfers ACK signal for "1".
(13) CPU transfers stop condition [P].

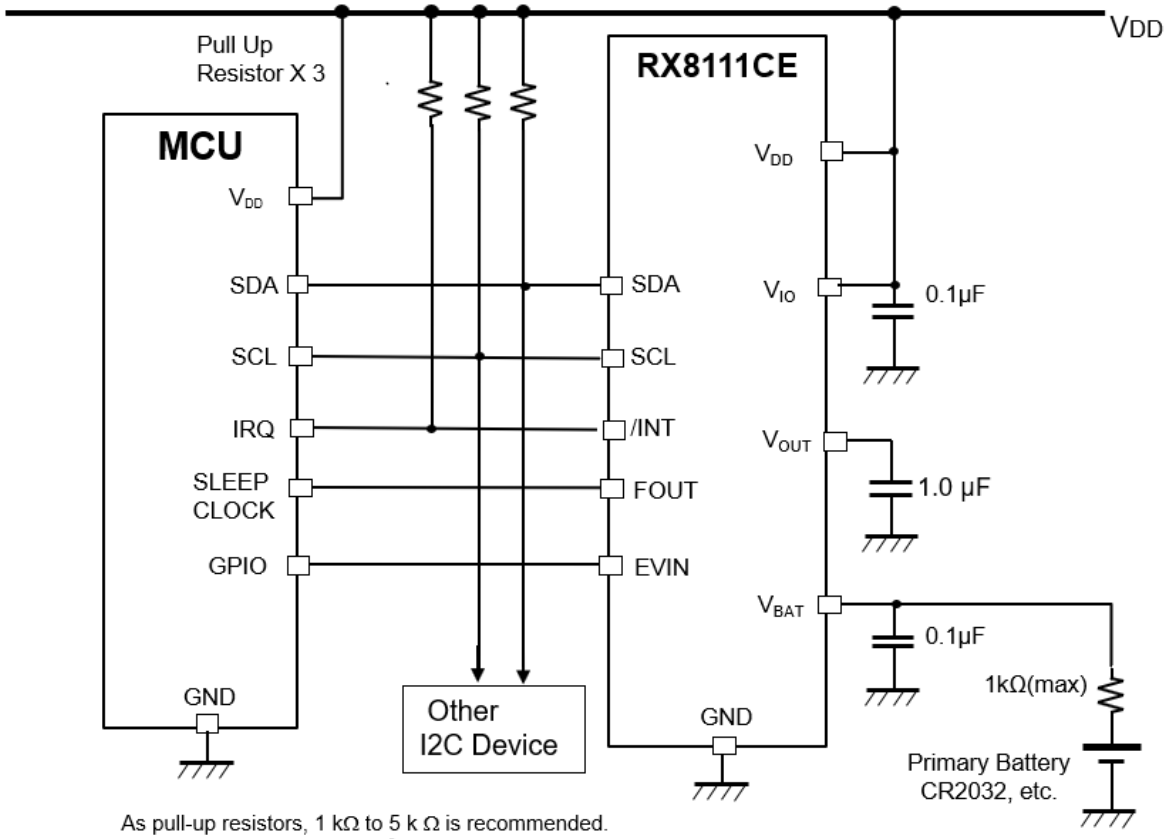


3) Read sequence when address is not specified

Once read mode has been initially set, data can be read immediately. In such cases, the address for each read operation is the previously accessed address + 1.

(1) CPU transfers start condition [S].
(2) CPU transmits the RX8111CE's slave address with the R/W bit set to read mode.
(3) Check for ACK signal from RX8111 (from this point on, the CPU is the receiver and the RX8111CE is the transmitter).
(4) Data is output from the RX8111CE to the address following the end of the previously accessed address.
(5) CPU transfers ACK signal to RX8111CE.
(6) Repeat (4) and (5) if necessary. Read addresses are automatically incremented in the RX8111CE.
(7) CPU transfers ACK signal for "1".
(8) CPU transfers stop condition [P].

15. Circuit Diagram Connection



As pull-up resistors, 1 kΩ to 5 k Ω is recommended.
SDA and SCL should meet I²C Bus specifications.
Each bypass capacitors should be located in the vicinity of RTC.
The capacitors of V_{OUT} is 1.0 µF.

16. Tables

17. Figures

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