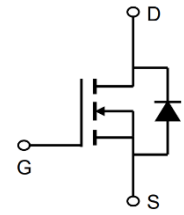


## 30V N-Channel Enhancement Mode MOSFET

### Description

The AP50N03DF uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a

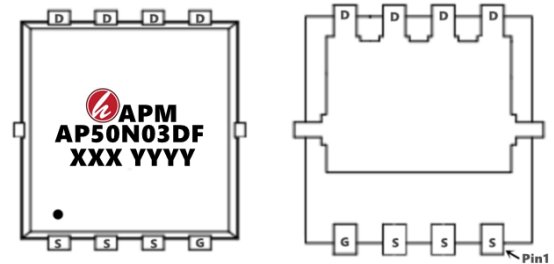
Battery protection or in other Switching application.



### General Features

$V_{DS} = 30V$   $I_D = 50A$

$R_{DS(ON)} < 12m\Omega$  @  $V_{GS}=10V$  (Type: 10.5m $\Omega$ )



### Application

Lithium battery protection

Wireless impact

Mobile phone fast charging



### Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP50N03DF	PDFN3*3-8L	AP50N03DF XXX YYYYY	5000

### Absolute Maximum Ratings ( $T_C=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	30	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D@T_C=25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^1$	50	A
$I_D@T_C=100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^1$	23	A
IDM	Pulsed Drain Current <sup>2</sup>	75	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	24.2	mJ
IAS	Avalanche Current	22	A
$P_D@T_C=25^\circ\text{C}$	Total Power Dissipation <sup>4</sup>	26	W
$P_D@T_A=25^\circ\text{C}$	Total Power Dissipation <sup>4</sup>	1.67	W
TSTG	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup>	75	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance Junction-Case <sup>1</sup>	4.8	$^\circ\text{C/W}$

## 30V N-Channel Enhancement Mode MOSFET

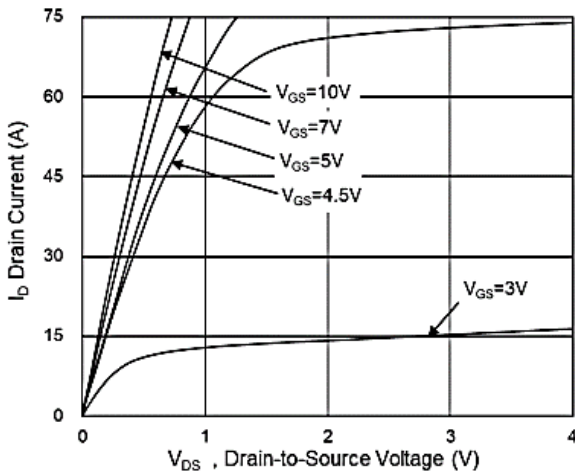
### Electrical Characteristics (T<sub>c</sub>=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	30	---	---	V
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =10V, I <sub>D</sub> =6A	---	10.5	12	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =5A	---	15.5	19	
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =250uA	1.2	1.6	2.5	V
I <sub>DSS</sub>	Drain-Source Leakage Current	V <sub>DS</sub> =24V, V <sub>GS</sub> =0V, T <sub>J</sub> =25°C	---	---	1	uA
		V <sub>DS</sub> =24V, V <sub>GS</sub> =0V, T <sub>J</sub> =55°C	---	---	5	
I <sub>GSS</sub>	Gate-Source Leakage Current	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	---	---	±100	nA
g <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =12A	---	32	---	S
R <sub>g</sub>	Gate Resistance	V <sub>DS</sub> =0V, V <sub>GS</sub> =0V, f=1MHz	---	2.1	---	Ω
Q <sub>g</sub>	Total Gate Charge (4.5V)	V <sub>DS</sub> =15V, V <sub>GS</sub> =4.5V, I <sub>D</sub> =6A	---	4.2	---	nC
Q <sub>gs</sub>	Gate-Source Charge		---	2.6	---	
Q <sub>gd</sub>	Gate-Drain Charge		---	1.4	---	
T <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> =15V, V <sub>GS</sub> =10V, R <sub>G</sub> =1.5Ω, I <sub>D</sub> =1A	---	13.1	---	ns
T <sub>r</sub>	Rise Time		---	6.3	---	
T <sub>d(off)</sub>	Turn-Off Delay Time		---	21	---	
T <sub>f</sub>	Fall Time		---	7	---	
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =15V, V <sub>GS</sub> =0V, f=1MHz	---	870	---	pF
C <sub>oss</sub>	Output Capacitance		---	135	---	
C <sub>rss</sub>	Reverse Transfer Capacitance		---	87	---	
I <sub>s</sub>	Continuous Source Current <sup>1,5</sup>	V <sub>G</sub> =V <sub>D</sub> =0V, Force Current	---	---	37	A
V <sub>SD</sub>	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V, I <sub>s</sub> =1A, T <sub>J</sub> =25°C	---	---	1	V

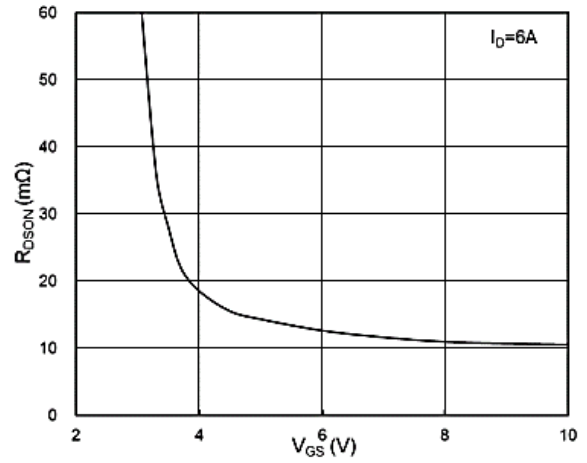
#### Note :

- 1、 The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2、 The data tested by pulsed , pulse width ≅ 300us , duty cycle ≅ 2%
- 3、 The power dissipation is limited by 175°C junction temperature
- 4、 The data is theoretically the same as I<sub>D</sub> and I<sub>DM</sub> , in real applications , should be limited by total power dissipation.

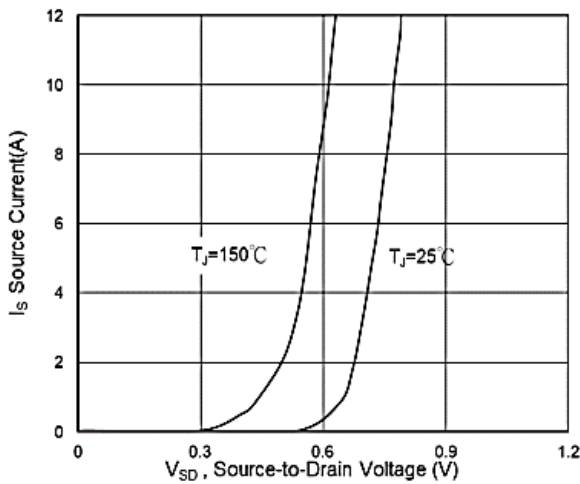
**Typical Characteristics**



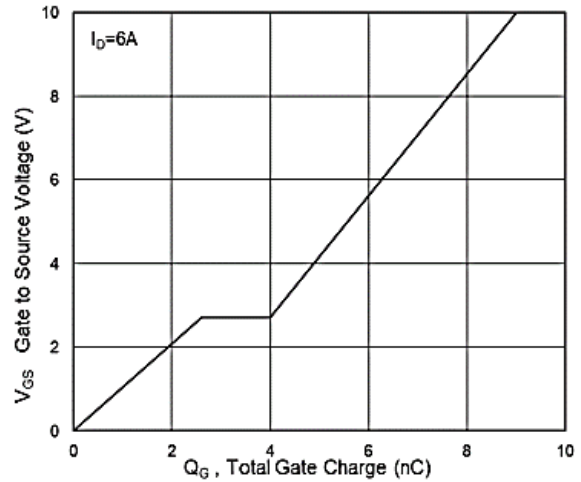
**Fig.1 Typical Output Characteristics**



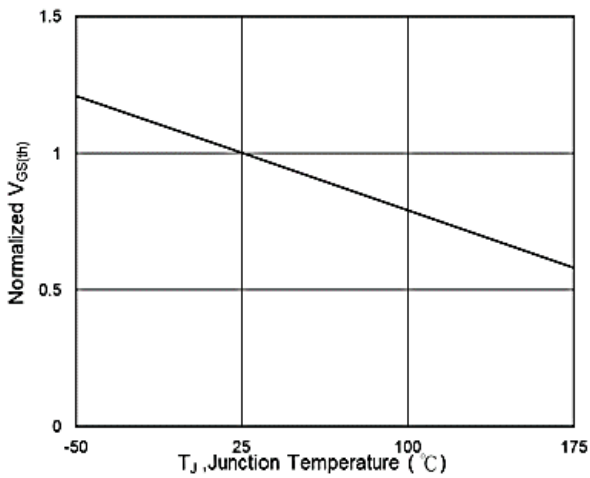
**Fig.2 On-Resistance vs G-S Voltage**



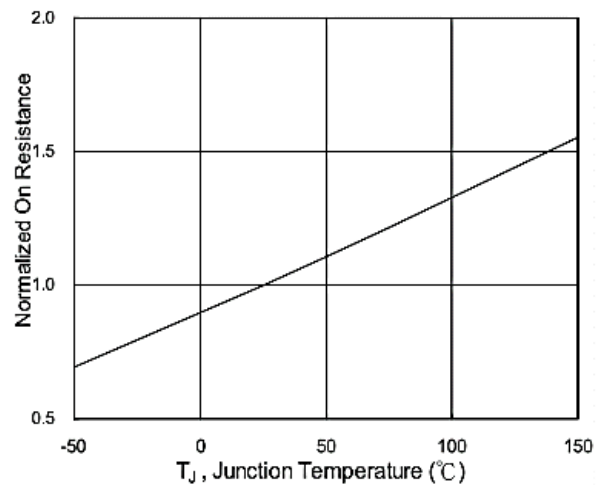
**Fig.3 Source Drain Forward Characteristics**



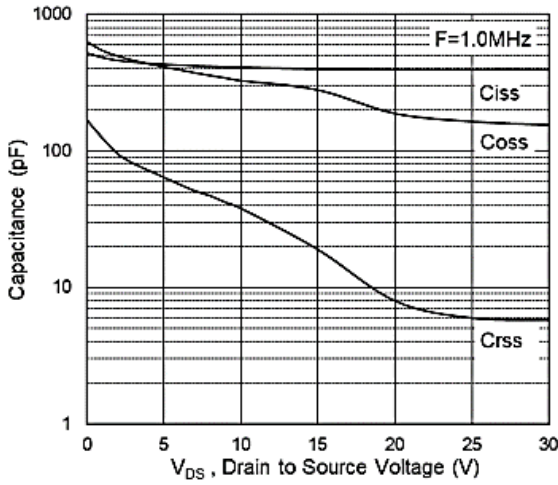
**Fig.4 Gate-charge Characteristics**



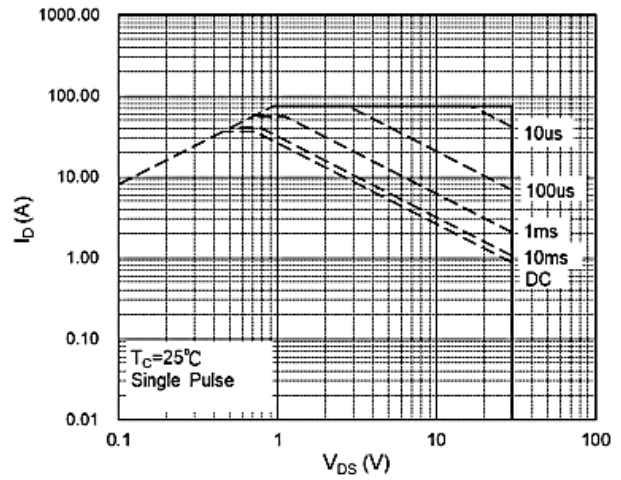
**Fig.5 Normalized  $V_{GS(th)}$  vs  $T_J$**



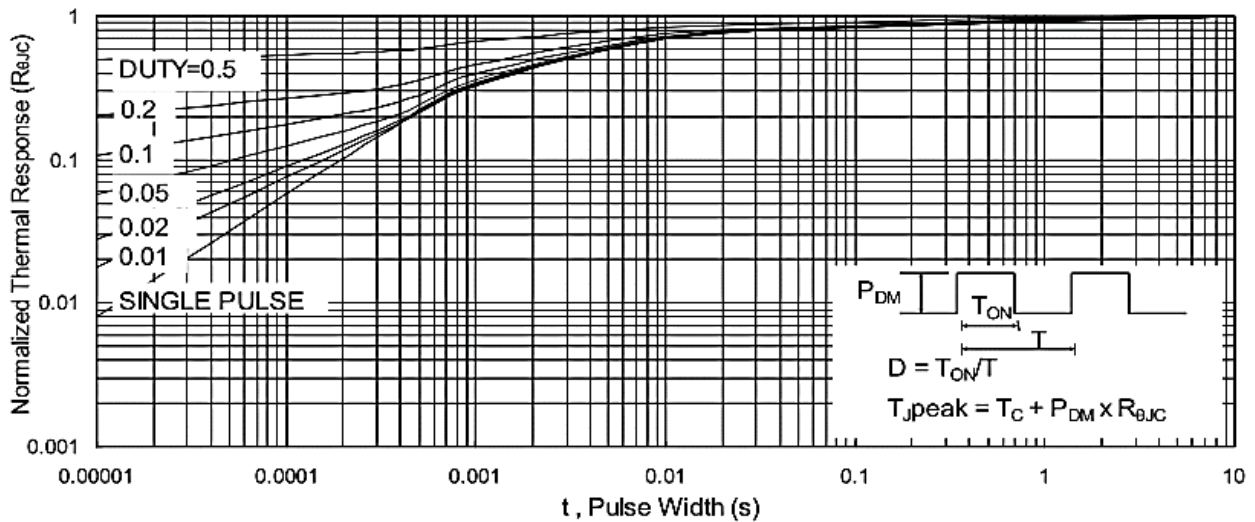
**Fig.6 Normalized  $R_{DS(on)}$  vs  $T_J$**



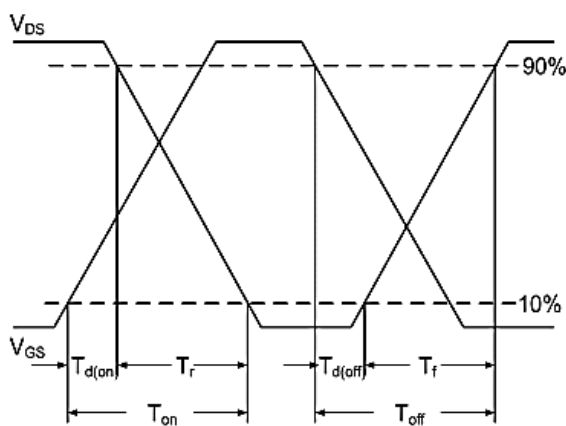
**Fig.7 Capacitance**



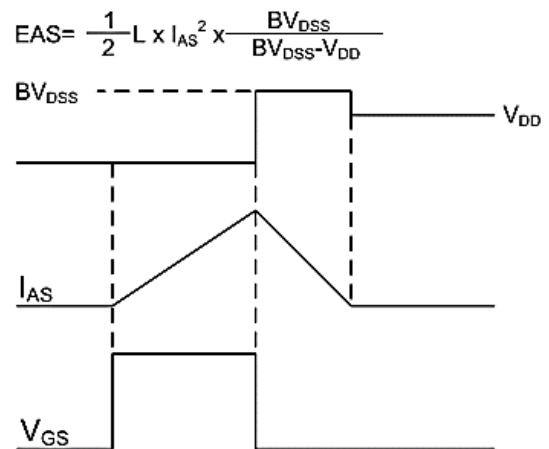
**Fig.8 Safe Operating Area**



**Fig.9 Normalized Maximum Transient Thermal Impedance**

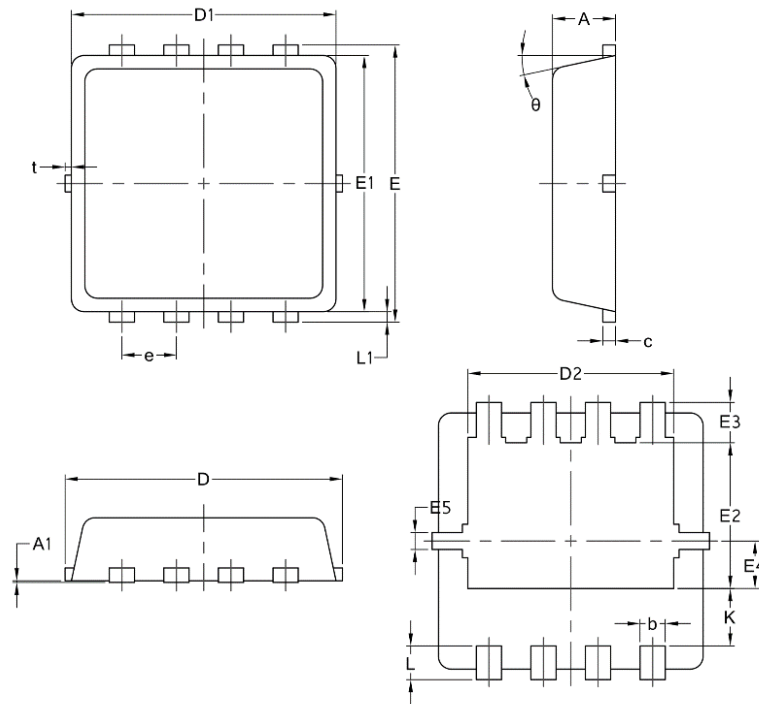


**Fig.10 Switching Time Waveform**



**Fig.11 Unclamped Inductive Waveform**

### Package Mechanical Data-DFN3\*3-8L-JQ Single



Symbol	Common		
	mm		
	Mim	Nom	Max
A	0.70	0.75	0.85
A1	/	/	0.05
b	0.20	0.30	0.40
c	0.10	0.152	0.25
D	3.15	3.30	3.45
D1	3.00	3.15	3.25
D2	2.29	2.45	2.65
E	3.15	3.30	3.45
E1	2.90	3.05	3.20
E2	1.54	1.74	1.94
E3	0.28	0.48	0.65
E4	0.37	0.57	0.77
E5	0.10	0.20	0.30
e	0.60	0.65	0.70
K	0.59	0.69	0.89
L	0.30	0.40	0.50
L1	0.06	0.125	0.20
t	0	0.075	0.13
Φ	10	12	14

**30V N-Channel Enhancement Mode MOSFET****Attention**

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Edition	Date	Change
Rve1.0	2021/8/10	Initial release

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