

## 200V N-Channel Enhancement Mode MOSFET

### Description

The AP40N20P/T is silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency.

### General Features

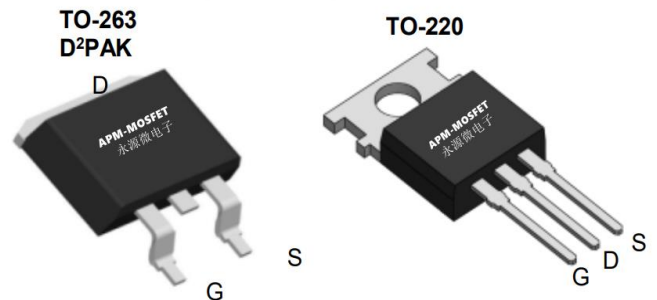
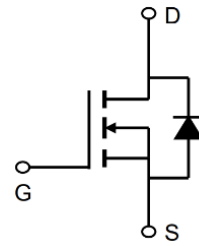
$V_{DS} = 200V$   $I_D = 40A$

$R_{DS(ON)} < 65m\Omega$  @  $V_{GS}=10V$  (Type: 50m $\Omega$ )

### Application

Uninterruptible Power Supply(UPS)

Power Factor Correction (PFC)



### Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP40N20T	TO-263-3L	AP40N20T XXX YYYY	800
AP40N20P	TO-220-3L	AP40N20P XXX YYYY	1000

### Absolute Maximum Ratings ( $T_C=25^{\circ}C$ unless otherwise noted)

Symbol	Parameter	Value	Unit
VDSS	Drain-Source Voltage	200	V
ID	Drain Current -continuous	40	A
IDM	Drain Current -pulse	112	A
VGSS	Gate-Source Voltage	$\pm 30$	V
EAS	Single Pulsed Avalanche Energy	588	mJ
IAR	Avalanche Current	28	A
EAR	Repetitive Avalanche Current	15.8	mJ
dv/dt	Peak Diode Recovery dv/dt	5.5	V/ns
PD $T_C=25^{\circ}C$	Power Dissipation	158	W
TJ, TSTG	Operating and Storage Temperature Range	$-55 \sim +150$	$^{\circ}C$
TL	Maximum Lead Temperature for Soldering Purposes	300	$^{\circ}C$
Rth(j-c)	Thermal Resistance, Junction to Case	0.79	$^{\circ}C/W$
Rth(j-A)	Thermal Resistance, Junction to Ambient	62.5	$^{\circ}C/W$

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### Electrical Characteristics (T<sub>J</sub>=25°C, unless otherwise noted)

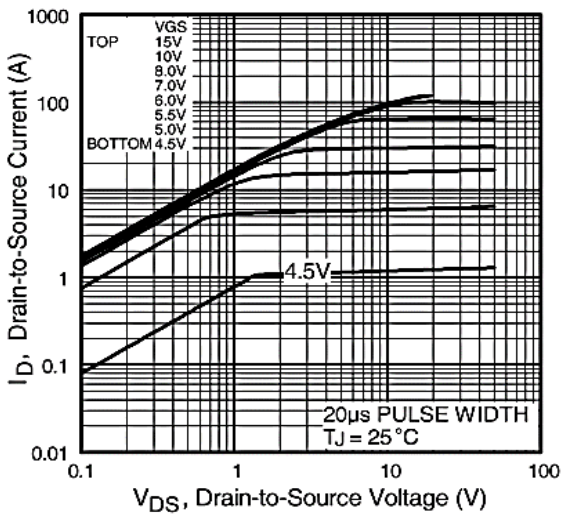
Symbol	Parameter	Tests conditions	Min	Typ	Max	Units
BV <sub>DSS</sub>	Drain-Source Voltage	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V	200	-	-	V
IDSS	Zero Gate Voltage Drain Current	V <sub>DS</sub> =200V, V <sub>GS</sub> =0V, T <sub>C</sub> =25°C	-	-	1	μA
IGSSF	Gate-body leakage current, forward	V <sub>DS</sub> =0V, V <sub>GS</sub> =30V	-	-	100	nA
IGSSR	Gate-body leakage current, reverse	V <sub>DS</sub> =0V, V <sub>GS</sub> =-30V	-	-	-100	nA
VGS(th)	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =250μA	2.0	3.0	4.0	V
RDS(ON)	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V , I <sub>D</sub> =14.0A	-	50	65	mΩ
g <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> = 40V , I <sub>D</sub> =14.0A	-	24	-	S
C <sub>iss</sub>	Input capacitance	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V, f=1.0MHz	-	2879	3742	pF
C <sub>oss</sub>	Output capacitance		-	362	470	pF
C <sub>rss</sub>	Reverse transfer capacitance		-	81	105	pF
t <sub>d(on)</sub>	Turn-On delay time	V <sub>DD</sub> =100V, I <sub>D</sub> =28A, R <sub>G</sub> =25Ω V <sub>GS</sub> =10V (note 4, 5)	-	28	69	ns
t <sub>r</sub>	Turn-On rise time		-	251	494	ns
t <sub>d(off)</sub>	Turn-Off delay time		-	309	617	ns
t <sub>f</sub>	Turn-Off Fall time		-	220	412	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =160V , I <sub>D</sub> =28A V <sub>GS</sub> =10V	-	103	136	nC
Q <sub>gs</sub>	Gate-Source charge		-	16	-	nC
Q <sub>gd</sub>	Gate-Drain charge		-	53	-	nC
IS	Continuous Body Diode Current	T <sub>C</sub> = 25 °C	-	-	28	A
ISM	Pulsed Diode Forward Current		-	-	112	A
VSD	Body Diode Voltage	V <sub>GS</sub> =0V, I <sub>S</sub> =28A	-		1.4	V
t <sub>rr</sub>	Reverse recovery time	V <sub>GS</sub> =0V, I <sub>S</sub> =28A dI <sub>F</sub> /dt=100A/μs		218		ns
Q <sub>rr</sub>	Reverse recovery charge			1.91		μC

#### Note :

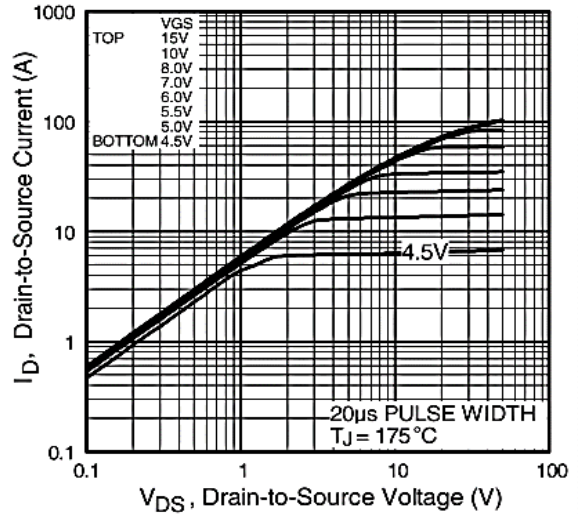
- 1、 The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2、 The EAS data shows Max. rating . L=1.5mH, I<sub>AS</sub>=28A, V<sub>DB</sub>=50V, R<sub>G</sub>=25 Ω, Starting T<sub>J</sub>=25°C
- 3、 The test condition is Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 1%
- 4、 The power dissipation is limited by 150°C junction temperature
- 5、 The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

**200V N-Channel Enhancement Mode MOSFET**

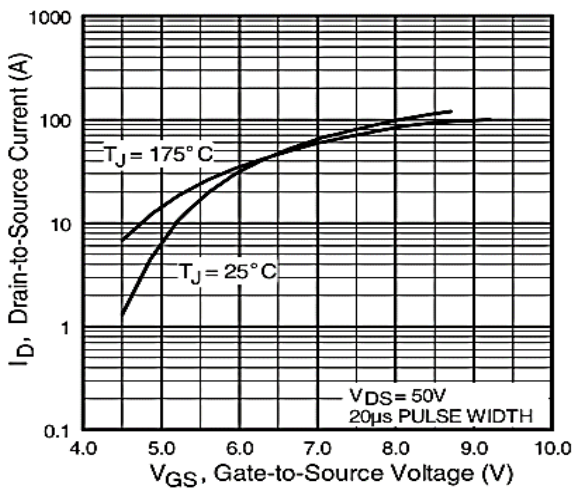
**Electrical Characteristics**



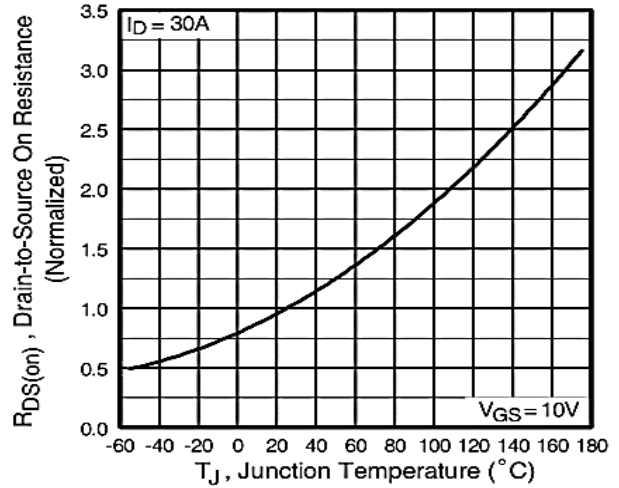
**Fig 1. Typical Output Characteristics**



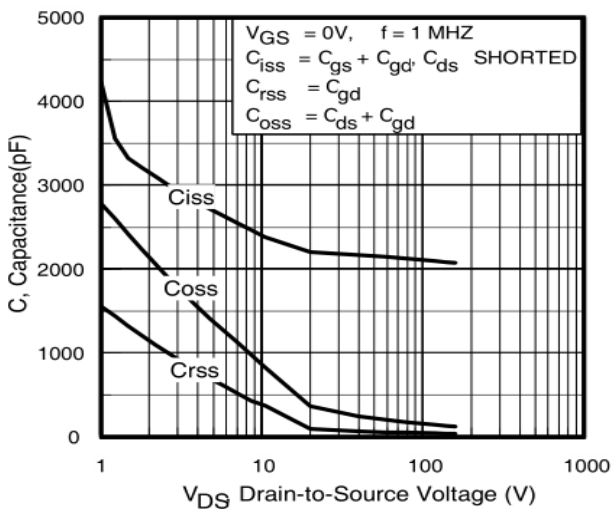
**Fig 2. Typical Output Characteristics**



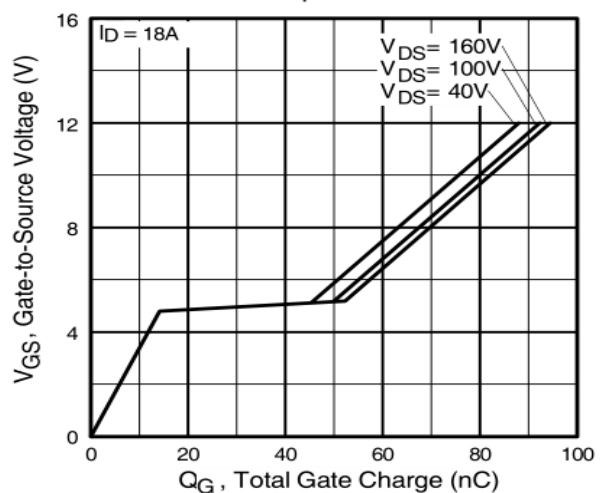
**Fig 3. Typical Transfer Characteristics**



**Fig 4. Normalized On-Resistance Vs. Temperature**



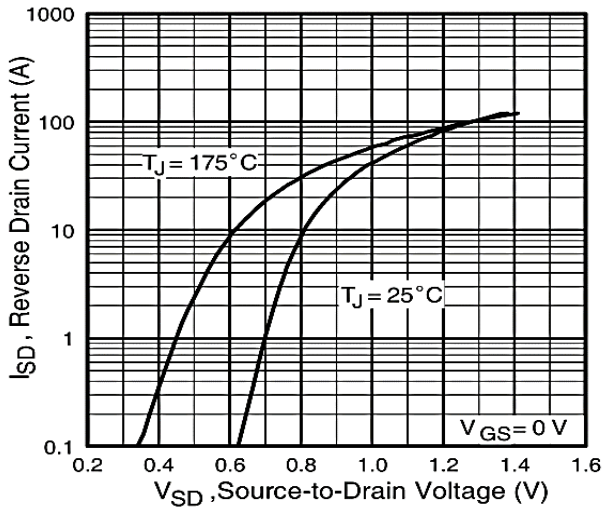
**Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage**



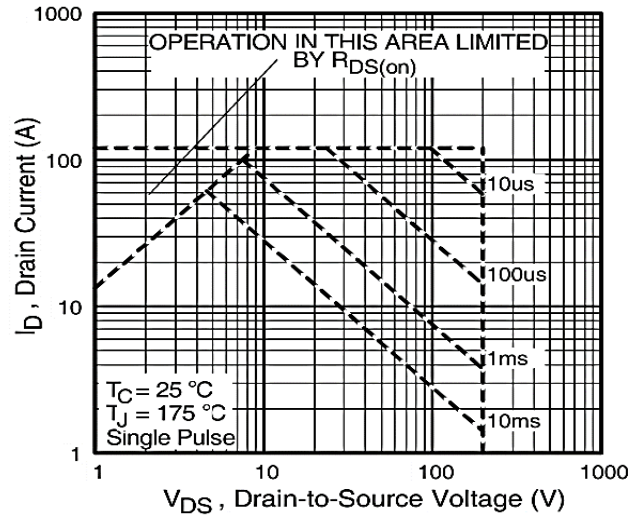
**Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage**



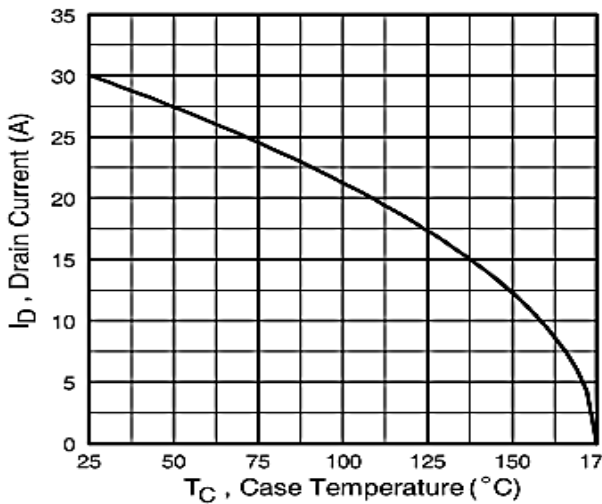
**200V N-Channel Enhancement Mode MOSFET**



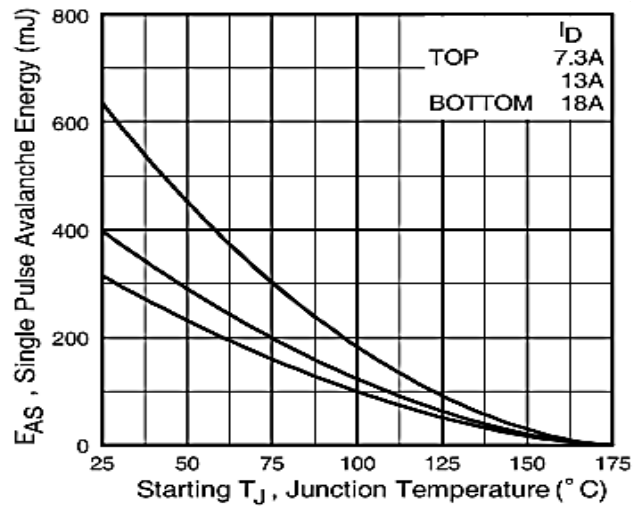
**Fig 7. Typical Source-Drain Diode Forward Voltage**



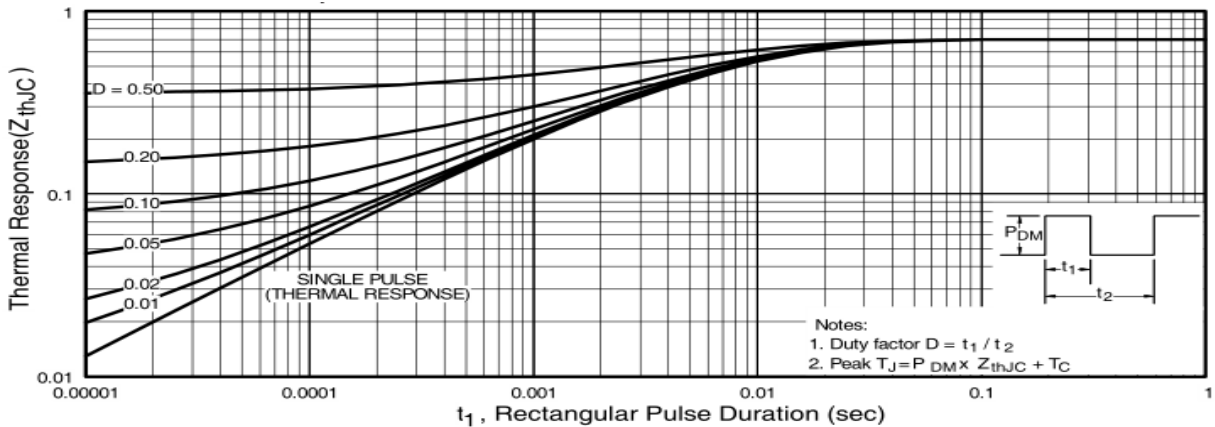
**Fig 8. Maximum Safe Operating Area**



**Fig 9. Maximum Drain Current Vs. Case Temperature**



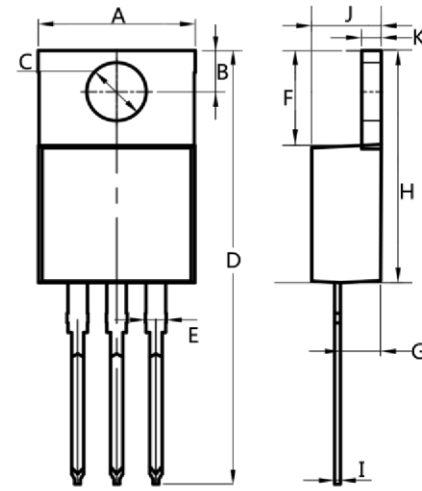
**Fig 12c. Maximum Avalanche Energy Vs. Drain Current**



**Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case**

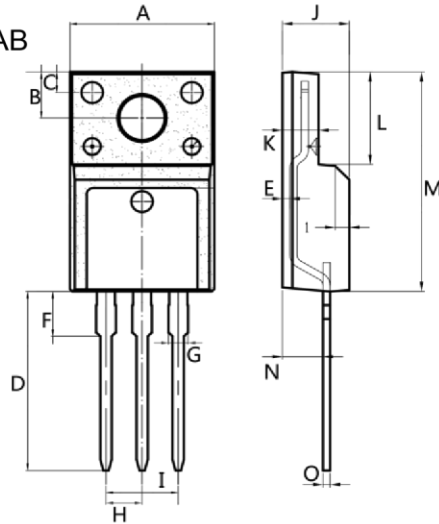
## 200V N-Channel Enhancement Mode MOSFET

TO-220AB



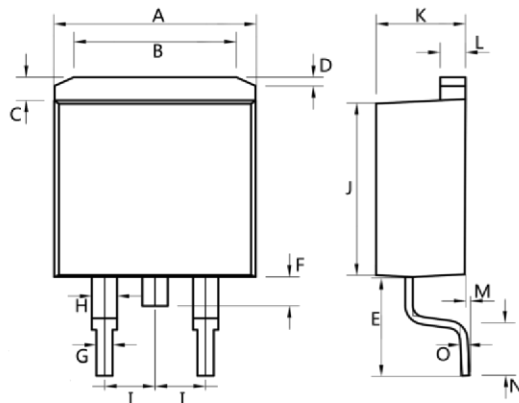
Dim.	Min.	Max.
A	10.0	10.4
B	2.5	3.0
C	3.5	4.0
D	28.0	30.0
E	1.1	1.5
F	6.2	6.6
G	2.9	3.3
H	15.0	16.0
I	0.35	0.45
J	4.3	4.7
K	1.2	1.4
All Dimensions in millimeter		

ITO-220AB



Dim.	Min.	Max.
A	9.9	10.3
B	2.9	3.5
C	1.15	1.45
D	12.75	13.25
E	0.55	0.75
F	3.1	3.5
G	1.25	1.45
H	Typ 2.54	
I	Typ 5.08	
J	4.55	4.75
K	2.4	2.7
L	6.35	6.75
M	15.0	16.0
N	2.75	3.15
O	0.45	0.60
All Dimensions in millimeter		

TO-263



Dim.	Min.	Max.
A	10.0	10.5
B	7.25	7.75
C	1.3	1.5
D	0.55	0.75
E	5.0	6.0
F	1.4	1.6
G	0.75	0.95
H	1.15	1.35
I	Typ 2.54	
J	8.4	8.6
K	4.4	4.6
L	1.25	1.45
M	0.02	0.1
N	2.4	2.8
O	0.35	0.45
All Dimensions in millimeter		

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## 200V N-Channel Enhancement Mode MOSFET

Edition	Date	Change
Rve1.0	2019/1/31	Initial release

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