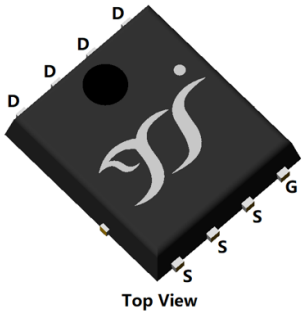
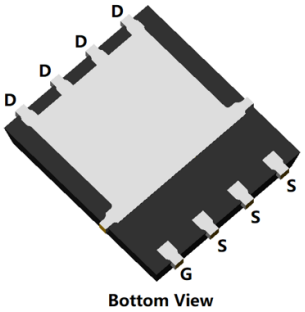
# P-Channel Enhancement Mode Field Effect Transistor

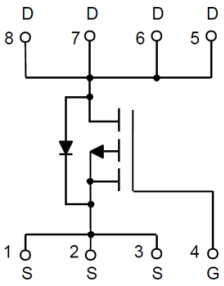



Top View




Bottom View

**PDFN5060-8L**




## Product Summary

- $V_{DS}$ -30V
- $I_D$ -40A
- $R_{DS(ON)}$( at $V_{GS}$=-20V) ＜12mohm
- $R_{DS(ON)}$( at $V_{GS}$=-10V) ＜14mohm
- $R_{DS(ON)}$( at $V_{GS}$=-4.5V) ＜24mohm
- 100% EAS Tested
- 100% ▽$V_{DS}$ Tested

## General Description

- Trench Power LV MOSFET technology
- High density cell design for Low $R_{DS(ON)}$
- High Speed switching
- Moisture Sensitivity Level 3
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

## Applications

- Battery protection
- Power management
- Load switch

## ■ Absolute Maximum Ratings ($T_A$=25℃unless otherwise noted)

| Parameter | | Symbol | Maximum | Unit |
|---|---|---|---|---|
| Drain-source Voltage | | $V_{DS}$ | -30 | V |
| Gate-source Voltage | | $V_{GS}$ | ±25 | V |
| Drain Current | $T_A$=25℃ @ Steady State | $I_D$ | -40 | A |
| | $T_A$=70℃ @ Steady State | | -32 | |
| Pulsed Drain Current [A] | | $I_{DM}$ | -160 | A |
| Single Pulse Avalanche Energy @L=0.5mH [B] | | $E_{AS}$ | 100 | mJ |
| Total Power Dissipation @ $T_C$=25℃ [C] | | $P_D$ | 45 | W |
| Thermal Resistance Junction-to-Case @ Steady State | | $R_{\theta JC}$ | 2.8 | ℃/W |
| Thermal Resistance Junction-to-Ambient @ Steady State [D] | | $R_{\theta JA}$ | 40 | ℃/W |
| Junction and Storage Temperature Range | | $T_J$ ,$T_{STG}$ | -55～+150 | ℃ |

## ■ Ordering Information (Example)

| PREFERED P/N | PACKING CODE | Marking | MINIMUM PACKAGE(pcs) | INNER BOX QUANTITY(pcs) | OUTER CARTON QUANTITY(pcs) | DELIVERY MODE |
|---|---|---|---|---|---|---|
| YJG40P03A | F1 | YJG40P03A | 5000 | 10000 | 100000 | 13“ reel |

## ■ Electrical Characteristics ($T_J$=25℃ unless otherwise noted)

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Static Parameter** | | | | | | |
| Drain-Source Breakdown Voltage | $BV_{DSS}$ | $V_{GS}$= 0V, $I_D$=-250μA | -30 | | | V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$=-30V,$V_{GS}$=0V,$T_C$=25℃ | | | -1 | μA |
| Gate-Body Leakage Current | $I_{GSS}$ | $V_{GS}$= ±25V, $V_{DS}$=0V | | | ±100 | nA |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$= $V_{GS}$, $I_D$=-250μA | -1.2 | -1.8 | -2.8 | V |
| Static Drain-Source On-Resistance | $R_{DS(ON)}$ | $V_{GS}$= -20V, $I_D$=-20A | | 7.6 | 12 | mΩ |
| | | $V_{GS}$= -10V, $I_D$=-15A | | 9 | 14 | |
| | | $V_{GS}$= -6.0V, $I_D$=-12A | | 11 | 21 | |
| | | $V_{GS}$= -4.5V, $I_D$=-10A | | 14.5 | 24 | |
| Diode Forward Voltage | $V_{SD}$ | $I_S$=-20A,$V_{GS}$=0V | | | -1.2 | V |
| Gate resistance | $R_G$ | f=1MHz, Open drain | - | 6.5 | - | Ω |
| Maximum Body-Diode Continuous Current | $I_S$ | | - | - | -40 | A |
| **Dynamic Parameters** | | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{DS}$=-15V,$V_{GS}$=0V,f=1MHZ | | 2152 | | pF |
| Output Capacitance | $C_{oss}$ | | | 308 | | |
| Reverse Transfer Capacitance | $C_{rss}$ | | | 242 | | |
| **Switching Parameters** | | | | | | |
| Total Gate Charge | $Q_g$ | $V_{GS}$=-10V,$V_{DS}$=-15V,$I_D$=-12A | | 40.1 | | nC |
| Gate Source Charge | $Q_{gs}$ | | | 8.4 | | |
| Gate Drain Charge | $Q_{gd}$ | | | 8.6 | | |
| Reverse Recovery Charge | $Q_{rr}$ | $I_F$= -12A, di/dt=100A/us | | 7.8 | | |
| Reverse Recovery Time | $t_{rr}$ | | | 18 | | ns |
| Turn-on Delay Time | $t_{D(on)}$ | $V_{GS}$=-10V,$V_{DD}$=-15V, $I_D$=-1A, $R_{GEN}$=2.5Ω | | 8 | | |
| Turn-on Rise Time | $t_r$ | | | 19 | | |
| Turn-off Delay Time | $t_{D(off)}$ | | | 75 | | |
| Turn-off Fall Time | $t_f$ | | | 46 | | |

A. Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.
B. $T_J$=25℃, $V_{DD}$=-25V, $V_G$=-10V, $R_G$=25Ω, L=0.5mH, IAS=-20A.
C. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

## ■ Typical Performance Characteristics

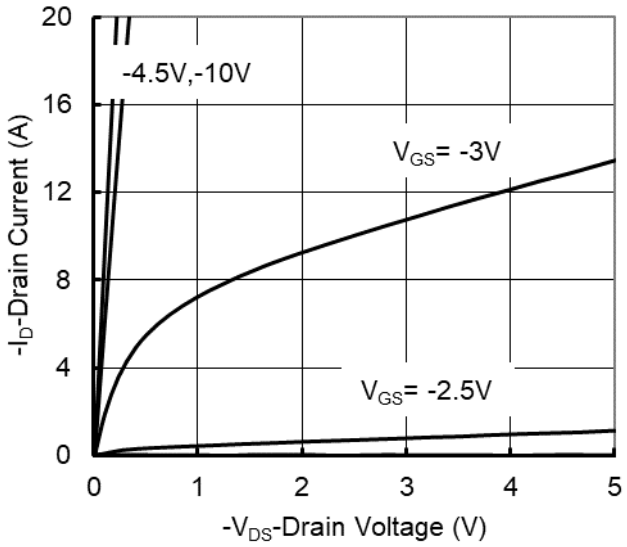



**Figure 1. Output Characteristics**

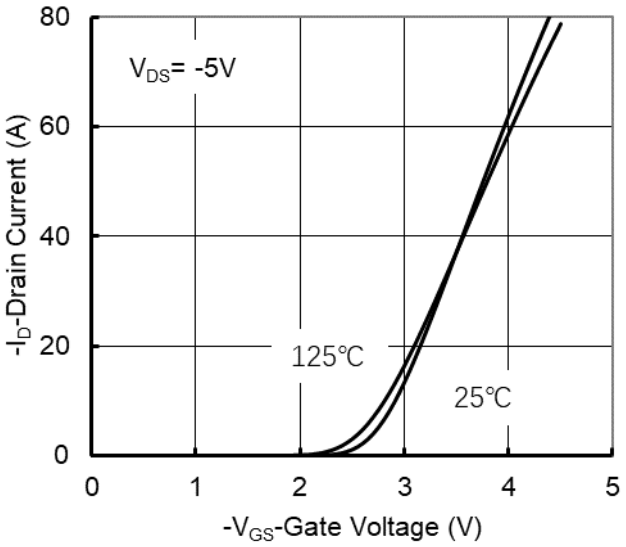



**Figure 2. Transfer Characteristics**

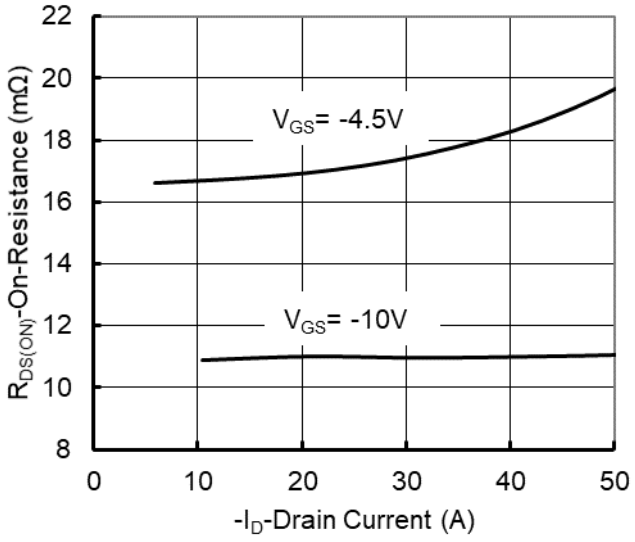



**Figure 3. On-Resistance vs. Drain Current and Gate Voltage**

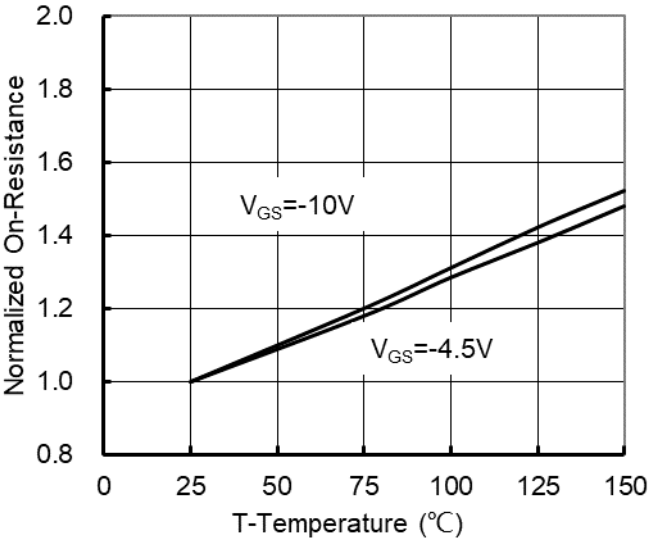



**Figure 4. On-Resistance vs. Junction Temperature**

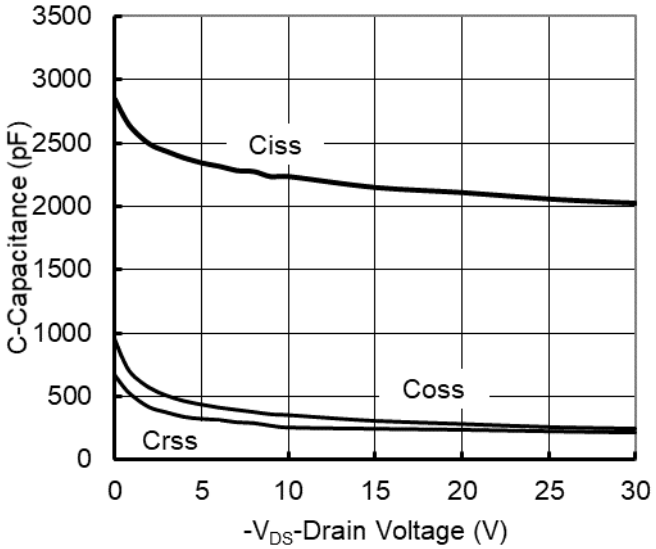



**Figure 5. Capacitance Characteristics**

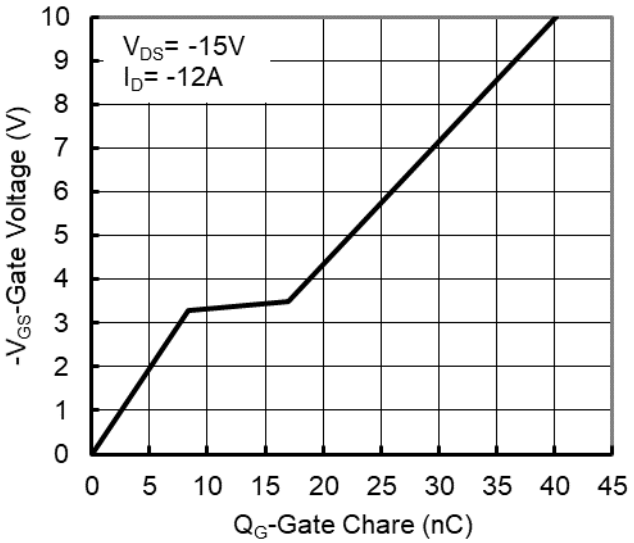



**Figure 6. Gate Charge**

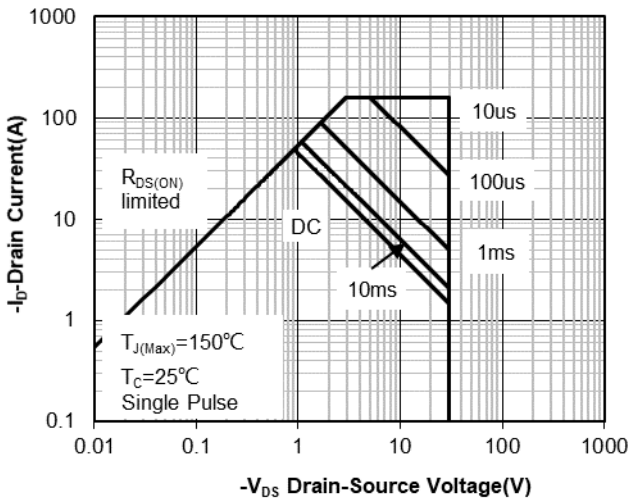



**Figure 7. Safe Operation Area**

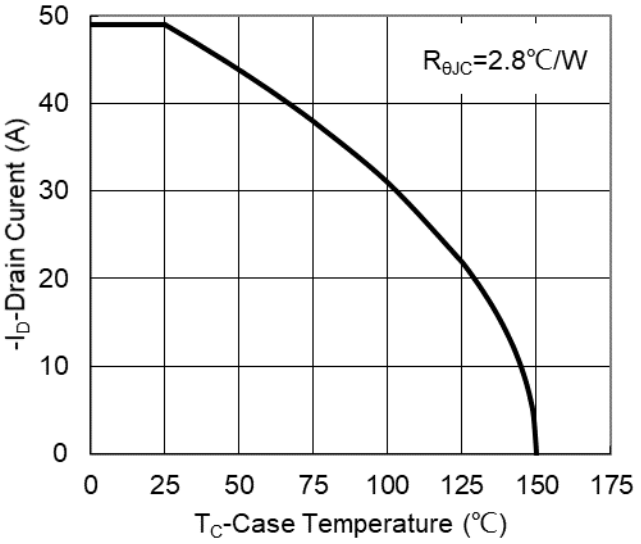



**Figure 8. Maximum Continuous Drain Current vs Case Temperature**

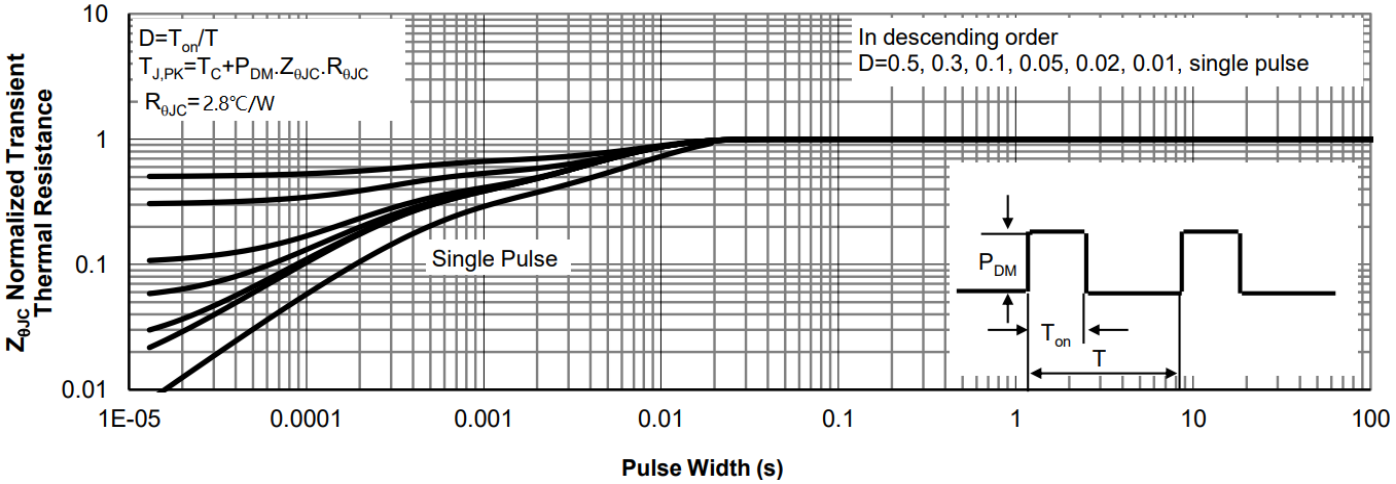
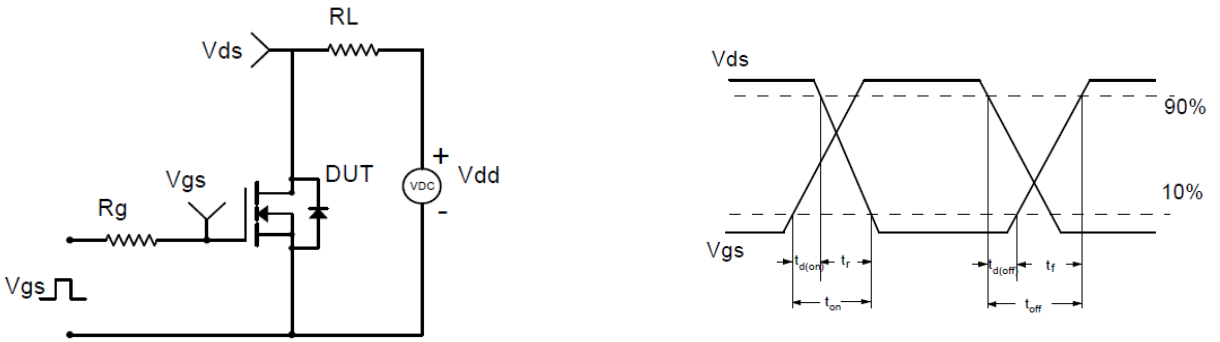
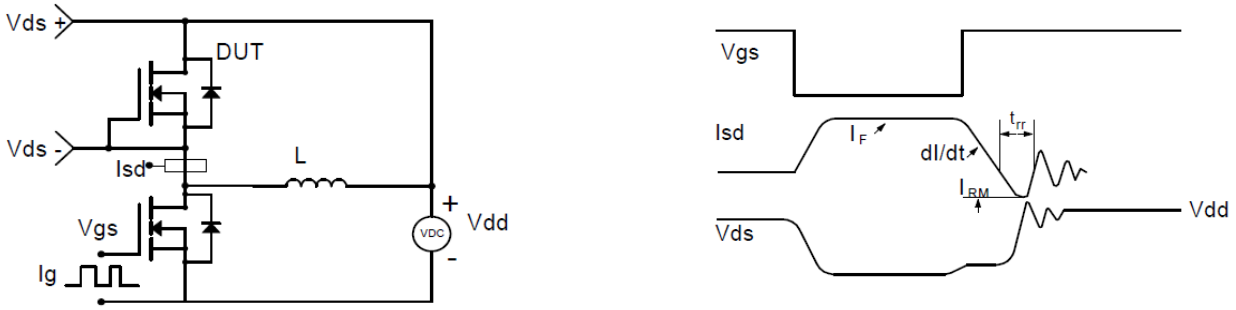


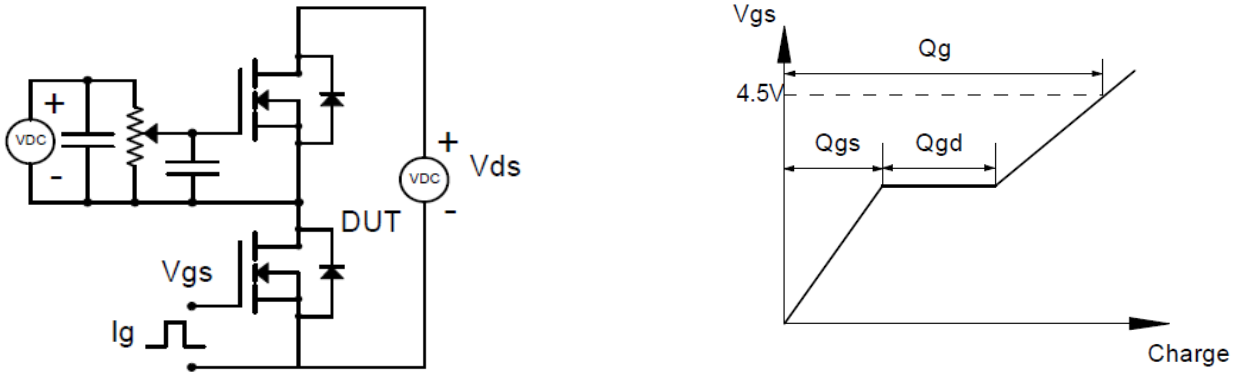

**Figure 9. Normalized Maximum Transient Thermal Impedance**



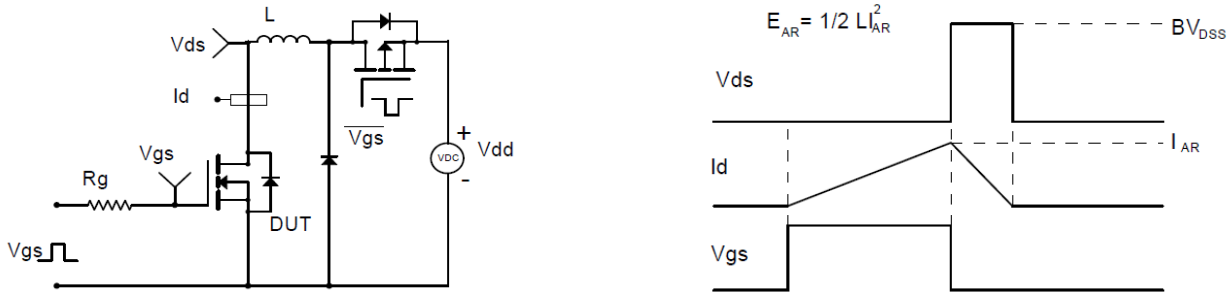

**Resistive Switching Test Circuit & Waveforms**




**Diode Recovery Test Circuit & Waveforms**

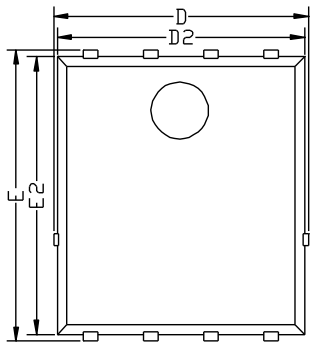



**Gate Charge Test Circuit & Waveform**

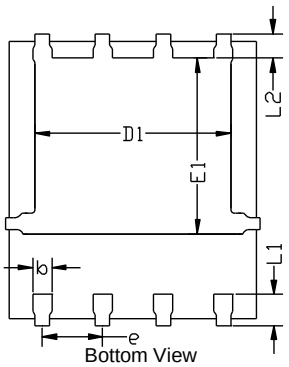



**Unclamped Inductive Switching (UIS) Test Circuit & Waveforms**

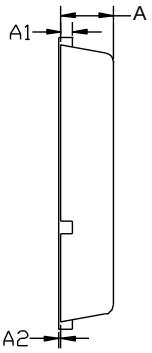
## ■ PDFN5060-8L Package information




Top View
正面视图



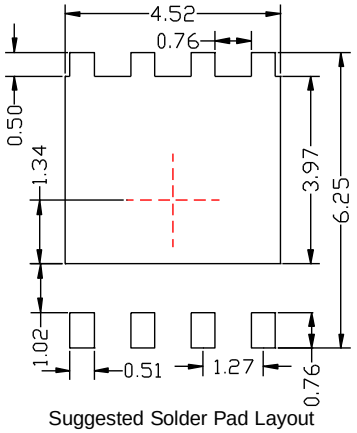

Bottom View
背面视图




Side View
侧面视图

| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| D | 5.15 | 5.35 | 5.55 |
| E | 5.95 | 6.15 | 6.35 |
| A | 1.00 | 1.10 | 1.20 |
| A1 | 0.254 BSC | | |
| A2 | | | 0.10 |
| D1 | 3.92 | 4.12 | 4.32 |
| E1 | 3.52 | 3.72 | 3.92 |
| D2 | 5.00 | 5.20 | 5.40 |
| E2 | 5.66 | 5.86 | 6.06 |
| L1 | 0.56 | 0.66 | 0.76 |
| L2 | 0.50 BSC | | |
| b | 0.31 | 0.41 | 0.51 |
| e | 1.27 BSC | | |

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:+/-0.10mm.
3.The pad layout is for reference purposes only.




Suggested Solder Pad Layout
Top View

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