

### **General Description**

APG80N10NF use advanced SGT MOSFET technology to provide low RDS(ON), low gate charge, fast switching and excellent avalanche characteristics.

This device is specially designed to get better ruggedness and suitable to use in

#### **Features**

Low RDS(on) & FOM

Extremely low switching loss

Excellent stability and uniformity or Invertors

#### **Applications**

Consumer electronic power supply

Motor control

Synchronous-rectification

Isolated DC

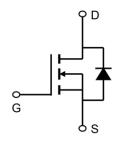
Synchronous-rectification applications

### **Package Marking and Ordering Information**

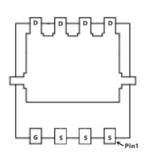
Product ID	Pack	Marking	Qty(PCS)
APG80N10NF	DFN5*6-8	APG80N10NF XXX YYYY	5000

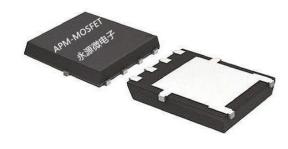
## **Absolute Maximum Ratings** at $T_j=25^{\circ}C$ unless otherwise noted

Symbol	Parameter	Rating	Units
VDS	Drain-Source Voltage	100	V
VGS	Gate-Source Voltage	±20	V
In@T <sub>A</sub> =25°C	Continuous Drain Current <sup>1</sup>	80	А
I <sub>D</sub> @T <sub>A</sub> =70°C	Continuous Drain Current <sup>1</sup>	62	Α
IDM	Pulsed Drain Current <sup>2</sup>	240	Α
EAS	Single Pulse Avalanche Energy <sup>3</sup>	120	mJ
IAS	Avalanche Current	15	Α
P <sub>D</sub> @T <sub>A</sub> =25°C	Total Power Dissipation <sup>4</sup>	135	W
TSTG	Storage Temperature Range	-55 to 150	°C
TJ	Operating Junction Temperature Range	-55 to 150	°C
ReJA	Thermal Resistance Junction-Ambient ¹(t≦10s)	54	°C/W
R <sub>θ</sub> JA	Thermal Resistance Junction-Ambient <sup>1</sup>	62	°C/W
R₀JC	Thermal Resistance Junction-Case <sup>1</sup>	0.84	°C/W











## **AElectrical Characteristics** at T<sub>j</sub>=25 °C unless otherwise specified

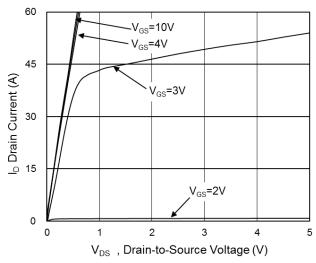
Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit	
BVDSS	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V , I <sub>D</sub> =250uA	100			V	
DDC(ON)	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =10V , I <sub>D</sub> =13.5A		6.6	8	mΩ	
RDS(ON)	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =4.5V , I <sub>D</sub> =11.5A		8.7	10.5		
VGS(th)	Gate Threshold Voltage	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =250uA	1.2		2.3	V	
IDSS	Drain-Source Leakage Current	V <sub>DS</sub> =80V , V <sub>GS</sub> =0V , T <sub>J</sub> =25°C		1			
		V <sub>DS</sub> =80V , V <sub>GS</sub> =0V , T <sub>J</sub> =55°C			5	- uA	
IGSS	Gate-Source Leakage Current	V <sub>GS</sub> =±20V , V <sub>DS</sub> =0V			±100	nA	
gfs	Forward Transconductance	V <sub>DS</sub> =5V , I <sub>D</sub> =13.5A		75		S	
Qg	Total Gate Charge (10V)			45		nC	
Qg	Total Gate Charge (4.5V)	VDS=50V , VGS=10V ,		19.3			
Qgs	Gate-Source Charge	ID=13.5A		9.5			
Qgd	Gate-Drain Charge			4.8			
Td(on)	Turn-On Delay Time			10			
Tr	Rise Time	VDD=50V , VGS=10V , RG=3Ω,		6.5			
Td(off)	Turn-Off Delay Time	ID=13.5A		45		ns	
Tf	Fall Time			7.5			
Ciss	Input Capacitance			3320			
Coss	Output Capacitance	VDS=50V , VGS=0V , f=1MHz		605		pF	
Crss	Reverse Transfer Capacitance			20			
IS	Continuous Source Current <sup>1,5</sup>	V <sub>G</sub> =V <sub>D</sub> =0V , Force Current			5	Α	
VSD	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V , I <sub>S</sub> =1A , T <sub>J</sub> =25°C			1.1	V	
trr	Reverse Recovery Time	IF=13.5A , di/dt=100A/μs ,		33		nS	
Qrr	Reverse Recovery Charge	T <sub>J</sub> =25°C		150		nC	

#### Note:

- 1. The data tested by surface mounted on a 1 inch 2 FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width  $\leq$  300us , duty cycle  $\leq$  2%
- 3. The EAS data shows Max. rating . The test condition is V DD =25 V, V GS = 10 V, L=0.3 mH, I AS = 15 A
- 4.The power dissipation is limited by 150  $^{\circ}\mathrm{C}$  junction temperature
- 5. The data is theoretically the same as I D and I DM , in real applications , should be limited by total power dissipation



## **Typical Characteristics**



**Fig.1 Typical Output Characteristics** 

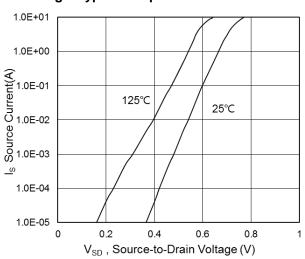


Fig.3 Source-Drain Forward Characteristics

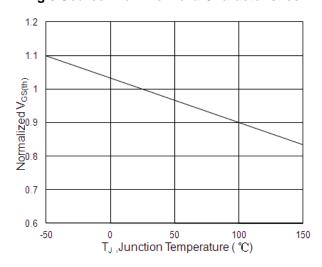


Fig.5 Normalized  $V_{GS(th)}$  vs.  $T_J$ 

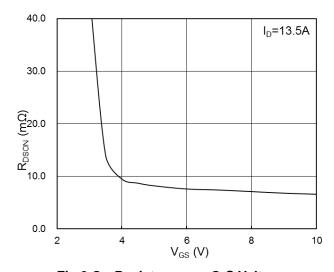


Fig.2 On-Resistance vs. G-S Voltage

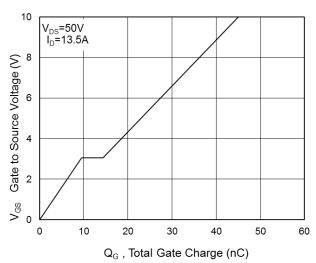


Fig.4 Gate-Charge Characteristics

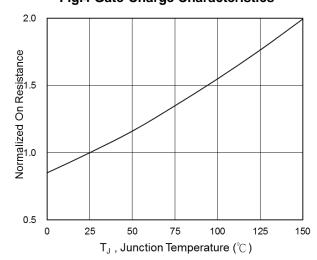
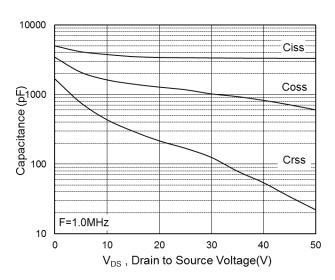


Fig.6 Normalized  $R_{\text{DSON}}$  vs.  $T_{\text{J}}$ 



# APG80N10NF

## 100V N-SGT Enhancement Mode MOSFET



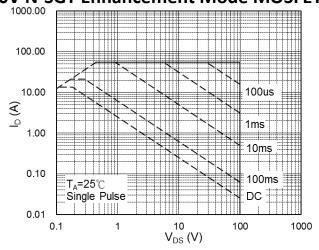


Fig.7 Capacitance

Fig.8 Safe Operating Area

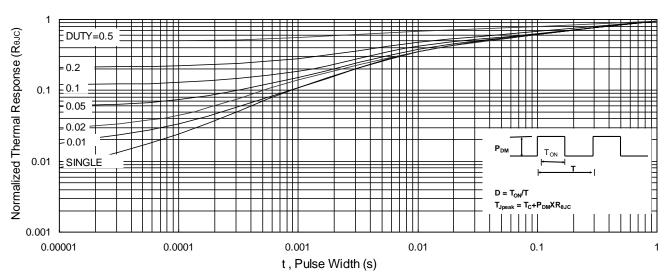
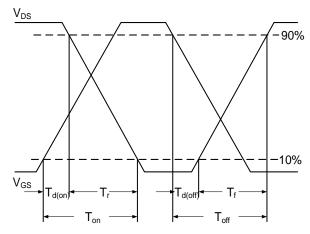


Fig.9 Normalized Maximum Transient Thermal Impedance





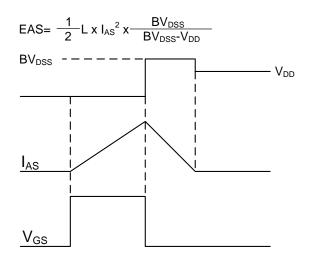
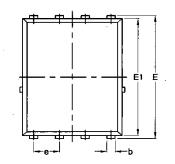
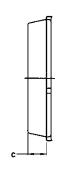


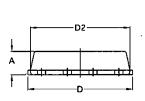
Fig.11 Unclamped Inductive Switching Waveform

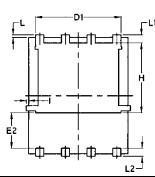


# Package Mechanical Data-DFN5\*6-8L-JQ Single









		Com	mon	
Symbol	mm		Inch	
	Mim	Max	Min	Max
Α	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
С	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
е	1.27	BSC	0.05	BSC
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
Н	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070



## APG80N10NF

#### 100V N-SGT Enhancement Mode MOSFET

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# APG80N10NF

## **100V N-SGT Enhancement Mode MOSFET**

Edition	Date	Change
Rve1.0	2019/12/1	Initial release

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