

60V N-SGT Enhancement Mode MOSFET

General Description

APG20N06S use advanced SGT MOSFET technology to provide low RDS(ON), low gate charge, fast switching and excellent avalanche characteristics.

This device is specially designed to get better ruggedness and suitable to use in

Features

- Low RDS(on) & FOM
- Extremely low switching loss
- Excellent stability and uniformity or Invertors

Applications

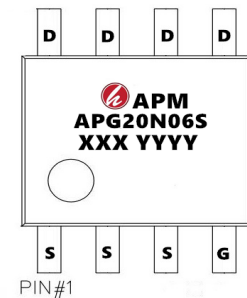
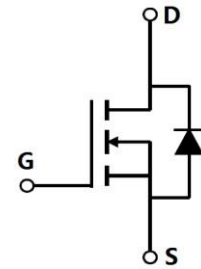
- Consumer electronic power supply
- Motor control
- Synchronous-rectification
- Isolated DC
- Synchronous-rectification applications

Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
APG20N06S	SOP-8	APG20N06S XXX YYYY	3000

Absolute Maximum Ratings at T_j=25°C unless otherwise noted

Parameter	Symbol	Value	Unit
Drain source voltage	V _{DS}	60	V
Gate source voltage	V _{GS}	±20	V
Continuous drain current ¹⁾	I _D	20	A
Pulsed drain current ²⁾	I _{D, pulse}	48	A
Power dissipation ³⁾	P _D	4	W
Single pulsed avalanche energy ⁴⁾	E _{AS}	30	mJ
Operation and storage temperature	T _{stg} , T _j	-55 to 150	°C
Thermal resistance, junction-ambient ⁵⁾	R _{θJA}	31	°C/W



60V N-SGT Enhancement Mode MOSFET

Electrical Characteristics at $T_j=25\text{ }^\circ\text{C}$ unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Drain-source breakdown voltage	BV_{DSS}	60		100	V	$V_{GS}=0\text{ V}$, $I_D=250\text{ }\mu\text{A}$
Gate threshold voltage	$V_{GS(th)}$	1.0		2.5	V	$V_{DS}=V_{GS}$, $I_D=250\text{ }\mu\text{A}$
Drain-source on-state resistance	$R_{DS(ON)}$		7.5	10	m Ω	$V_{GS}=10\text{ V}$, $I_D=20\text{ A}$
Drain-source on-state resistance	$R_{DS(ON)}$		10	13	m Ω	$V_{GS}=4.5\text{ V}$, $I_D=10\text{ A}$
Gate-source leakage current	I_{GSS}			100	nA	$V_{GS}=20\text{ V}$
				-100		$V_{GS}=-20\text{ V}$
Drain-source leakage current	I_{DSS}			1	μA	$V_{DS}=40\text{ V}$, $V_{GS}=0\text{ V}$
Input capacitance	C_{iss}		1182.1		pF	$V_{GS}=0\text{ V}$, $V_{DS}=50\text{ V}$, $f=100\text{ kHz}$
Output capacitance	C_{oss}		199.5		pF	
Reverse transfer capacitance	C_{rss}		4.1		pF	
Turn-on delay time	$t_{d(on)}$		17.9		ns	$V_{GS}=10\text{ V}$, $V_{DS}=50\text{ V}$, $R_G=2\text{ }\Omega$, $I_D=10\text{ A}$
Rise time	t_r		4.0		ns	
Turn-off delay time	$t_{d(off)}$		34.9		ns	
Fall time	t_f		5.5		ns	
Total gate charge	Q_g		18.4		nC	
Gate-source charge	Q_{gs}		3.3		nC	
Gate-drain charge	Q_{gd}		3.1		nC	
Gate plateau voltage	$V_{plateau}$		2.8		V	$I_D=10\text{ A}$, $V_{DS}=50\text{ V}$, $V_{GS}=10\text{ V}$
Diode forward current	I_S			60	A	$V_{GS}<V_{th}$
Pulsed source current	I_{SP}			180		
Diode forward voltage	V_{SD}			1.3	V	$I_S=20\text{ A}$, $V_{GS}=0\text{ V}$
Reverse recovery time	t_{rr}		41.8		ns	$I_S=10\text{ A}$, $di/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge	Q_{rr}		36.1		nC	
Peak reverse recovery current	I_{rrm}		1.4		A	

Note

- 1) Calculated continuous current based on maximum allowable junction temperature.
- 2) Repetitive rating; pulse width limited by max. junction temperature.
- 3) P_d is based on max. junction temperature, using junction-case thermal resistance.
- 4) $V_{DD}=50\text{ V}$, $R_G=50\text{ }\Omega$, $L=0.3\text{ mH}$, starting $T_j=25\text{ }^\circ\text{C}$.
- 5) The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_a=25\text{ }^\circ\text{C}$.

Electrical Characteristics Diagrams

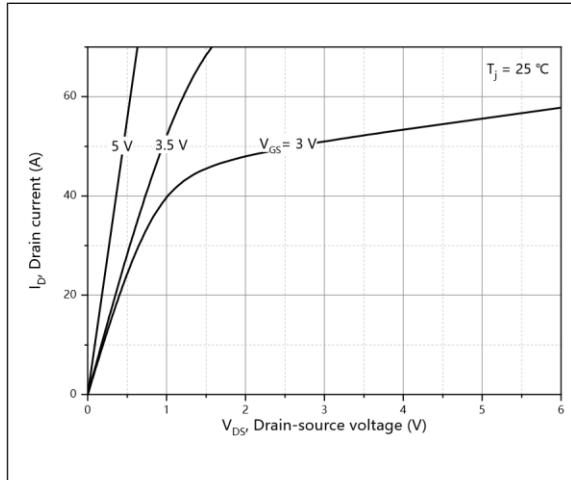


Figure 1, Typ. output characteristics

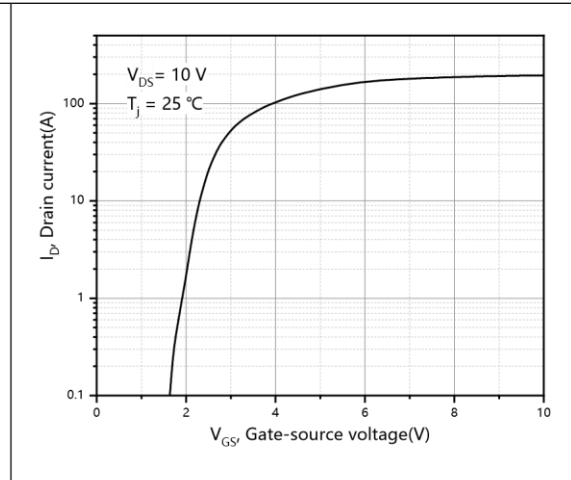


Figure 2, Typ. transfer characteristics

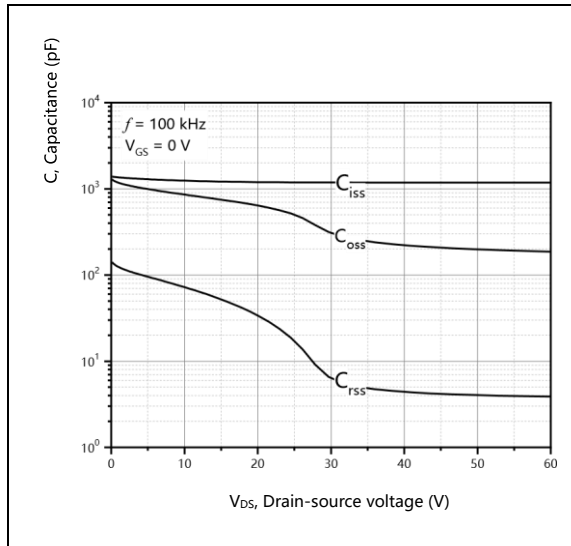


Figure 3, Typ. capacitances

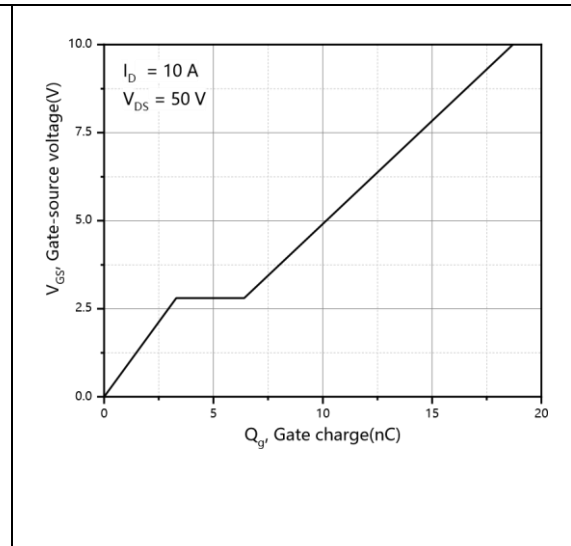


Figure 4, Typ. gate charge

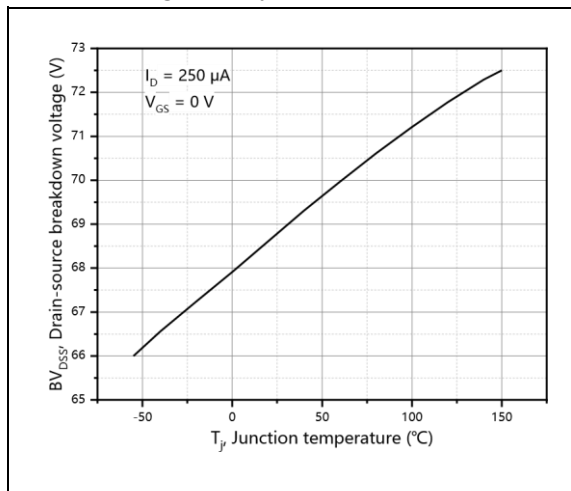


Figure 5, Drain-source breakdown voltage

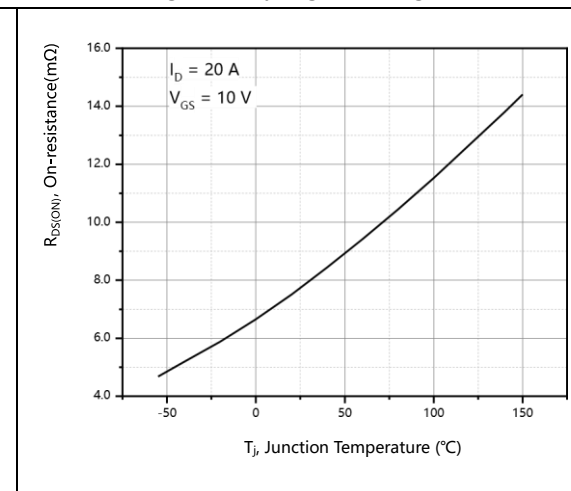


Figure 6, Drain-source on-state resistance

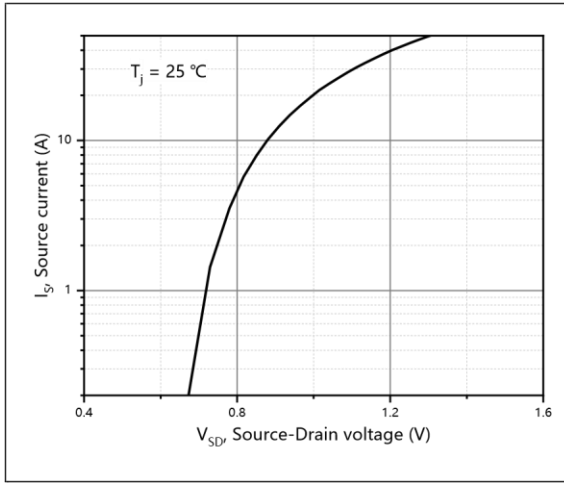


Figure 7, Forward characteristic of body diode

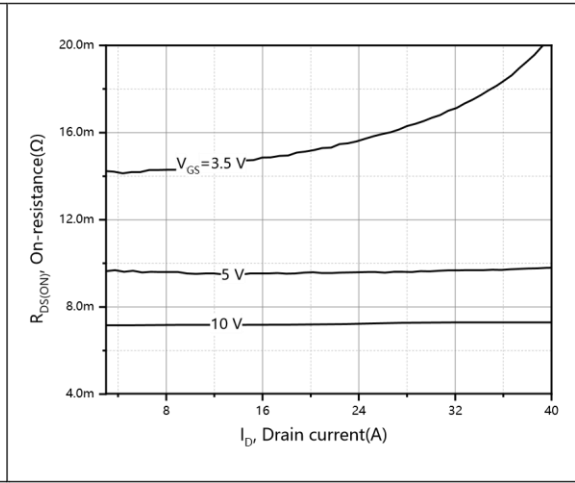


Figure 8, Drain-source on-state resistance

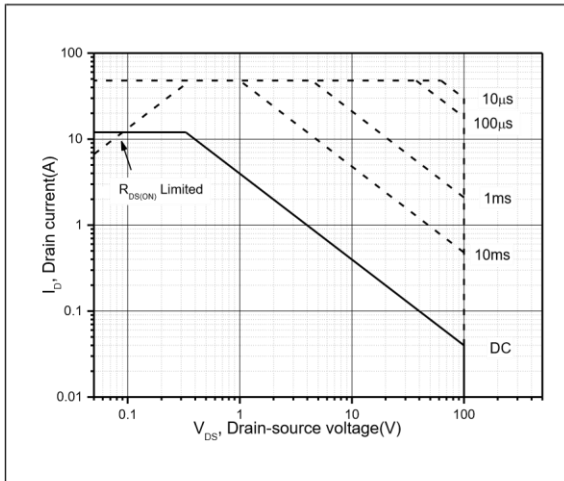


Figure 9, Safe operation area $T_C=25\text{ °C}$

Test circuits and waveforms

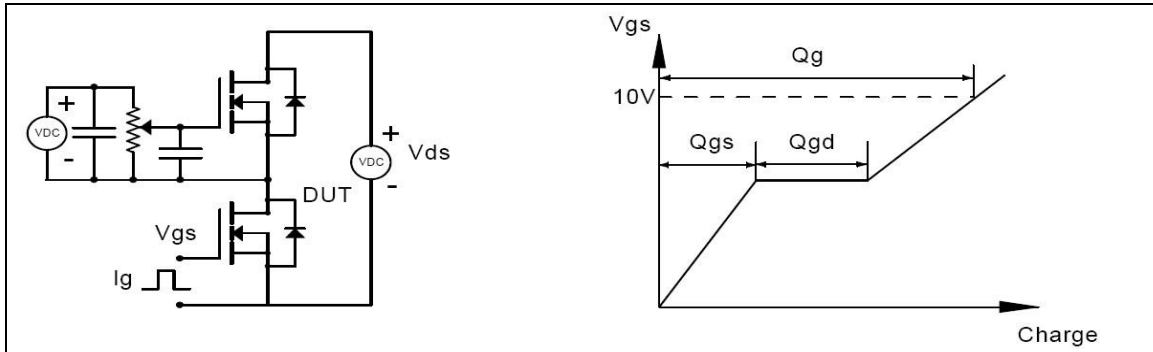


Figure 1, Gate charge test circuit & waveform

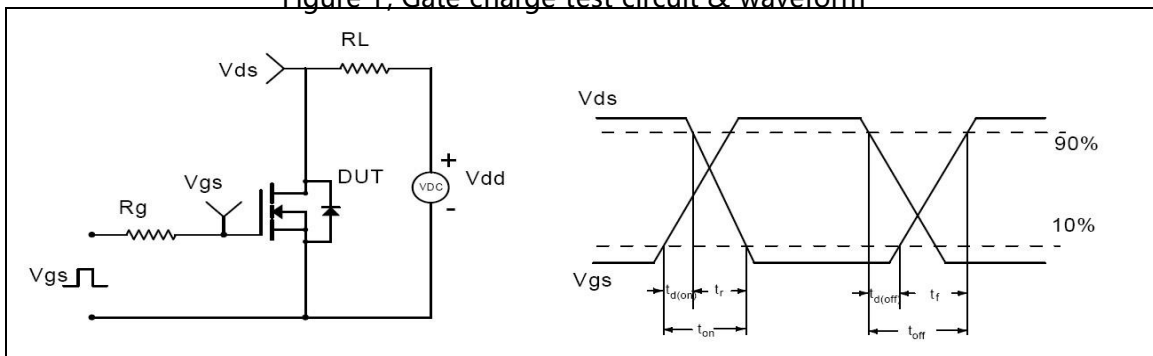


Figure 2, Switching time test circuit & waveforms

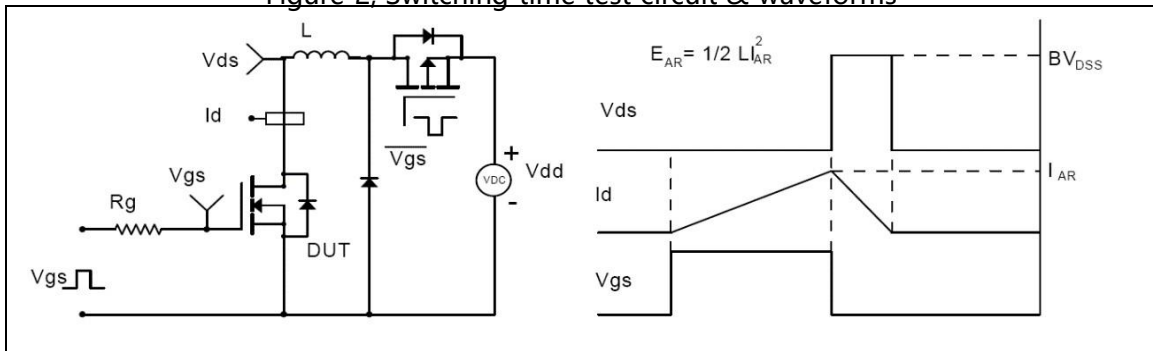


Figure 3, Unclamped inductive switching (UIS) test circuit & waveforms

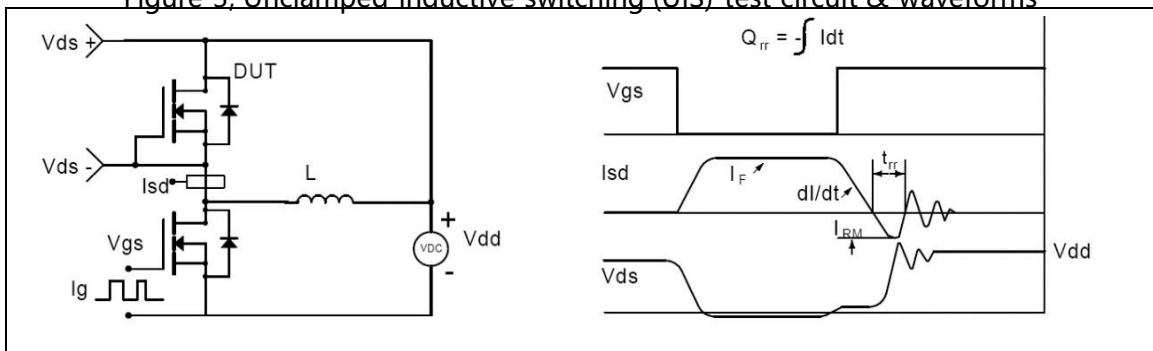
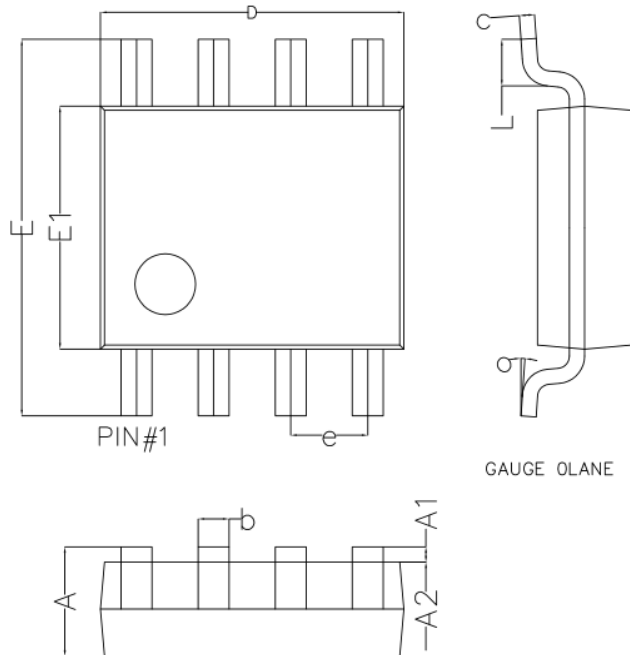


Figure 4, Diode reverse recovery test circuit & waveforms

SOP8 Package outline



Symbol	Dim in mm		
	Min	Nor	Max
A	1.350	1.550	1.750
A1	0.100	0.175	0.250
A2	1.350	1.450	1.550
b	0.330	0.420	0.510
c	0.170	0.210	0.250
D	4.800	4.900	5.000
e	1.270 (BSC)		
E	5.800	6.000	6.200
E1	3.800	3.900	4.000
L	0.400	0.835	1.2700
o	0°	4°	8°

60V N-SGT Enhancement Mode MOSFET

Attention

1, Any and all APM Microelectronics products described or contained herein do not have specifications that can handle applications that require extremely high levels of reliability, such as life support systems, aircraft's control systems, or other applications whose failure can be reasonably expected to result in serious physical and/or material damage. Consult with your APM Microelectronics representative nearest you before using any APM Microelectronics products described or contained herein in such applications.

2, APM Microelectronics assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all APM Microelectronics products described or contained herein.

3, Specifications of any and all APM Microelectronics products described or contained here instipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer's products or equipment.

4, APM Microelectronics Semiconductor CO., LTD. strives to supply high quality high reliability products. However, any and all semiconductor products fail with some probability. It is possible that these probabilistic failures could give rise to accidents or events that could endanger human lives that could give rise to smoke or fire, or that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.

5, In the event that any or all APM Microelectronics products (including technical data, services) described or contained herein are controlled under any of applicable local export control laws and regulations, such products must not be exported without obtaining the export license from the authorities concerned in accordance with the above law.

6, No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written permission of APM Microelectronics Semiconductor CO., LTD.

7, Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. APM Microelectronics believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

8, Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the APM Microelectronics product that you intend to use.