

60V N-SGT Enhancement Mode MOSFET

General Description

APG130N06NF use advanced SGT MOSFET technology to provide low RDS(ON), low gate charge, fast switching and excellent avalanche characteristics.

This device is specially designed to get better ruggedness and suitable to use in

Features

Low RDS(on) & FOM

Extremely low switching loss

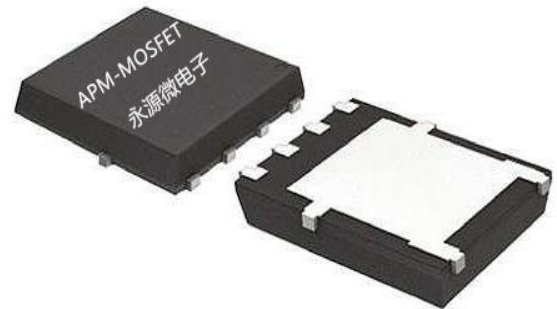
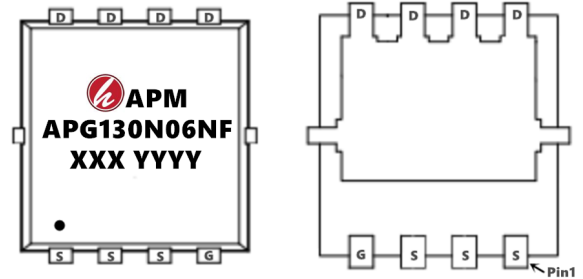
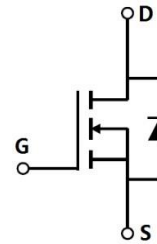
Excellent stability and uniformity or Invertors

Applications

Consumer electronic power supply Motor control

Synchronous-rectification Isolated DC

Synchronous-rectification applications



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
APG130N06NF	PDFN5*6-8L	APG130N06NF	5000

Absolute Maximum Ratings at $T_j=25^{\circ}\text{C}$ unless otherwise noted

Parameter	Symbol	Value	Unit
Drain source voltage	VDS	60	V
Gate source voltage	VGS	± 20	V
Continuous drain current ¹⁾	ID	130	A
Pulsed drain current ²⁾	ID, pulse	390	A
Power dissipation ³⁾	P _D	140	W
Single pulsed avalanche energy ⁵⁾	EAS	80	mJ
Operation and storage temperature	Tstg, T _j	-55 to 150	$^{\circ}\text{C}$
Thermal resistance, junction-case	R θ JC	0.89	$^{\circ}\text{C}/\text{W}$
Thermal resistance, junction-ambient ⁴⁾	R θ JA	62	$^{\circ}\text{C}/\text{W}$

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Electrical Characteristics at $T_j=25\text{ }^\circ\text{C}$ unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Drain-source breakdown voltage	BVDSS	60			V	$V_{GS}=0\text{ V}$, $I_D=250\text{ }\mu\text{A}$
Gate threshold voltage	$V_{GS(th)}$	1.0		2.5	V	$V_{DS}=V_{GS}$, $I_D=250\text{ }\mu\text{A}$
Drain-source on-state resistance	$R_{DS(ON)}$		2.5	3.0	$\text{m}\Omega$	$V_{GS}=10\text{ V}$, $I_D=20\text{ A}$
Drain-source on-state resistance	$R_{DS(ON)}$		3.5	4.5	$\text{m}\Omega$	$V_{GS}=4.5\text{ V}$, $I_D=10\text{ A}$
Gate-source leakage current	IGSS			100	nA	$V_{GS}=20\text{ V}$
				-100		$V_{GS}=-20\text{ V}$
Drain-source leakage current	IDSS			1	μA	$V_{DS}=60\text{ V}$, $V_{GS}=0\text{ V}$
Input capacitance	Ciss		5377		pF	$V_{GS}=0\text{ V}$, $V_{DS}=25\text{ V}$, $f=100\text{ kHz}$
Output capacitance	Coss		1666		pF	
Reverse transfer capacitance	Crss		77.7		pF	
Turn-on delay time	$t_{d(on)}$		22.5		ns	$V_{GS}=10\text{ V}$, $V_{DS}=30\text{ V}$, $R_G=2\text{ }\Omega$, $I_D=25\text{ A}$
Rise time	t_r		6.7		ns	
Turn-off delay time	$t_{d(off)}$		80.3		ns	
Fall time	t_f		26.8		ns	
Gate-source charge	Q_{gs}		10.7		nC	$I_D=25\text{ A}$, $V_{DS}=30\text{ V}$, $V_{GS}=10\text{ V}$
Gate-drain charge	Q_{gd}		10.9		nC	
Gate plateau voltage	$V_{plateau}$		2.9		V	
Diode forward current	I_s			130	A	$V_{GS}<V_{th}$
Pulsed source current	ISP			390		
Diode forward voltage	VSD			1.3	V	$I_s=20\text{ A}$, $V_{GS}=0\text{ V}$
Reverse recovery time	t_{rr}		68.3		ns	$I_s=25\text{ A}$, $di/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge	Q_{rr}		73.0		nC	
Peak reverse recovery current	I_{rrm}		1.9		A	

Note

- 1) Calculated continuous current based on maximum allowable junction temperature.
- 2) Repetitive rating; pulse width limited by max. junction temperature.
- 3) P_d is based on max. junction temperature, using junction-case thermal resistance.
- 4) The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_a=25\text{ }^\circ\text{C}$.
- 5) $V_{DD}=50\text{ V}$, $R_G=25\text{ }\Omega$, $L=0.3\text{ mH}$, starting $T_j=25\text{ }^\circ\text{C}$.

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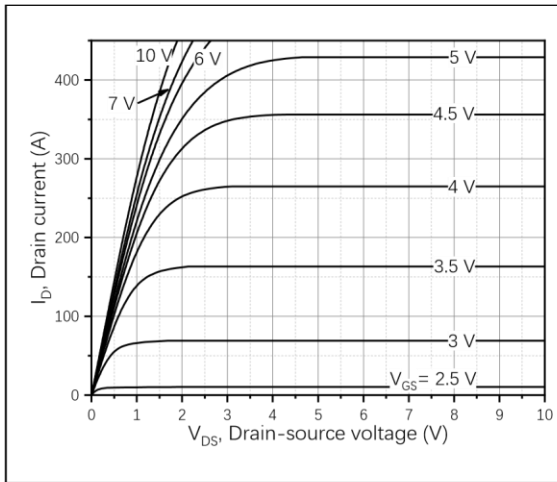


Figure 1, Typ. output characteristics

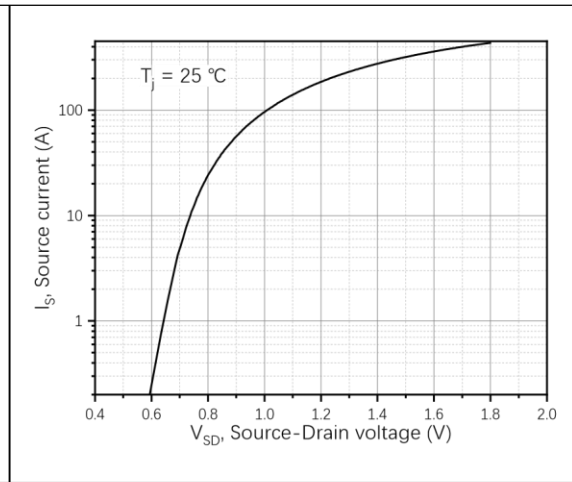


Figure 2, Typ. transfer characteristics

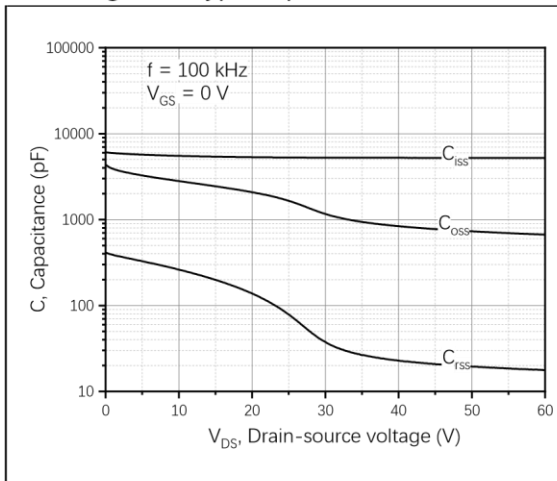


Figure 3, Typ. capacitances

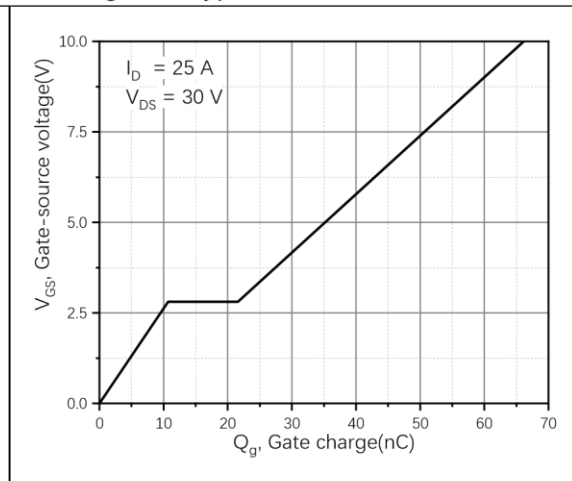


Figure 4, Typ. gate charge

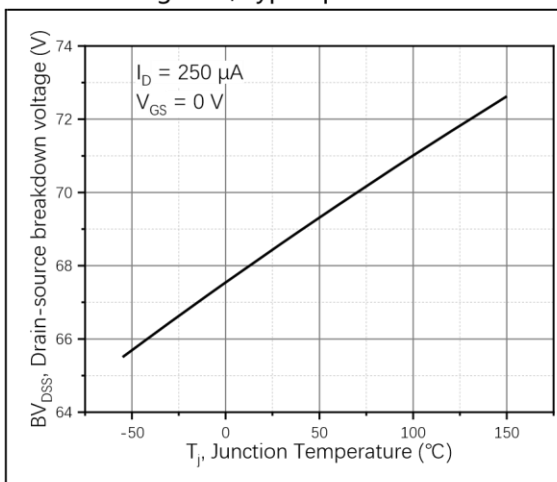


Figure 5, Drain-source breakdown voltage

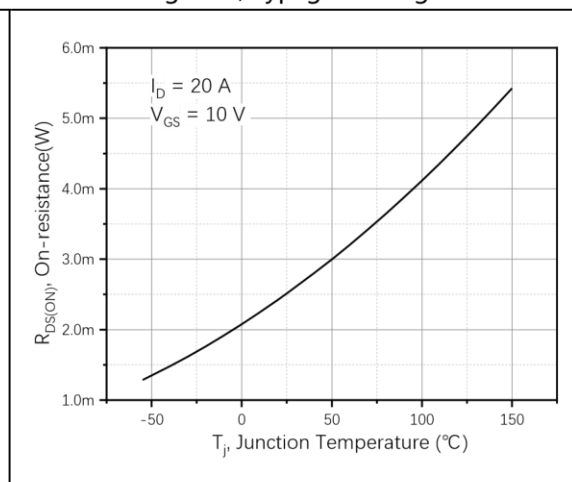


Figure 6, Drain-source on-state resistance

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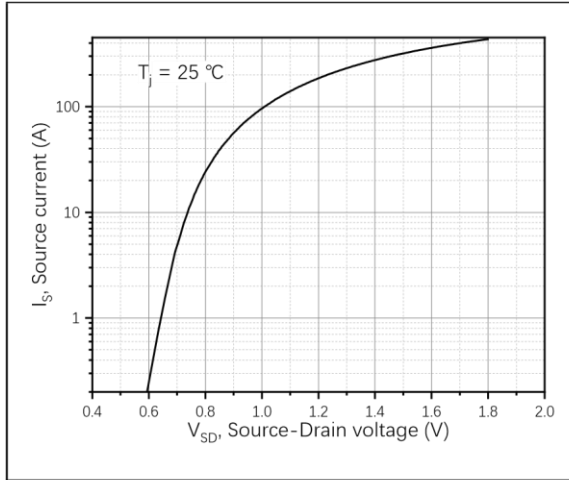


Figure 7, Forward characteristic of body diode

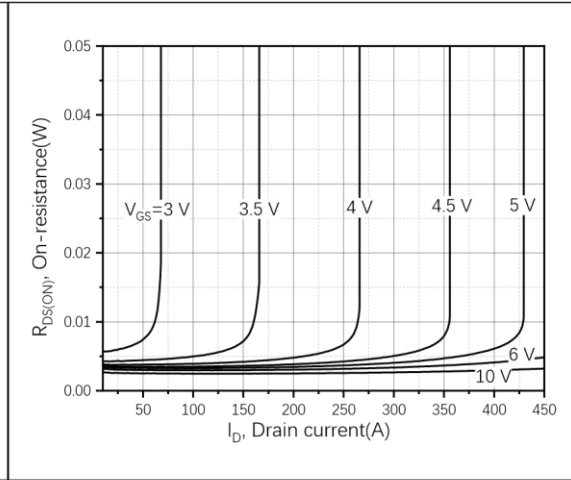


Figure 8, Drain-source on-state resistance

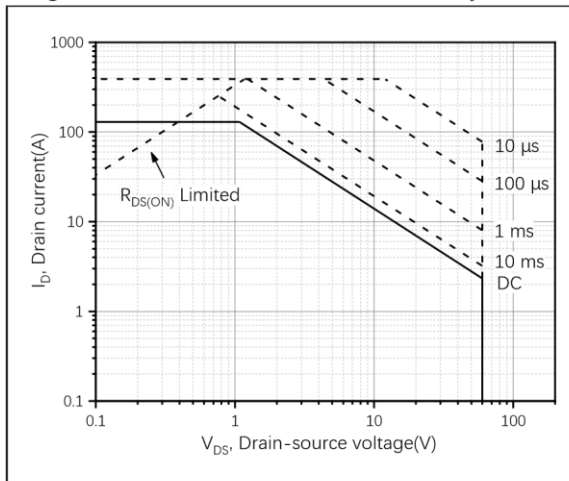


Figure 9, Safe operation area $T_C=25\text{ }^\circ\text{C}$

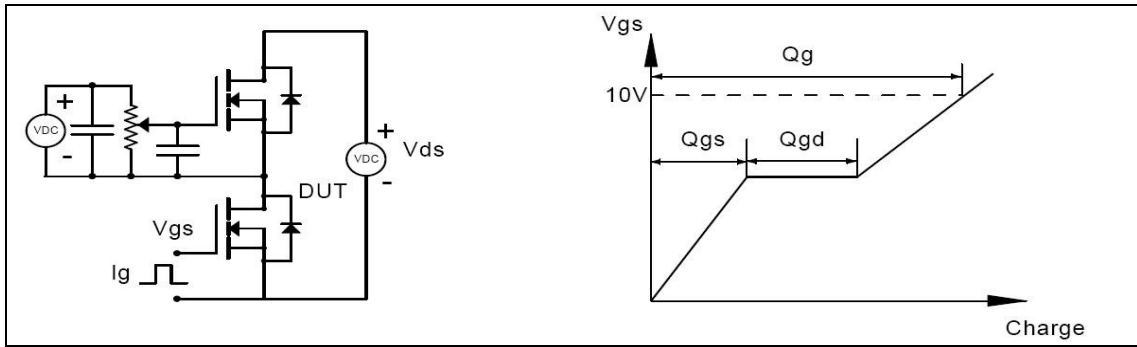


Figure 1, Gate charge test circuit & waveform

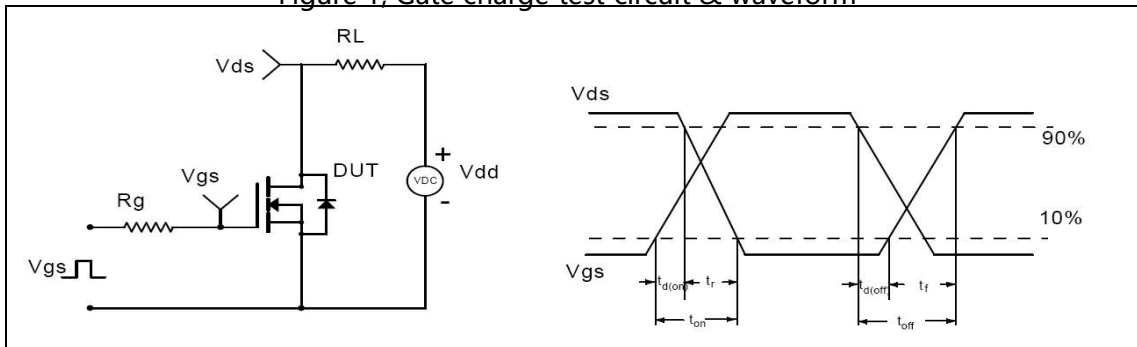


Figure 2, Switching time test circuit & waveforms

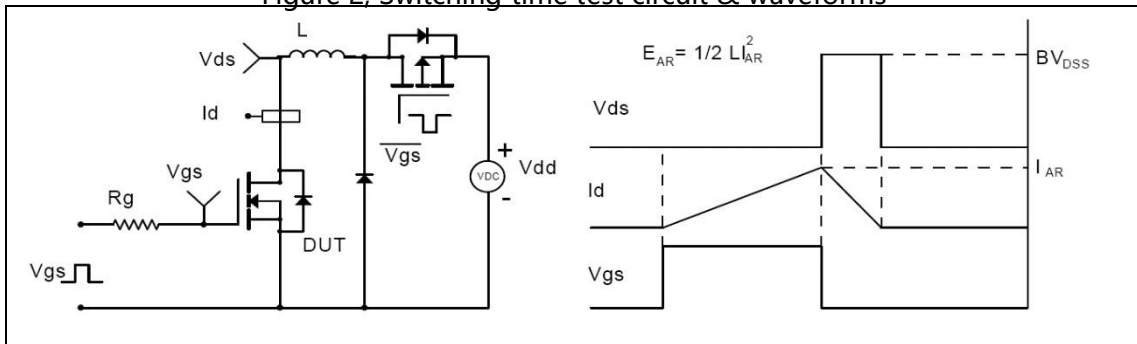


Figure 3, Unclamped inductive switching (UIS) test circuit & waveforms

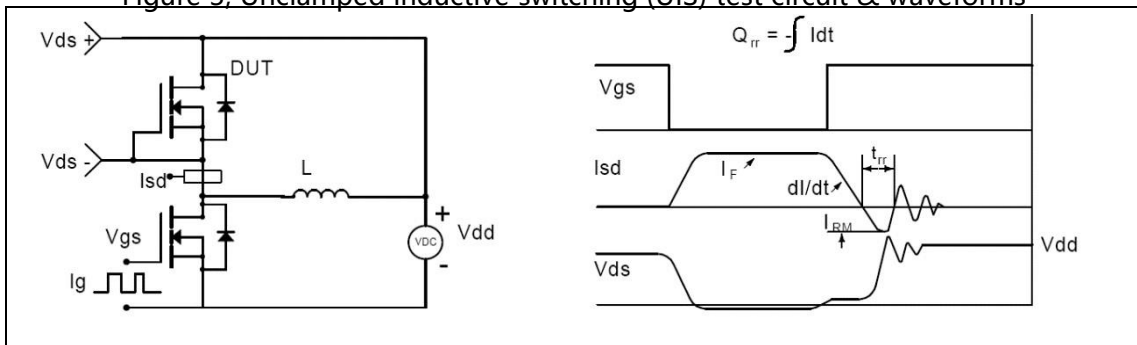
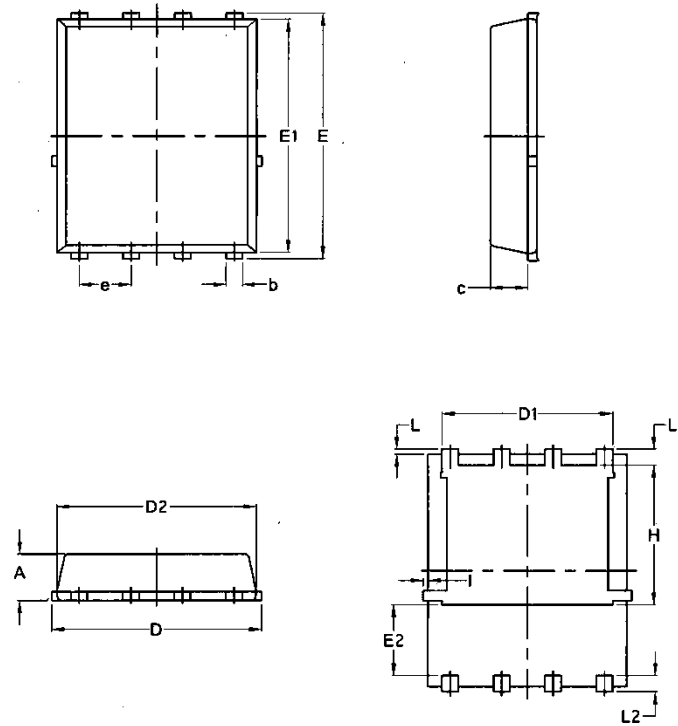


Figure 4, Diode reverse recovery test circuit & waveforms

Package Mechanical Data-DFN5*6-8L-JQ Single



Symbol	Common			
	mm		Inch	
	Min	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070

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