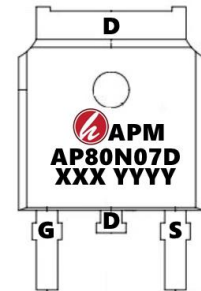
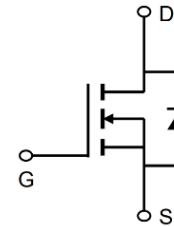


68V N-Channel Enhancement Mode MOSFET

Description

The AP80N07D uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.



General Features

$V_{DS} = 68V$ $I_D = 80A$

$R_{DS(ON)} < 8.6m\Omega$ @ $V_{GS}=10V$ (Type: $6.5m\Omega$)

Application

- Battery protection
- Load switch
- Uninterruptible power supply



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP80N07D	TO-252-3L	AP80N07D XXX YYYY	2500

Absolute Maximum Ratings ($T_C=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	68	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_C=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	80	A
$I_D@T_C=100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	52	A
IDM	Pulsed Drain Current ²	320	A
EAS	Single Pulse Avalanche Energy ³	121	mJ
IAS	Avalanche Current	22	A
$P_D@T_C=25^\circ C$	Total Power Dissipation ⁴	116	W
TSTG	Storage Temperature Range	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ C$
$R_{\theta JA}$	Thermal Resistance Junction-ambient ¹	63	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	0.85	$^\circ C/W$

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Electrical Characteristics (T_J=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	68	72	---	V
ΔBVDSS/ΔT _J	BVDSS Temperature Coefficient	Reference to 25°C, I _D =1mA	---	0.023	---	V/°C
RDS(ON)	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =10A	---	6.5	8.6	mΩ
VGS(th)	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =250uA	2.0	3.0	4.0	V
ΔVGS(th)	VGS(th) Temperature Coefficient		---	-4.2	---	mV/°C
IDSS	Drain-Source Leakage Current	V _{DS} =24V, V _{GS} =0V, T _J =25°C	---	---	1	uA
		V _{DS} =24V, V _{GS} =0V, T _J =55°C	---	---	5	
IGSS	Gate-Source Leakage Current	V _{GS} =±20V, V _{DS} =0V	---	---	±100	nA
gfs	Forward Transconductance	V _{DS} =5V, I _D =10A	---	5.5	---	S
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz	---	2.3	---	Ω
Q _g	Total Gate Charge (4.5V)	V _{DS} =30V, I _D =20A, V _{GS} =10V	---	35	---	nC
Q _{gs}	Gate-Source Charge		---	11	---	
Q _{gd}	Gate-Drain Charge		---	9	---	
Td(on)	Turn-On Delay Time	V _{DS} =30V, I _D =20A, R _{GEN} =6Ω, V _{GS} =10V	---	15	---	ns
T _r	Rise Time		---	94	---	
Td(off)	Turn-Off Delay Time		---	46	---	
T _f	Fall Time		---	32	---	
Ciss	Input Capacitance	V _{DS} =15V, V _{GS} =0V, f=1MHz	---	4062	---	pF
Coss	Output Capacitance		---	261	---	
Crss	Reverse Transfer Capacitance		---	231	---	
I _S	Continuous Source Current ^{1,5}	V _G =V _D =0V, Force Current	---	---	80	A
I _{SM}	Pulsed Source Current ^{2,5}		---	---	320	A
VSD	Diode Forward Voltage ²	V _{GS} =0V, I _S =80A	---	---	1.2	V
trr	Reverse Recovery Time	T _J =25°C I _F =20A, dI/dt=100A/μs	---	78	---	nS
Q _{rr}	Reverse Recovery Charge		---	51	---	nC

Note :

- 1、 The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2、 The data tested by pulsed , pulse width .The EAS data shows Max. rating .
- 3、 The test cond ≅ 300us duty cycle ≅ 2%, duty cycle ition is T_J =25°C, V_{DD} =35V, V_G =10V, R_G =25Ω, L=0.5mH, I_{AS} =22A
- 4、 The power dissipation is limited by 175°C junction temperature
- 5、 The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

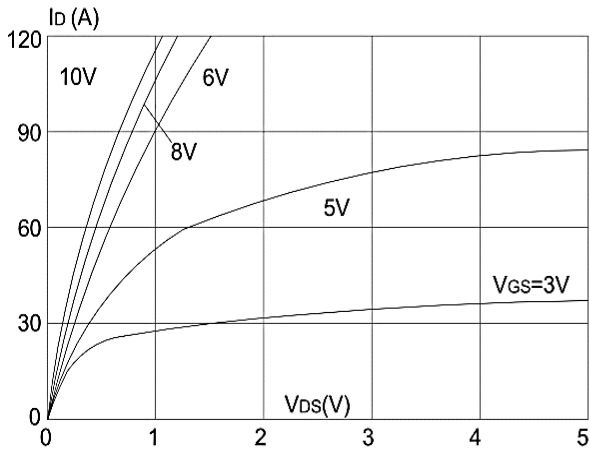


Figure 1: Output Characteristics

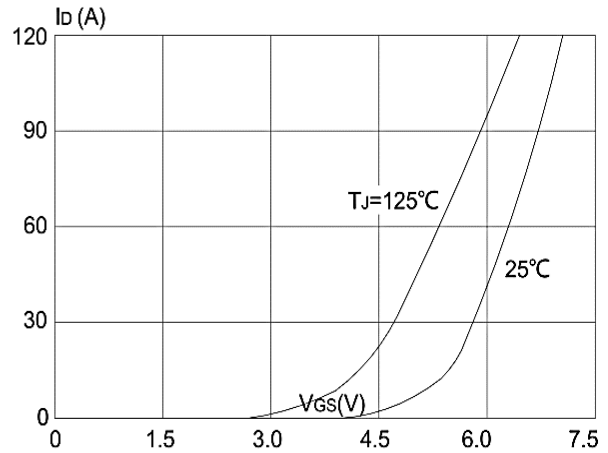


Figure 2: Typical Transfer Characteristics

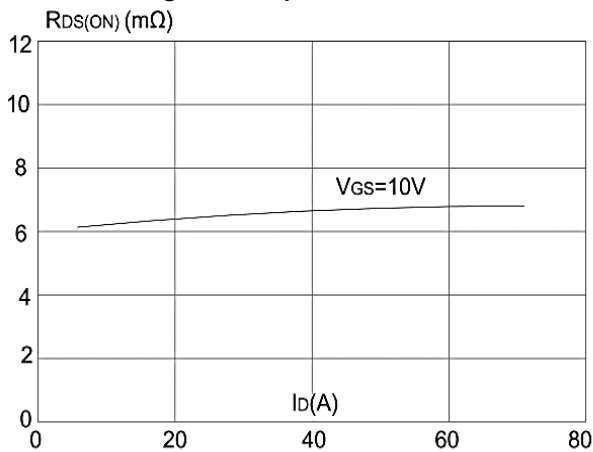


Figure 3: On-resistance vs. Drain Current

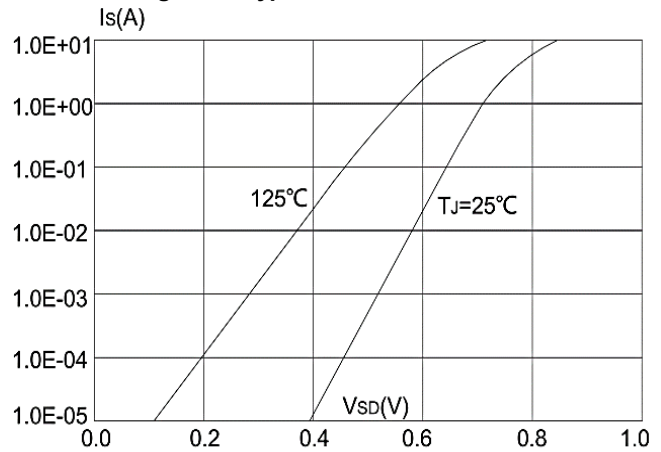


Figure 4: Body Diode Characteristics

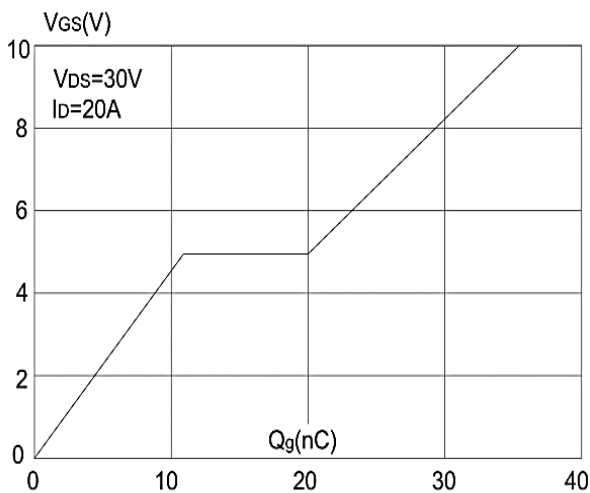


Figure 5: Gate Charge Characteristics

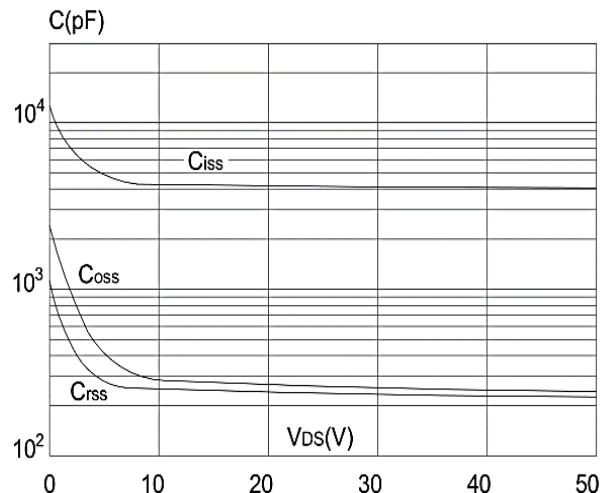


Figure 6: Capacitance Characteristics

68V N-Channel Enhancement Mode MOSFET

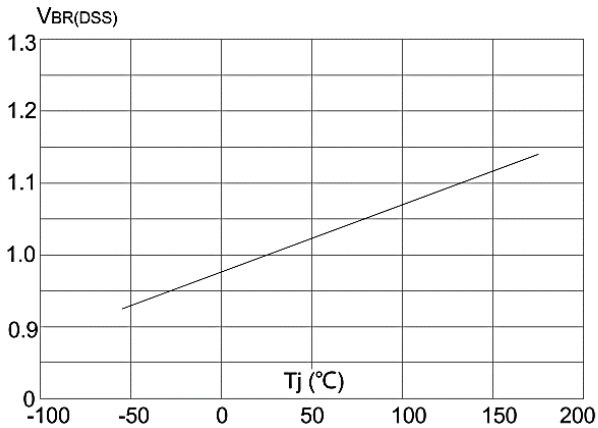


Figure 7: Normalized Breakdown Voltage vs Junction Temperature

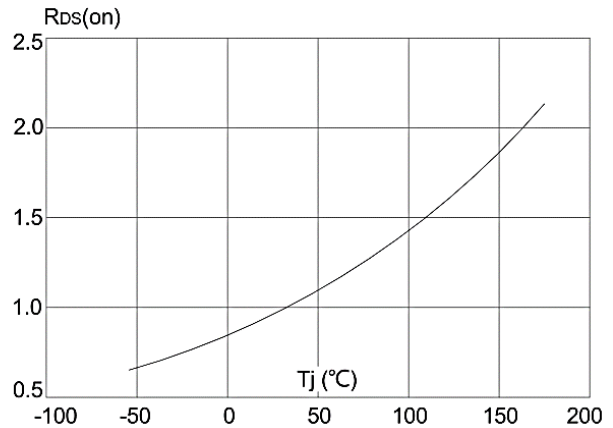


Figure 8: Normalized on Resistance vs. Junction Temperature

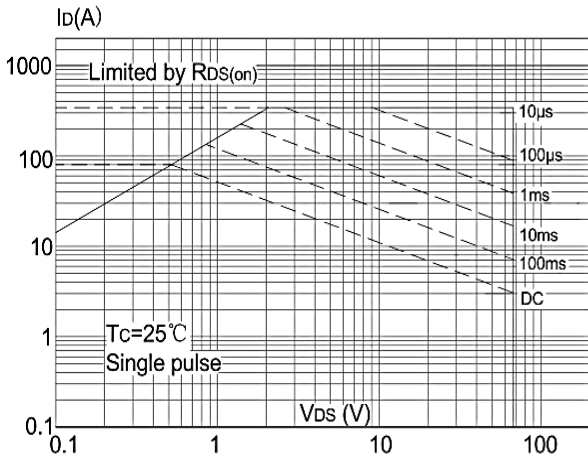


Figure 9: Maximum Safe Operating Area

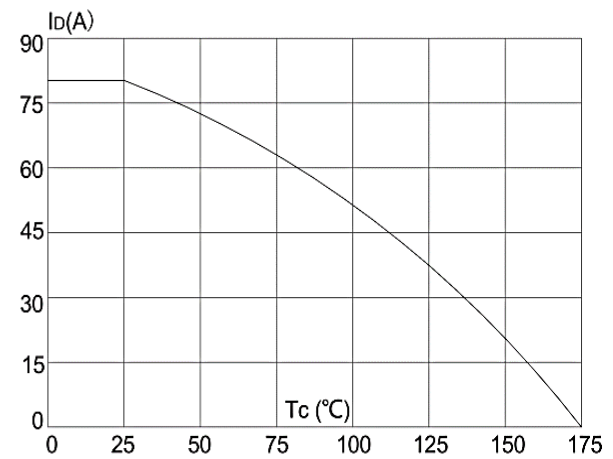


Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature

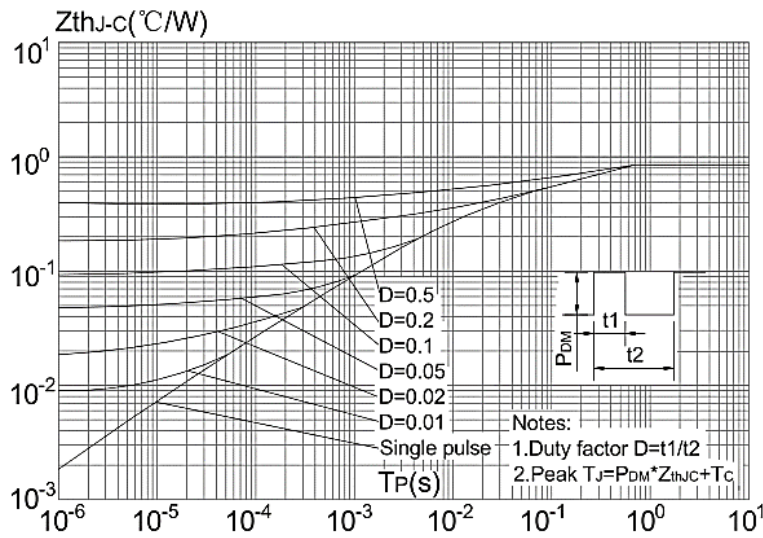
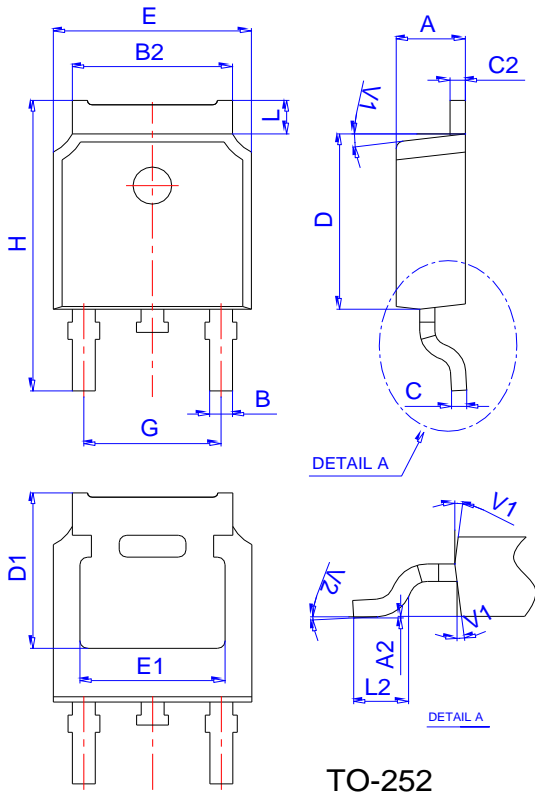


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Ambien

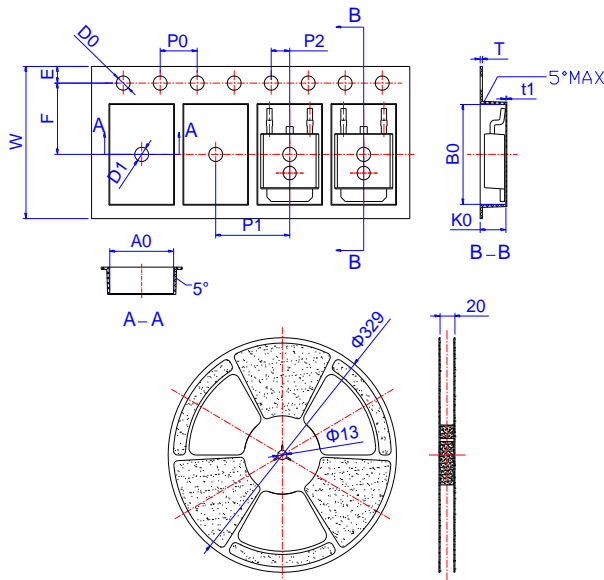
68V N-Channel Enhancement Mode MOSFET

Package Mechanical Data: TO-252-3L



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°

Reel Specification-TO-252



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
W	15.90	16.00	16.10	0.626	0.630	0.634
E	1.65	1.75	1.85	0.065	0.069	0.073
F	7.40	7.50	7.60	0.291	0.295	0.299
D0	1.40	1.50	1.60	0.055	0.059	0.063
D1	1.40	1.50	1.60	0.055	0.059	0.063
P0	3.90	4.00	4.10	0.154	0.157	0.161
P1	7.90	8.00	8.10	0.311	0.315	0.319
P2	1.90	2.00	2.10	0.075	0.079	0.083
A0	6.85	6.90	7.00	0.270	0.271	0.276
B0	10.45	10.50	10.60	0.411	0.413	0.417
K0	2.68	2.78	2.88	0.105	0.109	0.113
T	0.24		0.27	0.009		0.011
t1	0.10			0.004		
10P0	39.80	40.00	40.20	1.567	1.575	1.583

68V N-Channel Enhancement Mode MOSFET**Attention**

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68V N-Channel Enhancement Mode MOSFET

Edition	Date	Change
RVE1.0	2020/12/21	Initial release

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