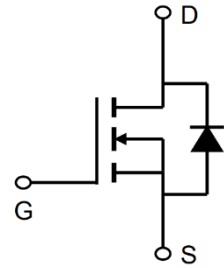


40V N-Channel Enhancement Mode MOSFET

Description

The AP60N04NF uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.



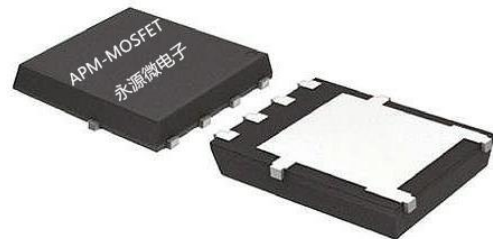
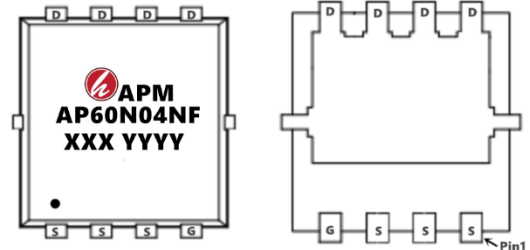
General Features

$V_{DS} = 40V$ $I_D = 60A$

$R_{DS(ON)} < 13.5m\Omega @ V_{GS}=10V$

Application

- Battery protection
- Load switch
- Uninterruptible power supply



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP60N04NF	PDFN5*6-8L	AP60N04NF XXX YYYY	5000

Absolute Maximum Ratings ($T_C=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	40	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D @ T_C=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	60	A
$I_D @ T_C=100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	28	A
$I_D @ T_A=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	10	A
$I_D @ T_A=70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	8	A
I_{DM}	Pulsed Drain Current ²	100	A
EAS	Single Pulse Avalanche Energy ³	20	mJ
I_{AS}	Avalanche Current	20	A
$P_D @ T_C=25^\circ C$	Total Power Dissipation ⁴	46	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ C$
$R_{\theta JA}$	Thermal Resistance Junction-ambient (Steady State) ¹	62	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	2.7	$^\circ C/W$



40V N-Channel Enhancement Mode MOSFET

Electrical Characteristics (T_J=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	40	45	---	V
ΔBVDSS/ΔT _J	BVDSS Temperature Coefficient	Reference to 25°C, I _D =1mA	---	0.034	---	V/°C
RDS(ON)	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =20A	---	10.5	13.5	mΩ
		V _{GS} =4.5V, I _D =10A	---	13.5	16.5	
VGS(th)	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =250uA	1.0	1.6	2.5	V
ΔVGS(th)	VGS(th) Temperature Coefficient		---	-5.64	---	mV/°C
IDSS	Drain-Source Leakage Current	V _{DS} =32V, V _{GS} =0V, T _J =25°C	---	---	1	uA
		V _{DS} =32V, V _{GS} =0V, T _J =55°C	---	---	5	
IGSS	Gate-Source Leakage Current	V _{GS} =±20V, V _{DS} =0V	---	---	±100	nA
gfs	Forward Transconductance	V _{DS} =5V, I _D =20A	---	36	---	S
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz	---	2.1	---	Ω
Q _g	Total Gate Charge (4.5V)	V _{DS} =20V, V _{GS} =4.5V, I _D =12A	---	10.7	---	nC
Q _{gs}	Gate-Source Charge		---	3.3	---	
Q _{gd}	Gate-Drain Charge		---	4.2	---	
Td(on)	Turn-On Delay Time	V _{DD} =12V, V _{GS} =10V, R _G =3.3Ω I _D =6A	---	8.6	---	ns
T _r	Rise Time		---	3.4	---	
Td(off)	Turn-Off Delay Time		---	25	---	
T _f	Fall Time		---	2.2	---	
Ciss	Input Capacitance	V _{DS} =15V, V _{GS} =0V, f=1MHz	---	1314	---	pF
Coss	Output Capacitance		---	120	---	
Crss	Reverse Transfer Capacitance		---	88	---	
IS	Continuous Source Current ^{1,5}	V _G =V _D =0V, Force Current	---	---	46	A
ISM	Pulsed Source Current ^{2,5}		---	---	100	A
VSD	Diode Forward Voltage ²	V _{GS} =0V, I _S =1A, T _J =25°C	---	---	1.2	V

Note :

- 1、The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2、The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%
- 3、The EAS data shows Max. rating. The test condition is V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=20A
- 4、The power dissipation is limited by 150°C junction temperature
- 5、The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

40V N-Channel Enhancement Mode MOSFET

Typical Characteristics

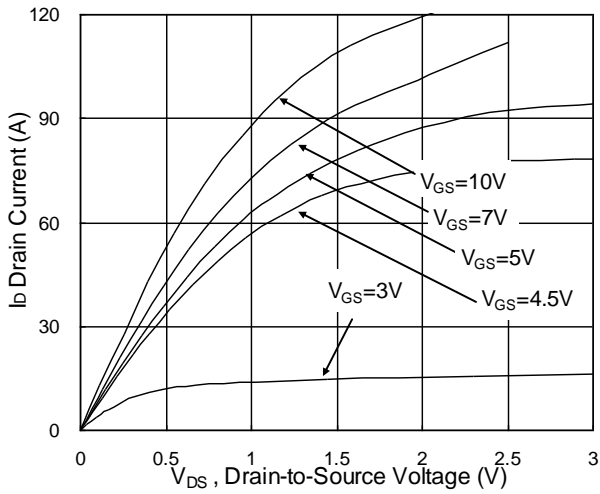


Fig.1 Typical Output Characteristics

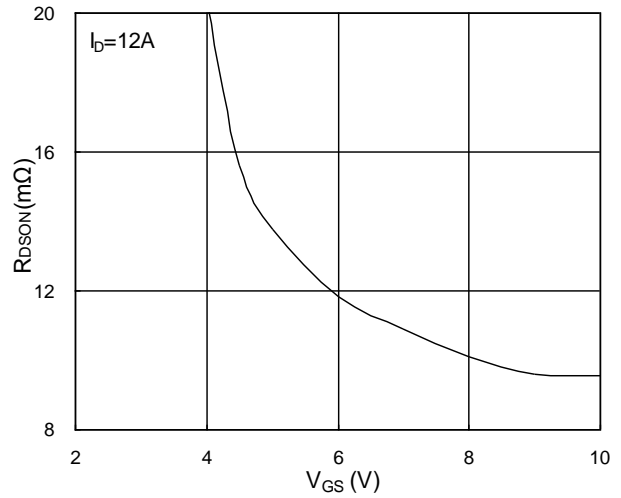


Fig.2 On-Resistance vs. G-S Voltage

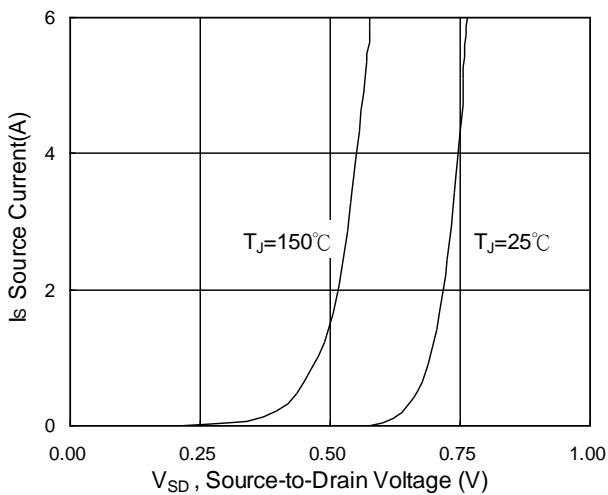


Fig.3 Forward Characteristics of Reverse

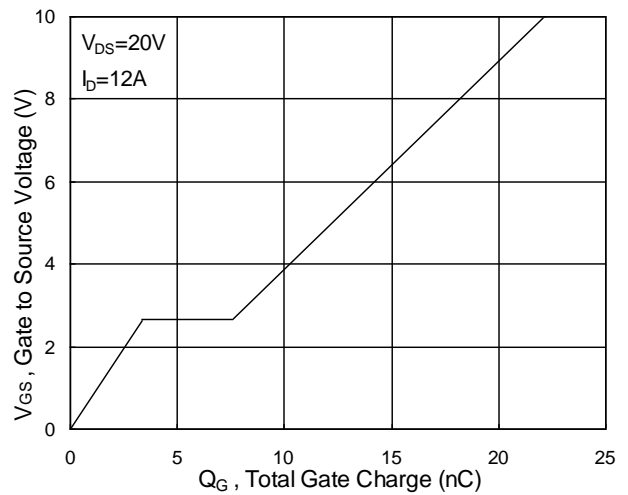


Fig.4 Gate-Charge Characteristics

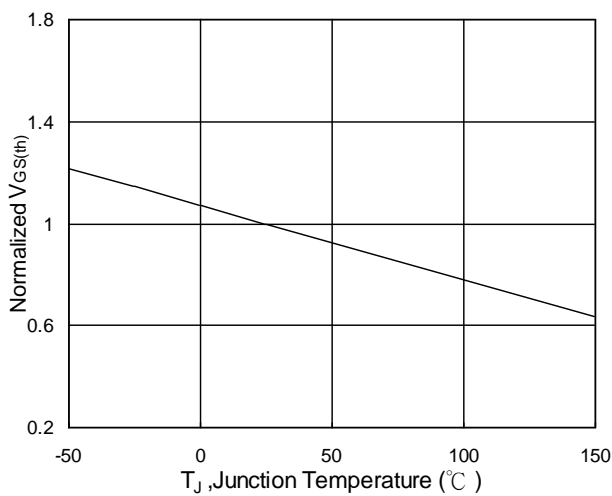


Fig.5 $V_{GS(th)}$ vs. T_J

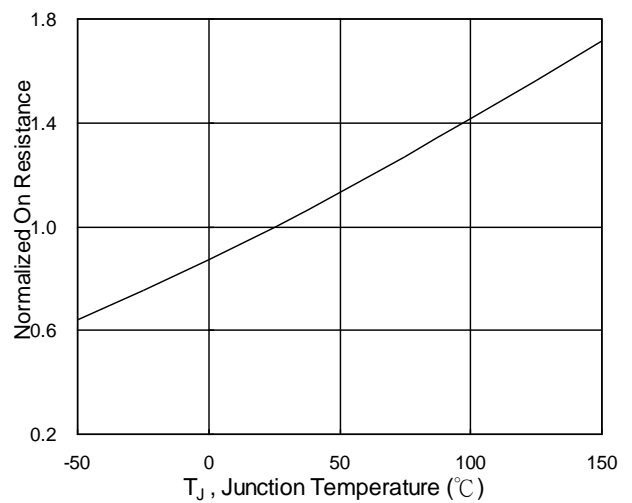


Fig.6 Normalized $R_{DS(on)}$ vs. T_J



40V N-Channel Enhancement Mode MOSFET

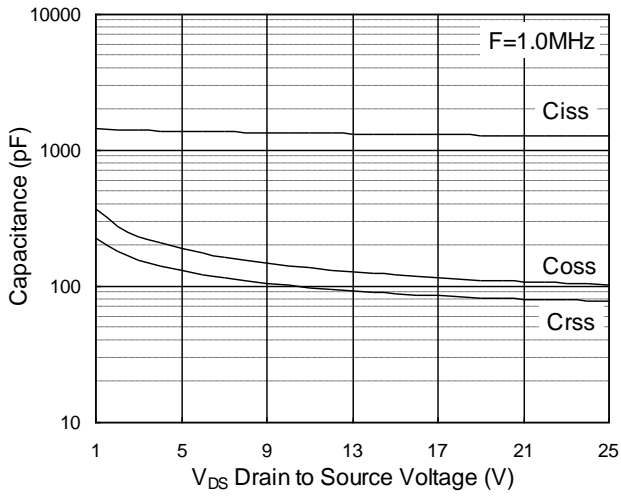


Fig.7 Capacitance

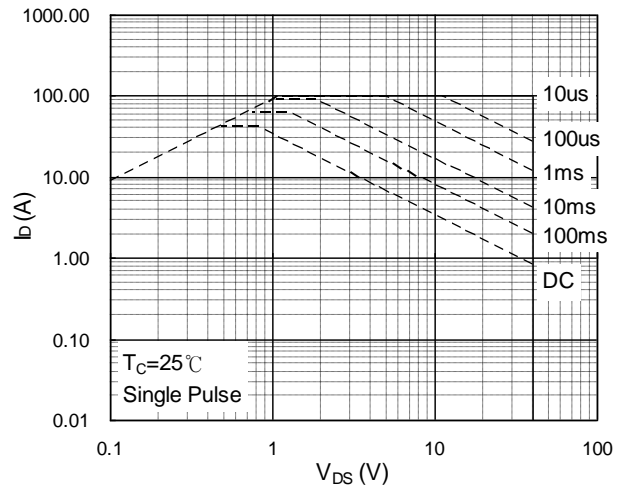


Fig.8 Safe Operating Area

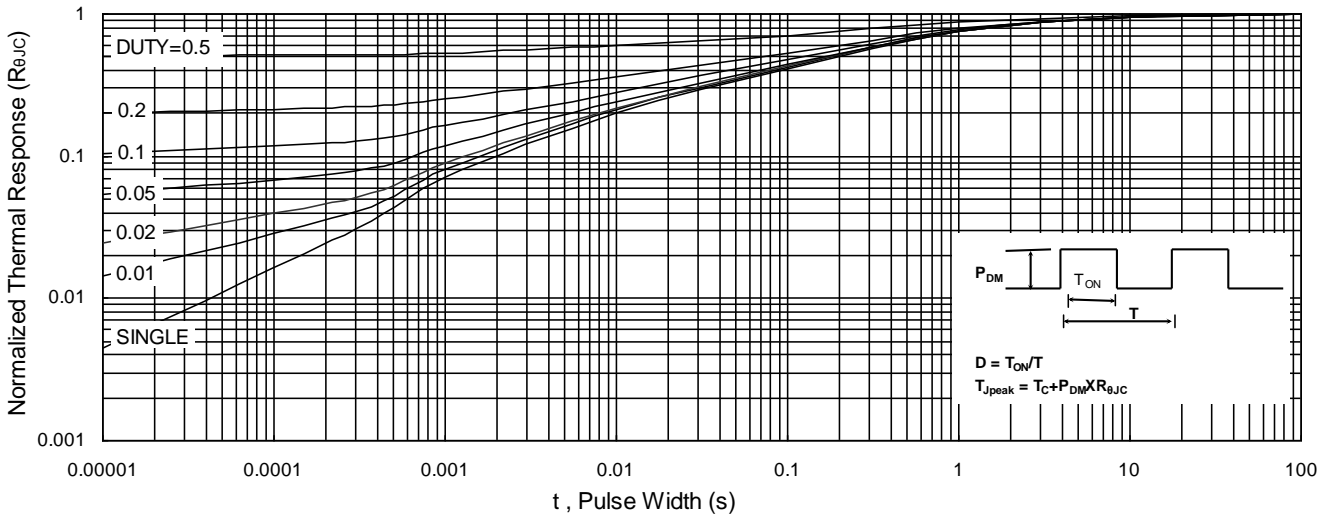


Fig.9 Normalized Maximum Transient Thermal Impedance

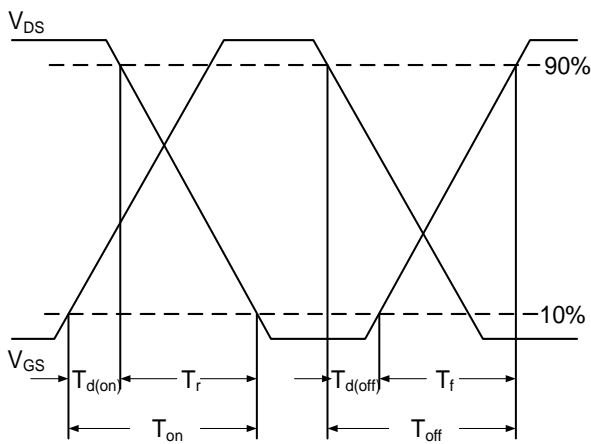


Fig.10 Switching Time Waveform

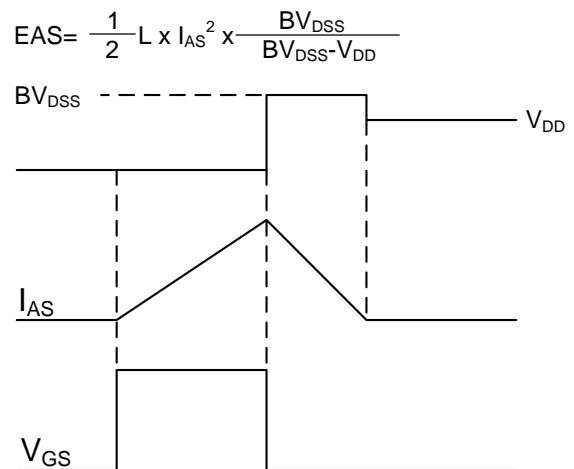
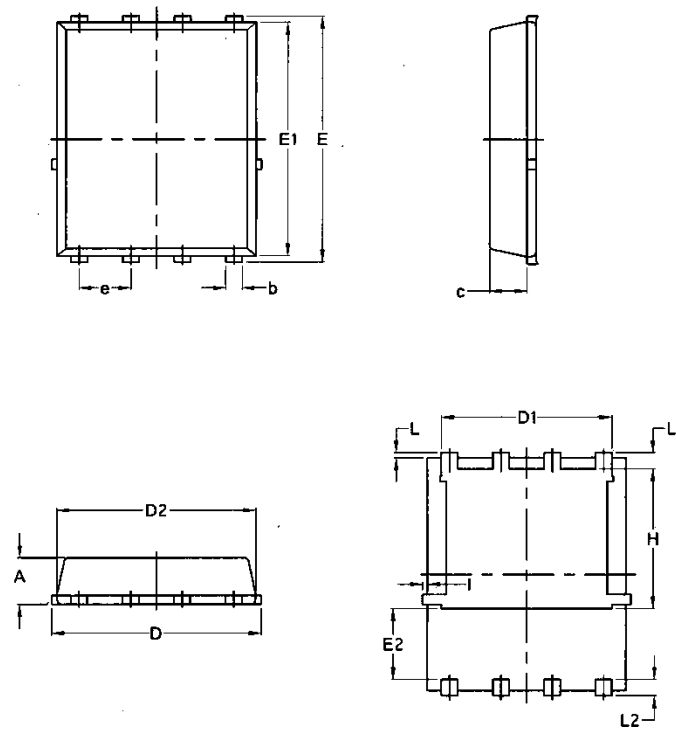


Fig.11 Unclamped Inductive Switching Waveform

40V N-Channel Enhancement Mode MOSFET Package Mechanical Data-DFN5*6-8L-JQ Single



Symbol	Common			
	mm		Inch	
	Min	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070

40V N-Channel Enhancement Mode MOSFET**Attention**

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40V N-Channel Enhancement Mode MOSFET

Edition	Date	Change
Rve1.0	2019/8/1	Initial release

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