

30V N-Channel Enhancement Mode MOSFET

Description

The AP60N03P uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

$V_{DS} = 30V$ $I_D = 60A$

$R_{DS(ON)} < 12m\Omega$ @ $V_{GS} = 10V$

Application

Battery protection
 Load switch
 Uninterruptible power supply



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP60N03P	TO-220-3L	AP60N03P XXX YYYY	1000

Absolute Maximum Ratings (TC=25°C unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	30	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	60	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	33	A
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	10.3	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	8.3	A
I_{DM}	Pulsed Drain Current ²	112	A
EAS	Single Pulse Avalanche Energy ³	24	mJ
I_{AS}	Avalanche Current	22	A
$P_D @ T_C = 25^\circ C$	Total Power Dissipation ⁴	52.1	W
$P_D @ T_A = 25^\circ C$	Total Power Dissipation ⁴	2	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ C$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	62	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	2.4	$^\circ C/W$



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Electrical Characteristics (at $T_J=25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	30	---	---	V
$\Delta BVDSS/\Delta T_J$	BVDSS Temperature Coefficient	Reference to 25°C , $I_D=1\text{mA}$	---	0.0193	---	$V/^\circ\text{C}$
RDS(ON)	Static Drain-Source On-Resistance ²	$V_{GS}=10V, I_D=30A$	---	---	12	m Ω
		$V_{GS}=4.5V, I_D=15A$	---	---	18	
VGS(th)	Gate Threshold Voltage		1.2	---	2.5	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient	$V_{GS}=V_{DS}, I_D=250\mu A$	---	-3.97	---	mV/ $^\circ\text{C}$
IDSS	Drain-Source Leakage Current	$V_{DS}=24V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	1	uA
		$V_{DS}=24V, V_{GS}=0V, T_J=55^\circ\text{C}$	---	---	5	
IGSS	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	± 100	nA
gfs	Forward Transconductance	$V_{DS}=5V, I_D=30A$	---	34	---	S
Rg	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1\text{MHz}$	---	1.8	---	Ω
Qg	Total Gate Charge (4.5V)	$V_{DS}=15V, V_{GS}=4.5V, I_D=15A$	---	9.8	---	nC
Qgs	Gate-Source Charge		---	4.2	---	
Qgd	Gate-Drain Charge		---	3.6	---	
Td(on)	Turn-On Delay Time	$V_{DD}=15V, V_{GS}=10V, R_G=3.3\Omega, I_D=15A$	---	4	---	ns
Tr	Rise Time		---	8	---	
Td(off)	Turn-Off Delay Time		---	31	---	
Tf	Fall Time		---	4	---	
Ciss	Input Capacitance	$V_{DS}=15V, V_{GS}=0V, f=1\text{MHz}$	---	940	---	pF
Coss	Output Capacitance		---	131	---	
IS	Continuous Source Current ^{1,5}		---	---	53	
ISM	Pulsed Source Current ^{2,5}	$V_{GS}=0V, I_S=1A, T_J=25^\circ\text{C}$	---	---	112	A
VSD	Diode Forward Voltage ²		---	---	1	V
trr	Reverse Recovery Time		---	8.5	---	nS
Qrr	Reverse Recovery Charge	$I_F=30A, di/dt=100A/\mu s, T_J=25^\circ\text{C}$	---	2.2	---	nC

Note :

- The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- The EAS data shows Max. rating . The test condition is $V_{DD}=25V, V_{GS}=10V, L=0.1\text{mH}, I_{AS}=15A$
- The power dissipation is limited by 150°C junction temperature
- The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

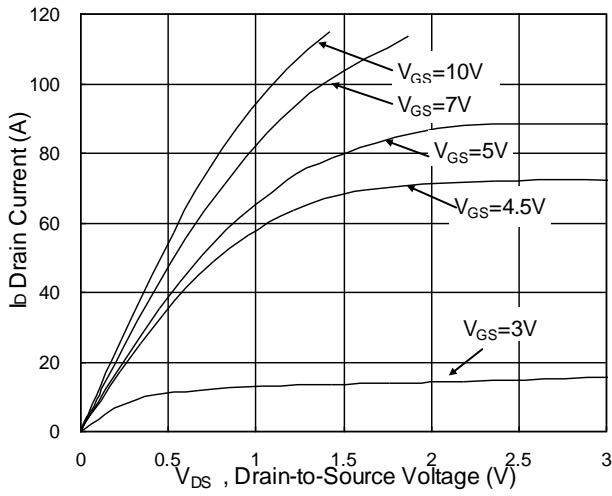


Fig.1 Typical Output Characteristics

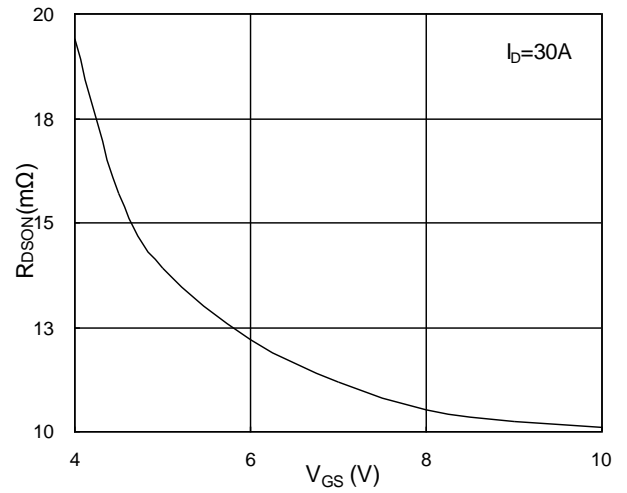


Fig.2 On-Resistance vs. G-S Voltage

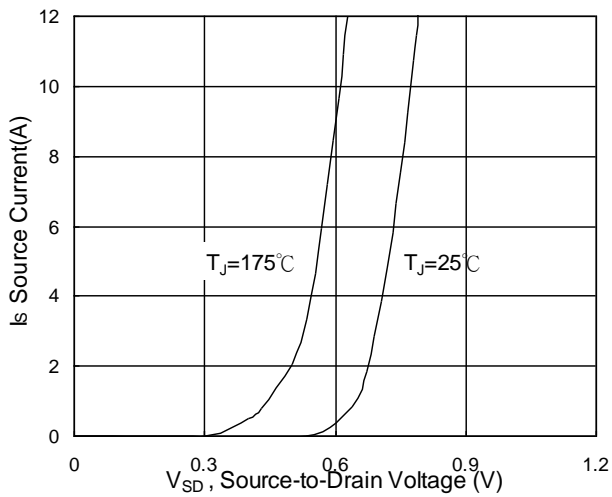


Fig.3 Forward Characteristics of Reverse

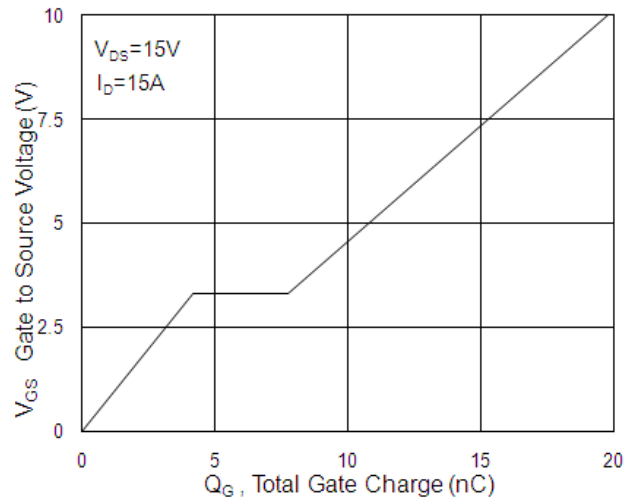


Fig.4 Gate-Charge Characteristics

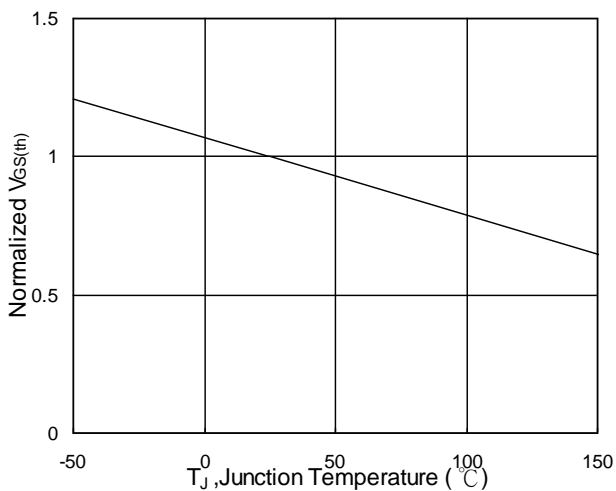


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

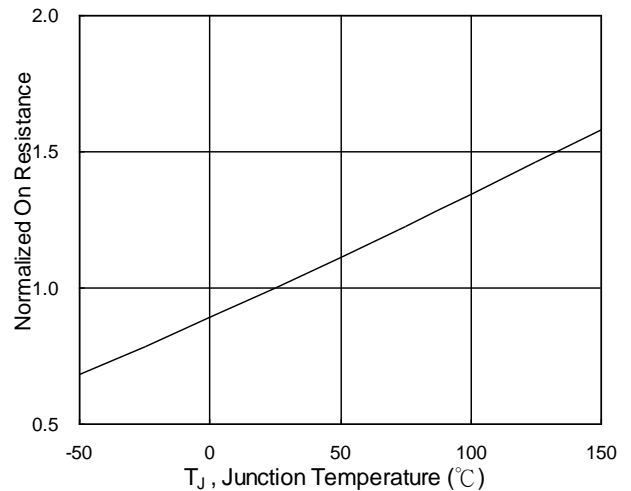


Fig.6 Normalized $R_{DS(on)}$ vs. T_J



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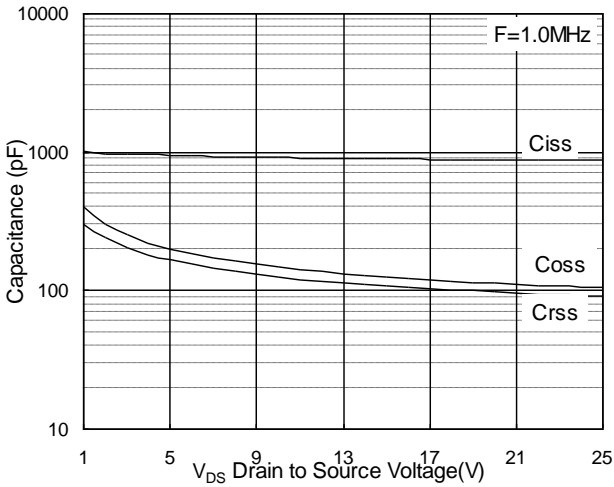


Fig.7 Capacitance

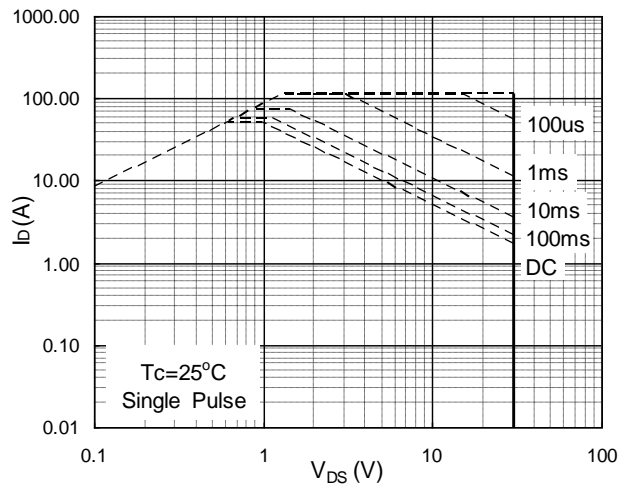


Fig.8 Safe Operating Area

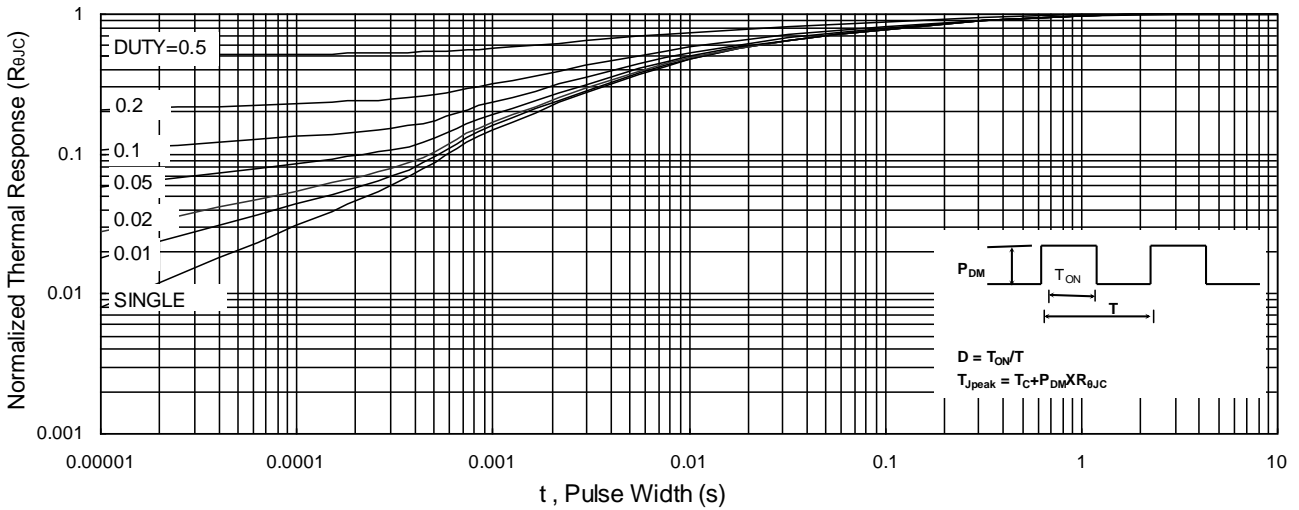


Fig.9 Normalized Maximum Transient Thermal Impedance

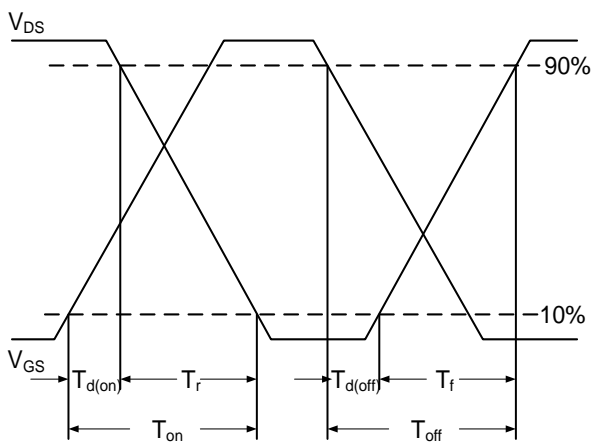


Fig.10 Switching Time Waveform

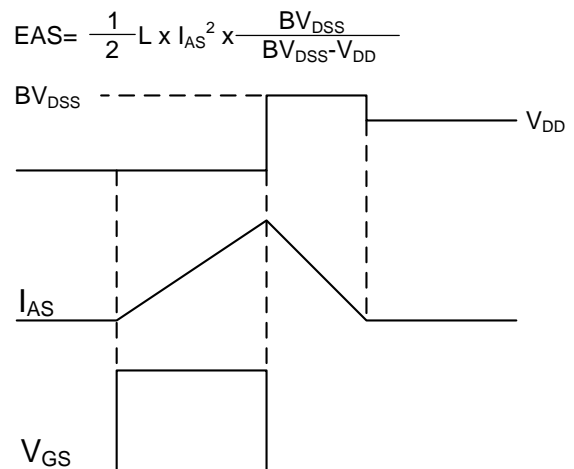
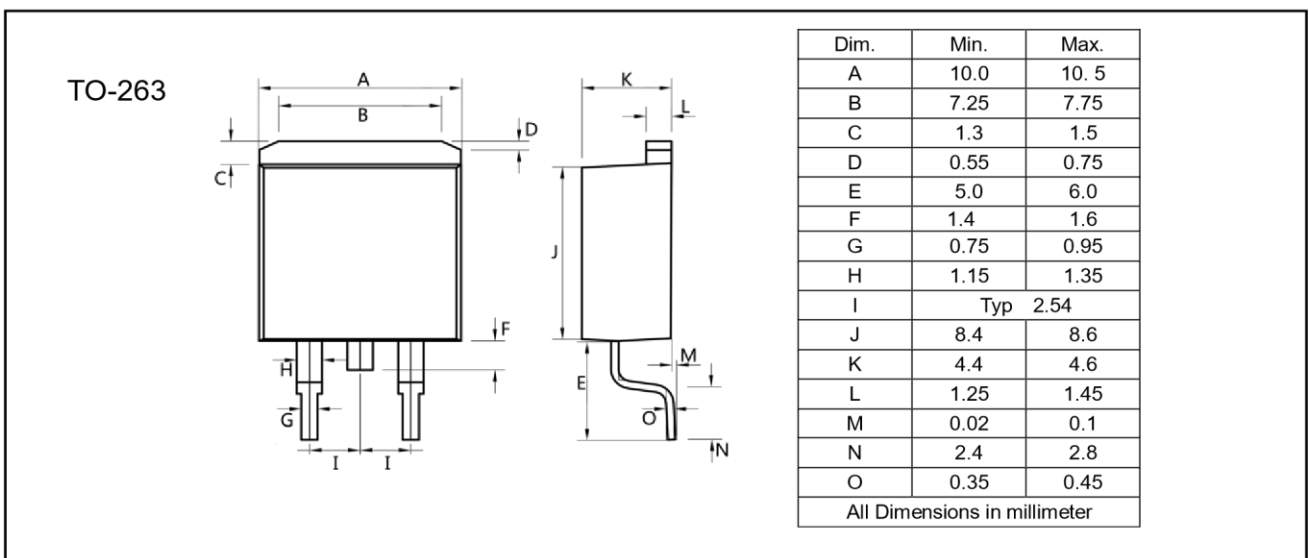
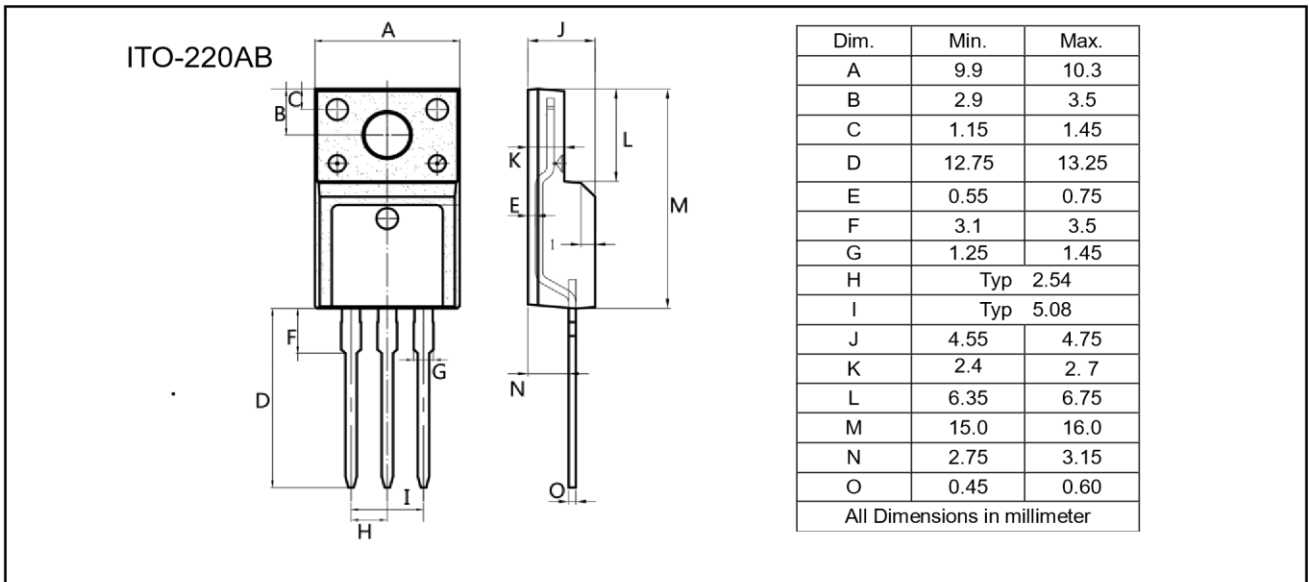
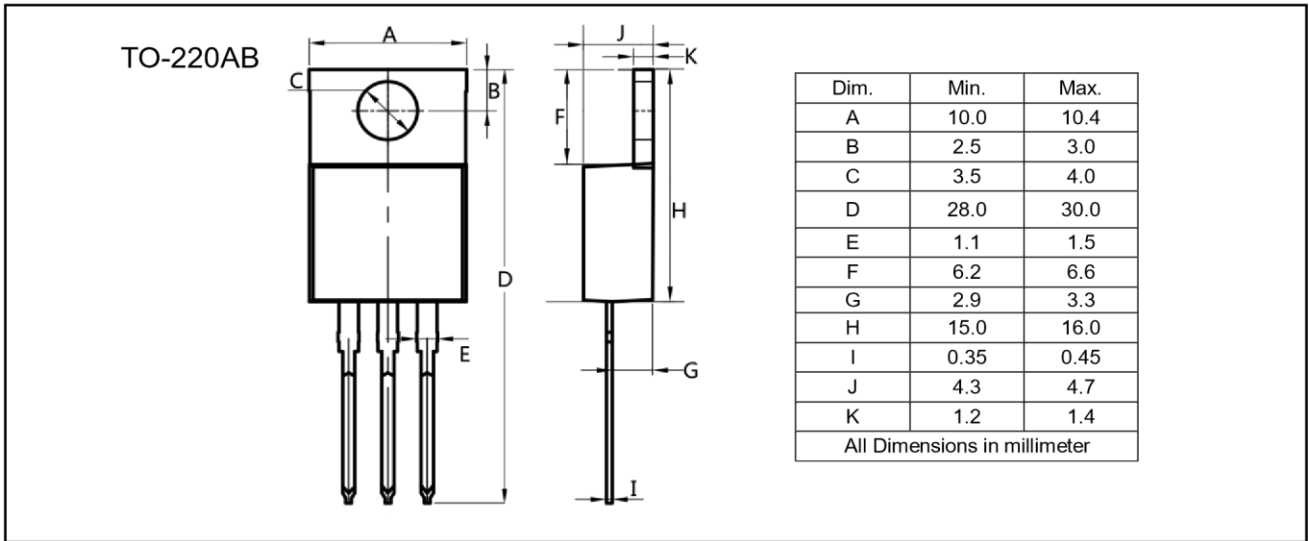


Fig.11 Unclamped Inductive Switching Waveform



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