

#### **Description**

The AP5N04MI uses advanced trench technology

to provide excellent R<sub>DS(ON)</sub>, low gate charge and

operation with gate voltages as low as 4.5V. This

device is suitable for use as a

Battery protection or in other Switching application.

#### **General Features**

 $V_{DS} = 40V I_{D} = 5.0A$ 

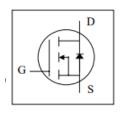
 $R_{DS(ON)} < 37m\Omega$  @  $V_{GS}=10V$ 

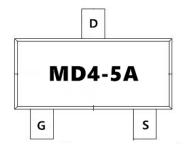
#### **Application**

**Battery protection** 

Load switch

Uninterruptible power supply







Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP5N04MI	SOT-23-3L	MD4-5A	3000

## Absolute Maximum Ratings (TA=25°C unless otherwise noted)

Symbol	Parameter	Rating	Units	
VDS	Drain-Source Voltage	40		
Vgs	Gate-Source Voltage	±20	V	
I <sub>D</sub> @T <sub>A</sub> =25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V <sup>1</sup>	5.0	А	
I <sub>D</sub> @T <sub>A</sub> =70°C	Continuous Drain Current, V <sub>GS</sub> @ 10V <sup>1</sup> 3.5		А	
Ірм	Pulsed Drain Current <sup>2</sup>	14	А	
P <sub>D</sub> @T <sub>A</sub> =25°C	Total Power Dissipation <sup>3</sup>	1	W	
Тѕтс	Storage Temperature Range	Storage Temperature Range -55 to 150		
TJ	Operating Junction Temperature Range	ion Temperature Range -55 to 150		
R <sub>0</sub> JA	Thermal Resistance Junction-ambient <sup>1</sup>	125	°C/W	
Rejc	Thermal Resistance Junction-Case <sup>1</sup>	80	°C/W	



## Electrical Characteristics (TA=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V , I <sub>D</sub> =250uA	40			V
∆BVpss/∆TJ	BVDSS Temperature Coefficient	Reference to 25°C , I <sub>D</sub> =1mA		0.032		V/°C
		V <sub>GS</sub> =10V , I <sub>D</sub> =4A		30	37	
RDS(ON)	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =4.5V , I <sub>D</sub> =3A		40	50	$\mathbf{m}\Omega$
VGS(th)	Gate Threshold Voltage		1.0	1.5	2.5	V
$\triangle V_{GS(th)}$	V <sub>GS(th)</sub> Temperature Coefficient	$V_{GS}=V_{DS}$ , $I_D=250uA$		-4.5		mV/°C
,	Drain-Source Leakage Current	V <sub>DS</sub> =32V , V <sub>GS</sub> =0V , T <sub>J</sub> =25°C			1	^
loss		V <sub>DS</sub> =32V , V <sub>GS</sub> =0V , T <sub>J</sub> =55°C			5	uA
Igss	Gate-Source Leakage Current	V <sub>GS</sub> =±20V , V <sub>DS</sub> =0V			±100	nA
gfs	Forward Transconductance	V <sub>DS</sub> =5V , I <sub>D</sub> =4A		8		S
Rg	Gate Resistance	V <sub>DS</sub> =0V , V <sub>GS</sub> =0V , f=1MHz		2.4	4.8	Ω
Qg	Total Gate Charge (4.5V)			5		
Qgs	Gate-Source Charge	V <sub>DS</sub> =15V , V <sub>GS</sub> =4.5V , I <sub>D</sub> =3A		1.54		nC
Qgd	Gate-Drain Charge			1.84		
Td(on)	Turn-On Delay Time			7.8		
Tr	Rise Time	V <sub>DD</sub> =15V , V <sub>GS</sub> =10V ,		2.1		
Td(off)	Turn-Off Delay Time	—R <sub>G</sub> =3.3 I <sub>D</sub> =1A		29		ns
T <sub>f</sub>	Fall Time			2.1		
Ciss	Input Capacitance			452		
Coss	Output Capacitance			51		pF
Crss	Reverse Transfer Capacitance			38		
ls	Continuous Source Current <sup>1,4</sup>	V <sub>G</sub> =V <sub>D</sub> =0V , Force Current			4.5	Α
Іѕм	Pulsed Source Current <sup>2,4</sup>				14	Α
VsD	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V , I <sub>S</sub> =1A , T <sub>J</sub> =25°C			1.2	V

#### Note:

<sup>1 .</sup>The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.

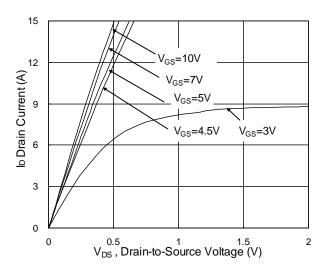
<sup>2.</sup>The data tested by pulsed , pulse width  $\leqq 300 us$  , duty cycle  $\leqq 2\%$ 

<sup>3 .</sup>The power dissipation is limited by 150  $^{\circ}\text{C}$  junction temperature

<sup>4.</sup>The data is theoretically the same as  $I_D$  and  $I_{DM}$ , in real applications, should be limited by total power dissipation.



#### **Typical Characteristics**



**Fig.1 Typical Output Characteristics** 

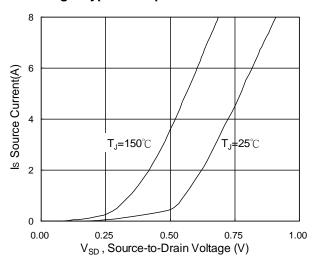


Fig.3 Forward Characteristics Of Reverse

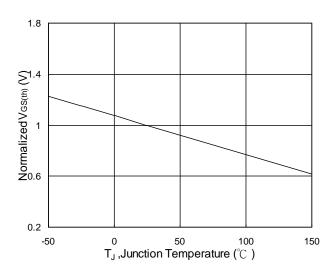


Fig.5 Normalized V<sub>GS(th)</sub> vs. T<sub>J</sub>

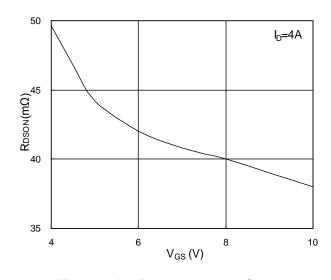
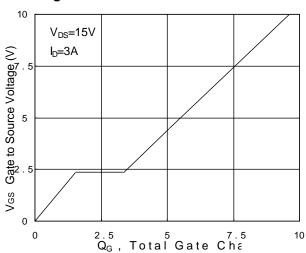


Fig.2 On-Resistance vs. Gate-Source



**Fig.4 Gate-Charge Characteristics** 

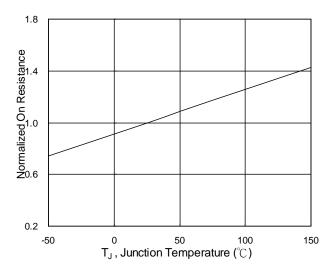
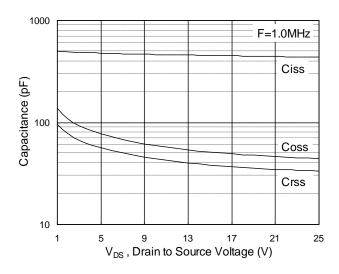


Fig.6 Normalized R<sub>DSON</sub> vs. T<sub>J</sub>







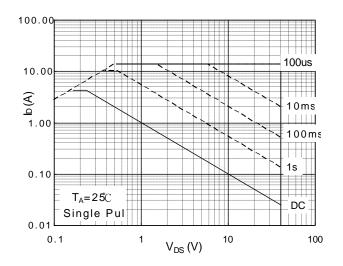


Fig.7 Capacitance

Fig.8 Safe Operating Area

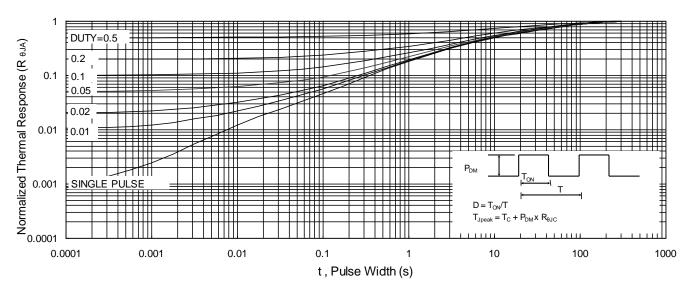


Fig.9 Normalized Maximum Transient Thermal Impedance

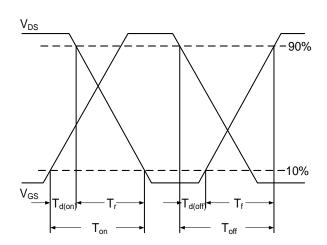


Fig.10 Switching Time Waveform

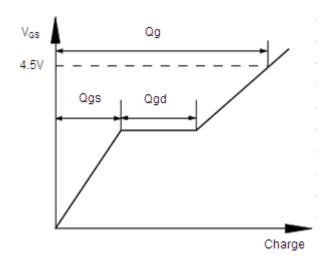
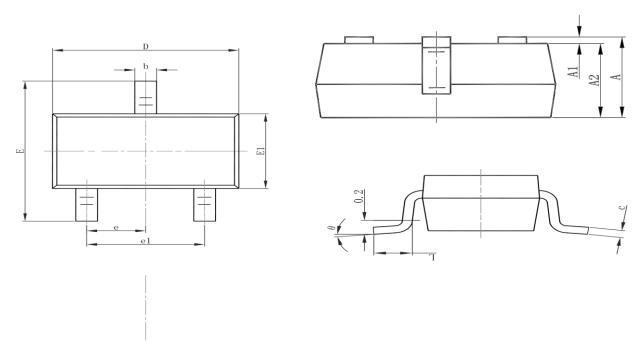


Fig.11 Gate Charge Waveform





# Package Mechanical Data:SOT23-3L



Symbol	Dimensions In Millimeters		Dimensions In Inches		
	Min.	Max.	Min.	Max.	
Α	1.050	1.250	0.041	0.049	
A1	0.000	0.100	0.000	0.004	
A2	1.050	1.150	0.041	0.045	
b	0.300	0.500	0.012	0.020	
С	0.100	0.200	0.004	0.008	
D	2.820	3.020	0.111	0.119	
E1	1.500	1.700	0.059	0.067	
E	2.650	2.950	0.104	0.116	
е	0.950(BSC)		0.037(BSC)		
e1	1.800	2.000	0.071	0.079	
L	0.300	0.600	0.012	0.024	
θ	0°	8°	0°	8°	



# 40V N-Channel Enhancement Mode MOSFET Attention

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