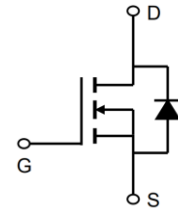


60V N-Channel Enhancement Mode MOSFET

Description

The AP50N06D uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.



General Features

$V_{DS} = 60V$ $I_D = 50A$

$R_{DS(ON)} < 16m\Omega$ @ $V_{GS}=10V$

Application

Battery protection

Load switch

Uninterruptible power supply

Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP50N06D	TO-252-3L	AP50N06D XXXX YYY	2500

Absolute Maximum Ratings ($T_C=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	60	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_C=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	50	A
$I_D@T_C=100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	25	A
$I_D@T_A=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	7.4	A
$I_D@T_A=70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	6	A
IDM	Pulsed Drain Current ²	90	A
EAS	Single Pulse Avalanche Energy ³	39.2	mJ
IAS	Avalanche Current	28	A
$P_D@T_C=25^\circ C$	Total Power Dissipation ⁴	45	W
$P_D@T_A=25^\circ C$	Total Power Dissipation ⁴	2	W
TSTG	Storage Temperature Range	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ C$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	62	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	2.8	$^\circ C/W$

Electrical Characteristics (T_J=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	60	65	---	V
ΔBVDSS/ΔT _J	BVDSS Temperature Coefficient	Reference to 25°C, I _D =1mA	---	0.057	---	V/°C
RDS(ON)	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =20A	---	11.5	16	mΩ
		V _{GS} =4.5V, I _D =10A	---	16.3	20	
VGS(th)	Gate Threshold Voltage		1.2	1.8	2.5	V
ΔVGS(th)	VGS(th) Temperature Coefficient	V _{GS} =V _{DS} , I _D =250uA	---	-5.68	---	mV/°C
IDSS	Drain-Source Leakage Current	V _{DS} =48V, V _{GS} =0V, T _J =25°C	---	---	1	uA
		V _{DS} =48V, V _{GS} =0V, T _J =55°C	---	---	5	
IGSS	Gate-Source Leakage Current	V _{GS} =±20V, V _{DS} =0V	---	---	±100	nA
gfs	Forward Transconductance	V _{DS} =5V, I _D =15A	---	45	---	S
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz	---	1.7	---	Ω
Q _g	Total Gate Charge (4.5V)		---	19.3	---	nC
Q _{gs}	Gate-Source Charge	V _{DS} =48V, V _{GS} =4.5V, I _D =15A	---	7.1	---	
Q _{gd}	Gate-Drain Charge		---	7.6	---	
Td(on)	Turn-On Delay Time		---	7.2	---	ns
T _r	Rise Time	V _{DD} =30V, V _{GS} =10V, R _G =3.3Ω, I _D =15A	---	50	---	
Td(off)	Turn-Off Delay Time		---	36.4	---	
T _f	Fall Time		---	7.6	---	
C _{iss}	Input Capacitance		---	2423	---	pF
C _{oss}	Output Capacitance	V _{DS} =15V, V _{GS} =0V, f=1MHz	---	145	---	
C _{rss}	Reverse Transfer Capacitance		---	97	---	
I _s	Continuous Source Current ^{1,5}		---	---	35	A
ISM	Pulsed Source Current ^{2,5}	V _{GS} =V _D =0V, Force Current	---	---	80	A
VSD	Diode Forward Voltage ²	V _{GS} =0V, I _S =A, T _J =25°C	---	---	1	V
t _{rr}	Reverse Recovery Time	I _F =15A, dI/dt=100A/μs, T _J =25°C	---	16.3	---	nS
Q _{rr}	Reverse Recovery Charge		---	11	---	nC

Note :

1. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
2. The data tested by pulsed, pulse width ≅ 300us, duty cycle ≅ 2%
3. The EAS data shows Max. rating. The test condition is VDD=25V, VGS=10V, L=0.1mH, IAS=28A
4. The power dissipation is limited by 150°C junction temperature
5. The data is theoretically the same as ID and IDM, in real applications, should be limited by total power dissipation

Typical Characteristics

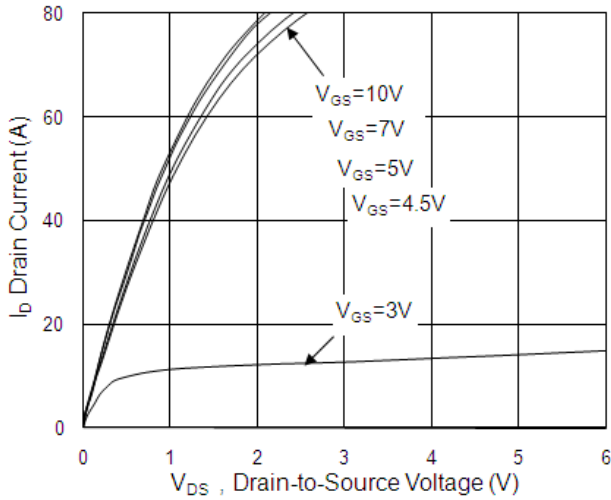


Fig.1 Typical Output Characteristics

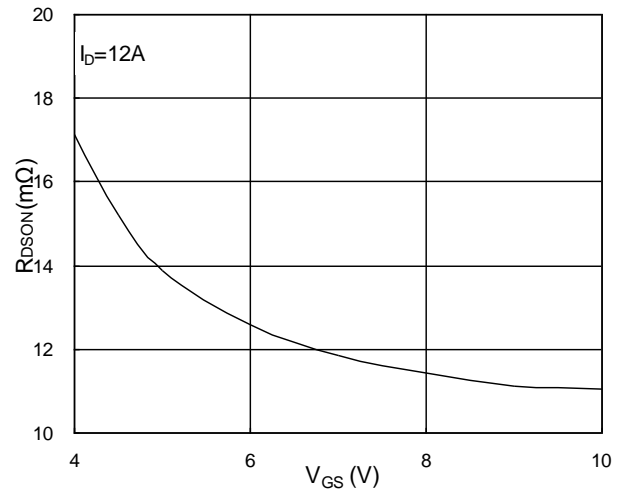


Fig.2 On-Resistance v.s Gate-Source

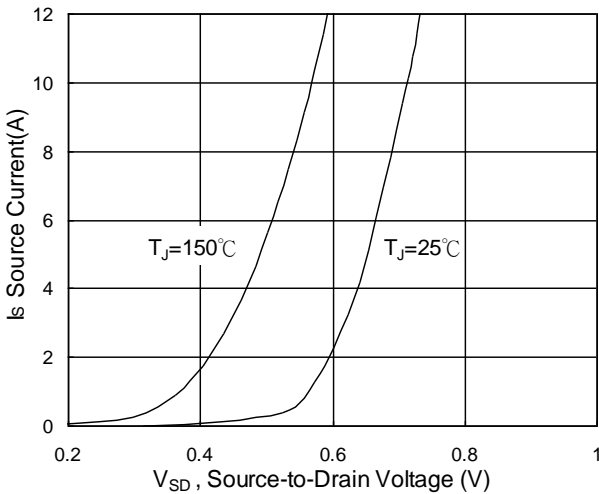


Fig.3 Forward Characteristics of Reverse

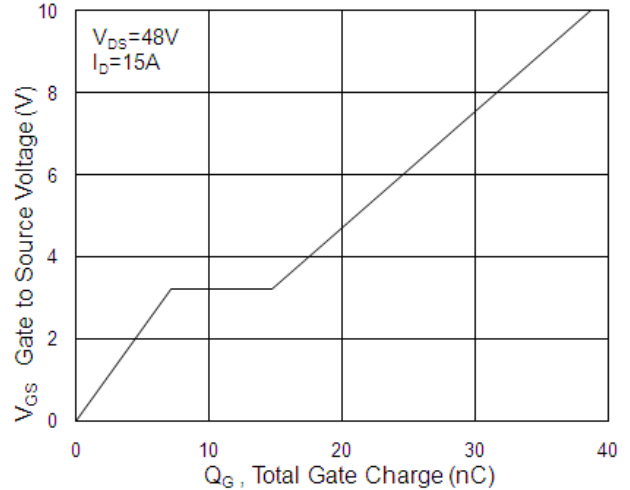


Fig.4 Gate-Charge Characteristics

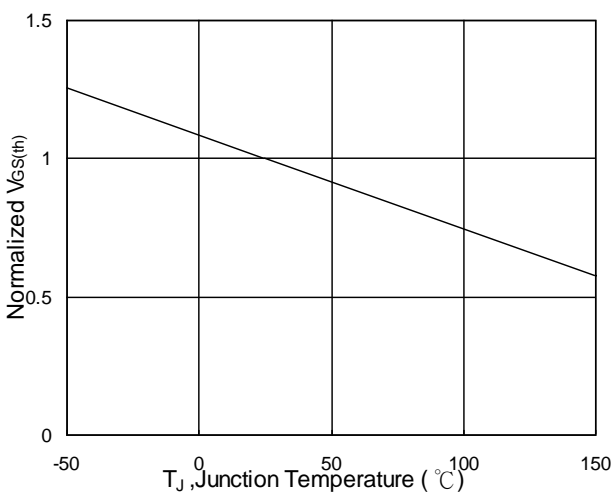


Fig.5 Normalized V_{GS} v.s T_J

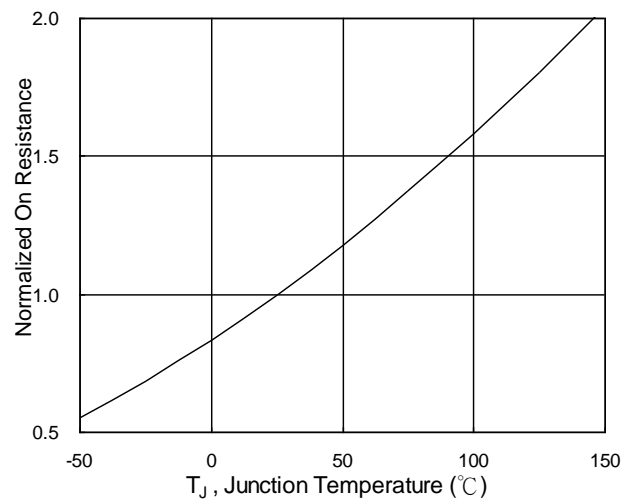


Fig.6 Normalized $R_{DS(on)}$ v.s T_J



60V N-Channel Enhancement Mode MOSFET

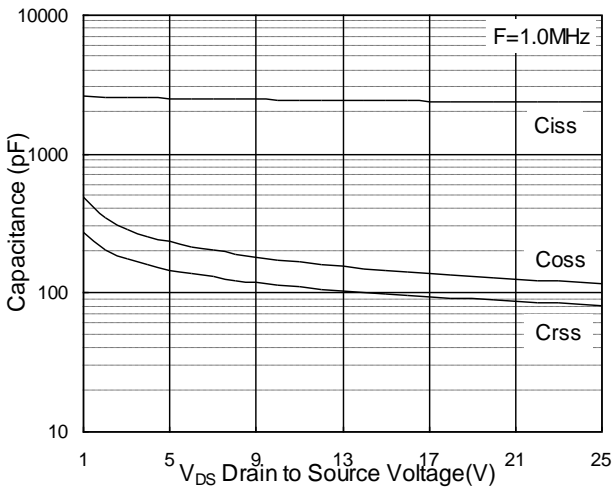


Fig.7 Capacitance

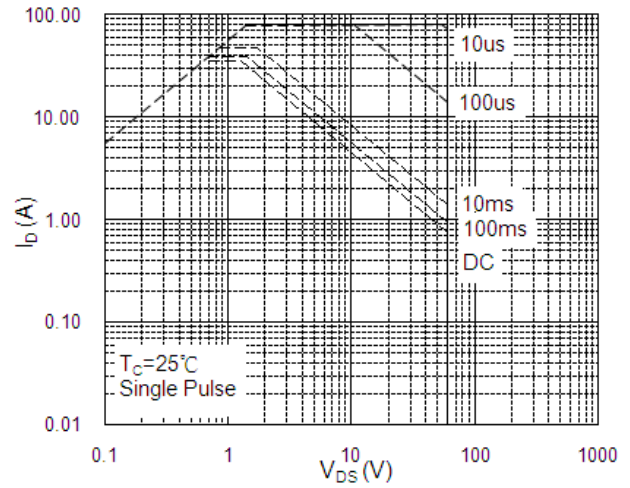


Fig.8 Safe Operating Area

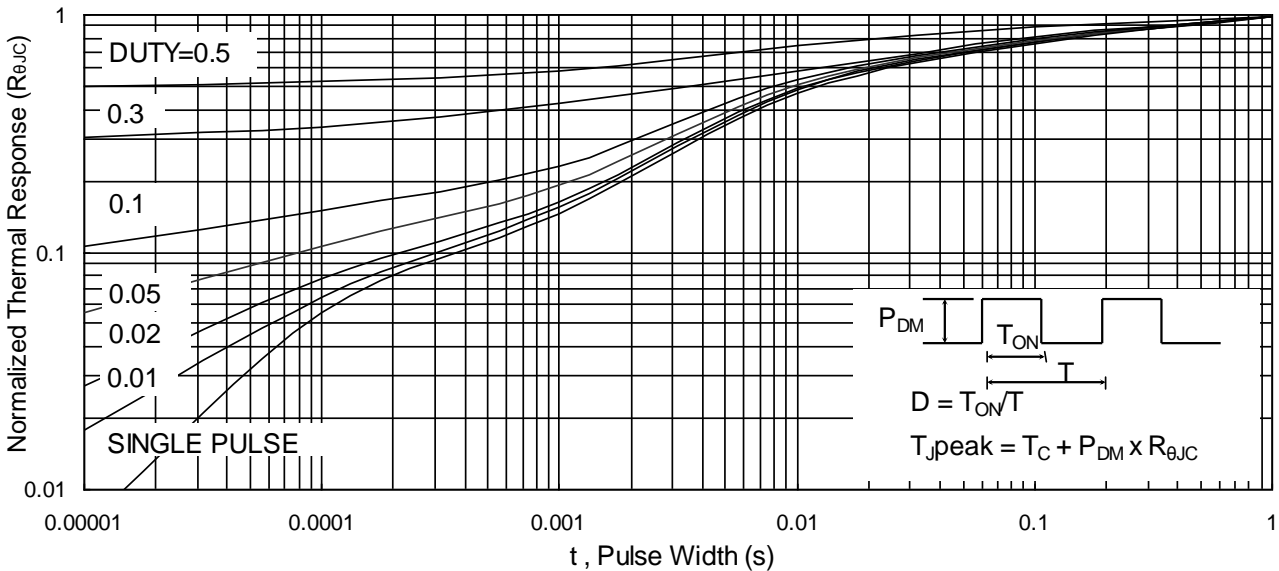


Fig.9 Normalized Maximum Transient Thermal Impedance

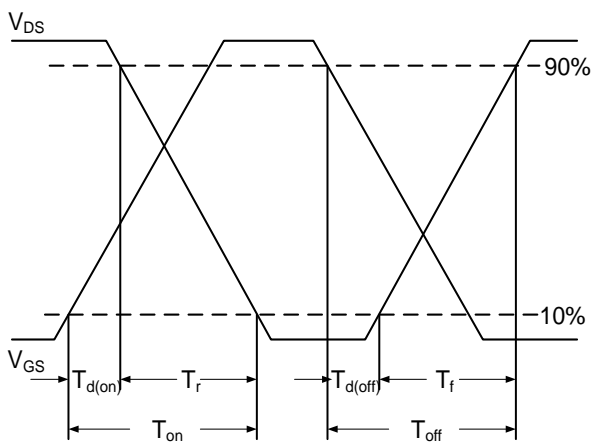


Fig.10 Switching Time Waveform

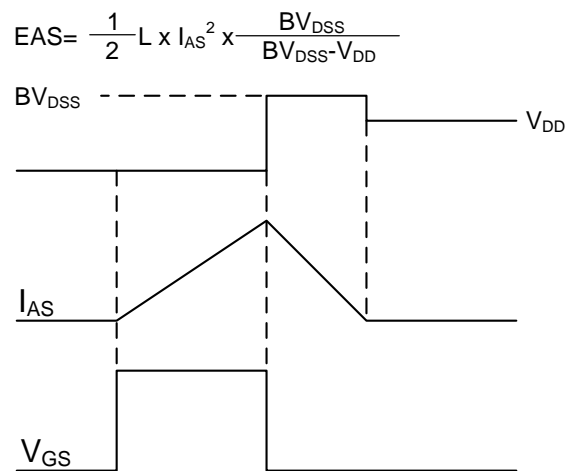
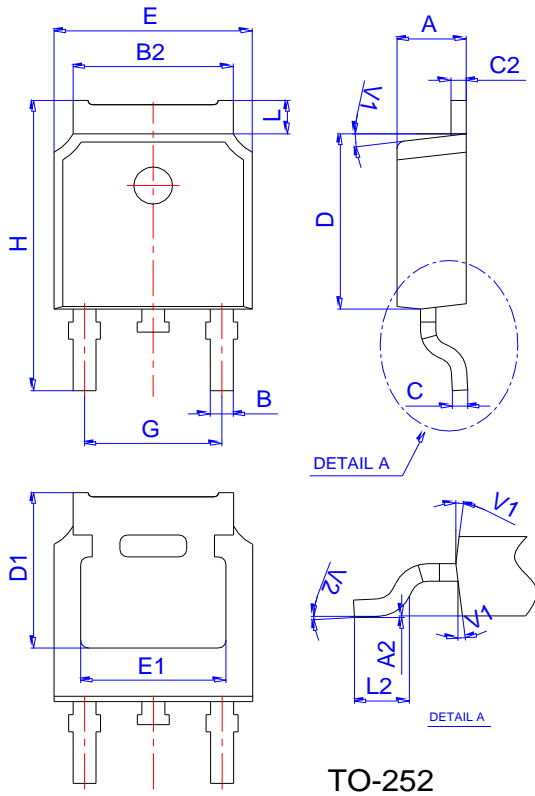


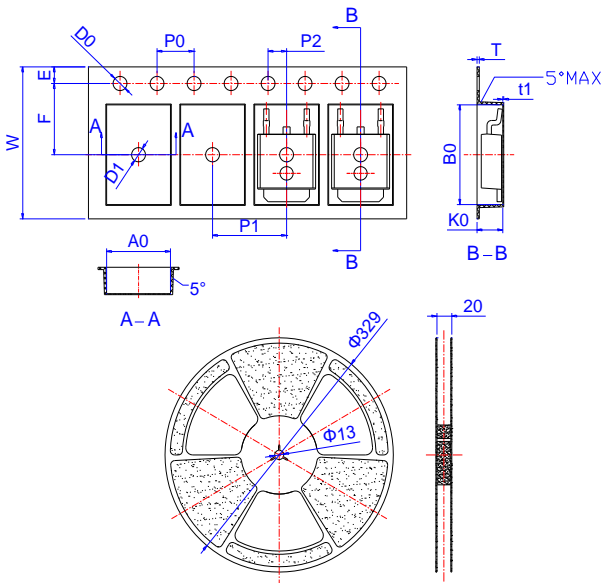
Fig.11 Unclamped Inductive Switching Waveform

Package Mechanical Data: TO-252-3L



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2		0°	6°	0°	7°	6°

Reel Specification-TO-252



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
W	15.90	16.00	16.10	0.626	0.630	0.634
E	1.65	1.75	1.85	0.065	0.069	0.073
F	7.40	7.50	7.60	0.291	0.295	0.299
D0	1.40	1.50	1.60	0.055	0.059	0.063
D1	1.40	1.50	1.60	0.055	0.059	0.063
P0	3.90	4.00	4.10	0.154	0.157	0.161
P1	7.90	8.00	8.10	0.311	0.315	0.319
P2	1.90	2.00	2.10	0.075	0.079	0.083
A0	6.85	6.90	7.00	0.270	0.271	0.276
B0	10.45	10.50	10.60	0.411	0.413	0.417
K0	2.68	2.78	2.88	0.105	0.109	0.113
T	0.24		0.27	0.009		0.011
t1	0.10			0.004		
10P0	39.80	40.00	40.20	1.567	1.575	1.583

60V N-Channel Enhancement Mode MOSFET

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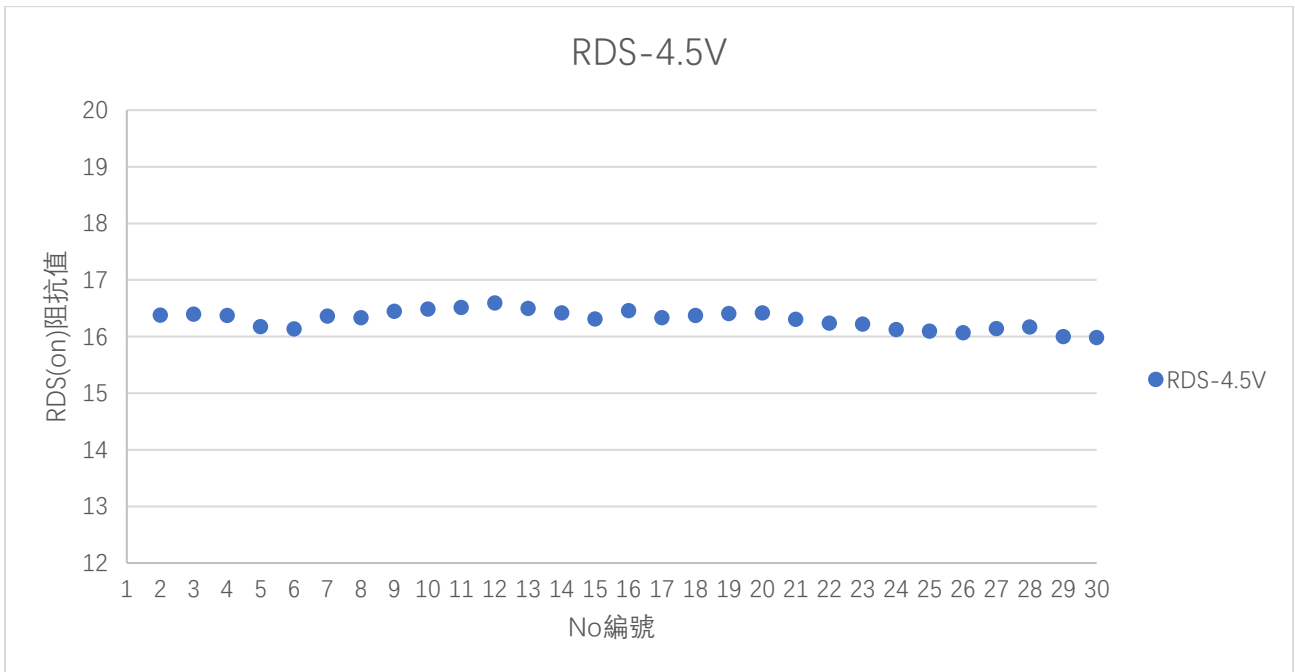
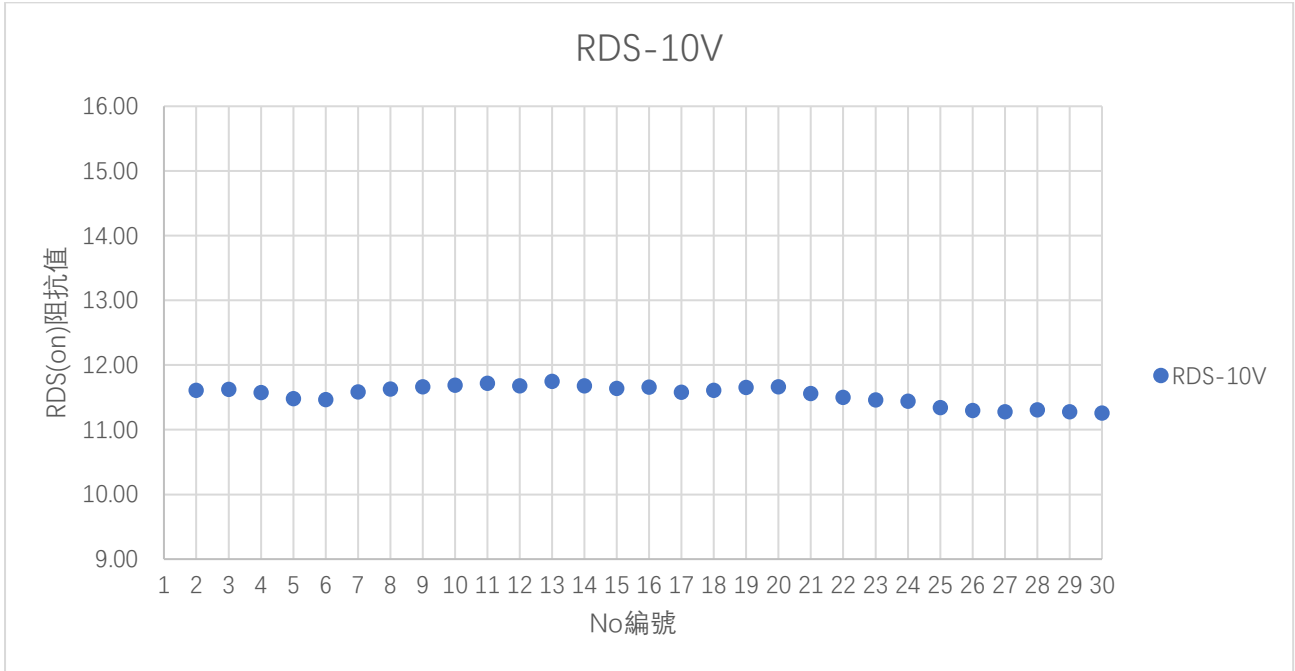
Edition	Date	Change
Rve3.8	2018/1/31	Initial release
Rve3.9	2019/12/01	Reduce RDS(on)

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Test Report For 30PCS (30pcs 典型測試報告)





60V N-Channel Enhancement Mode MOSFET

