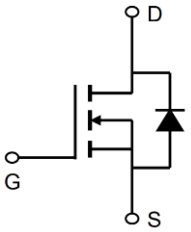
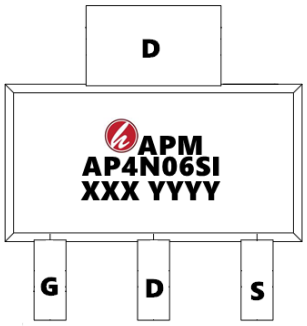
# AP4N06SI

## 60V N-Channel Enhancement Mode MOSFET

### Description

The AP4N06SI uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.




### General Features

$V_{DS}$=60V $I_D$ =4.8A

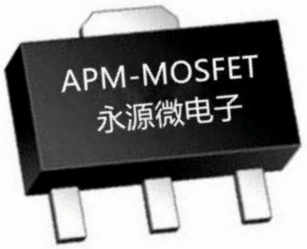
$R_{DS(ON)}$ < 95mΩ @ $V_{GS}$=10V (Type: 72mΩ)

### Application

Battery protection

Load switch

Uninterruptible power supply




### Package Marking and Ordering Information

| Product ID | Pack | Marking | Qty(PCS) |
|---|---|---|---|
| AP4N06SI | SOT-89-3L | AP4N06SI XXXX YYYY | 3000 |

### Absolute Maximum Ratings ($T_C$=25℃unless otherwise noted)

| Symbol | Parameter | Rating | Units |
|---|---|---|---|
| $V_{DS}$ | Drain-Source Voltage | 60 | V |
| $V_{GS}$ | Gate-Source Voltage | ±20 | V |
| $I_D$@$T_C$=25℃ | Continuous Drain Current, $V_{GS}$ @ 10V[1] | 4.8 | A |
| $I_D$@$T_C$=100℃ | Continuous Drain Current, $V_{GS}$ @ 10V[1] | 2.0 | A |
| $I_{DM}$ | Pulsed Drain Current[2] | 15 | A |
| EAS | Single Pulse Avalanche Energy[3] | 6.2 | mJ |
| $P_D$@$T_C$=25℃ | Total Power Dissipation[4] | 1.5 | W |
| $T_{STG}$ | Storage Temperature Range | -55 to 150 | ℃ |
| $T_J$ | Operating Junction Temperature Range | -55 to 150 | ℃ |
| $R_{\theta JA}$ | Thermal Resistance Junction-ambient [1] | 85 | ℃/W |
| $R_{\theta JC}$ | Thermal Resistance Junction-Case[1] | 48 | ℃/W |

## Electrical Characteristics ($T_J$=25 ℃, unless otherwise noted)

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| BVDSS | Drain-Source Breakdown Voltage | $V_{GS}$=0V , $I_D$=250uA | 60 | 65 | --- | V |
| △BVDSS/△TJ | $BV_{DSS}$ Temperature Coefficient | Reference to 25℃ , $I_D$=1mA | --- | 0.054 | --- | V/℃ |
| RDS(ON) | Static Drain-Source On-Resistance[2] | $V_{GS}$=10V , $I_D$=2A | --- | 72 | 95 | mΩ |
| | | $V_{GS}$=4.5V , $I_D$=1A | --- | 85 | 100 | |
| VGS(th) | Gate Threshold Voltage | $V_{GS}$=$V_{DS}$ , $I_D$ =250uA | 1.2 | 1.5 | 2.5 | V |
| △$V_{GS(th)}$ | $V_{GS(th)}$ Temperature Coefficient | | --- | -4.96 | --- | mV/℃ |
| IDSS | Drain-Source Leakage Current | $V_{DS}$=48V , $V_{GS}$=0V , $T_J$=25℃ | --- | --- | 1 | uA |
| | | $V_{DS}$=48V , $V_{GS}$=0V , $T_J$=55℃ | --- | --- | 5 | |
| IGSS | Gate-Source Leakage Current | $V_{GS}$=±20V , $V_{DS}$=0V | --- | --- | ±100 | nA |
| gfs | Forward Transconductance | $V_{DS}$=5V , $I_D$=2A | --- | 13 | --- | S |
| $Q_g$ | Total Gate Charge (4.5V) | $V_{DS}$=48V , $V_{GS}$=4.5V , $I_D$=2A | --- | 5 | 7.0 | nC |
| Qgs | Gate-Source Charge | | --- | 1.68 | 2.4 | |
| Qgd | Gate-Drain Charge | | --- | 1.9 | 2.7 | |
| Td(on) | Turn-On Delay Time | $V_{DD}$=30V , $V_{GS}$=10V , $R_G$=3.3Ω, $I_D$=2A | --- | 1.6 | 3.2 | ns |
| $T_r$ | Rise Time | | --- | 7.2 | 13 | |
| Td(off) | Turn-Off Delay Time | | --- | 25 | 50 | |
| $T_f$ | Fall Time | | --- | 14.4 | 28.8 | |
| Ciss | Input Capacitance | $V_{DS}$=15V , $V_{GS}$=0V , f=1MHz | --- | 511 | 715 | pF |
| Coss | Output Capacitance | | --- | 38 | 53 | |
| Crss | Reverse Transfer Capacitance | | --- | 25 | 35 | |
| IS | Continuous Source Current[1,4] | $V_G$=$V_D$=0V , Force Current | --- | --- | 2.3 | A |
| ISM | Pulsed Source Current[2,4] | | --- | --- | 9.2 | A |
| VSD | Diode Forward Voltage[2] | $V_{GS}$=0V , $I_S$=1A , $T_J$=25℃ | --- | --- | 1.2 | V |
| trr | Reverse Recovery Time | IF=2A , dI/dt=100A/μs , $T_J$=25℃ | --- | 9.7 | --- | nS |
| $Q_{rr}$ | Reverse Recovery Charge | | --- | 5.8 | --- | nC |

**Note :**

1、The data tested by surface mounted on a 1 inch 2 FR-4 board with 2OZ copper.

2、The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%

3、The EAS data shows Max. rating . The test condition is V DD =25V,V GS =10V,L=0.1mH,IAS =2A

4、The power dissipation is limited by 150℃ junction temperature

5、The data is theoretically the same as I D and I DM , in real applications , should be limited by total power dissipation.

## Typical Characteristics

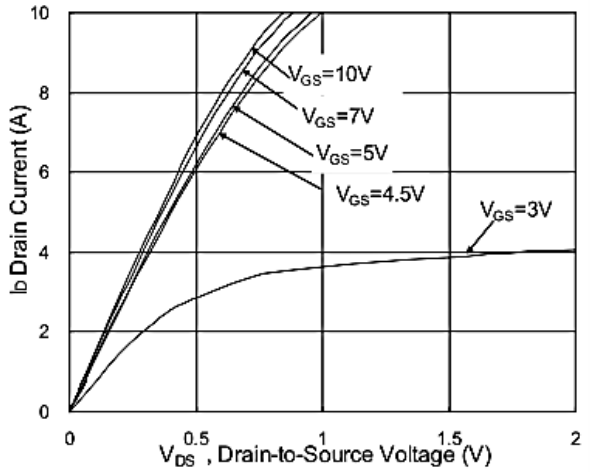



Fig.1 Typical Output Characteristics

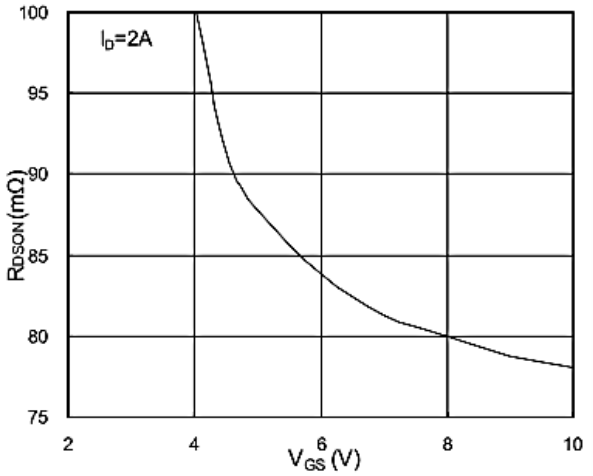



Fig.2 On-Resistance v.s Gate-Source

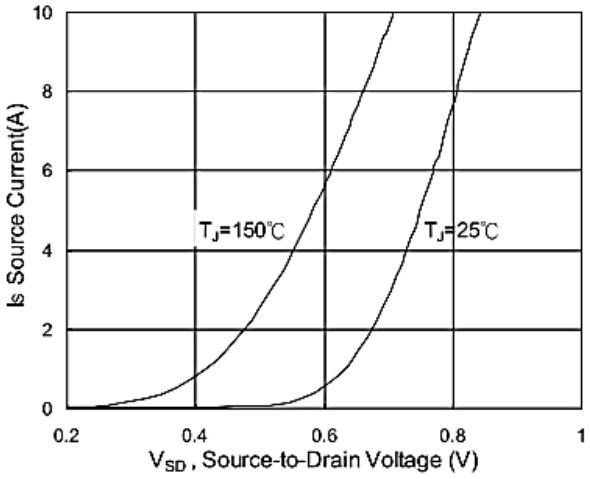



Fig.3 Forward Characteristics of Reverse

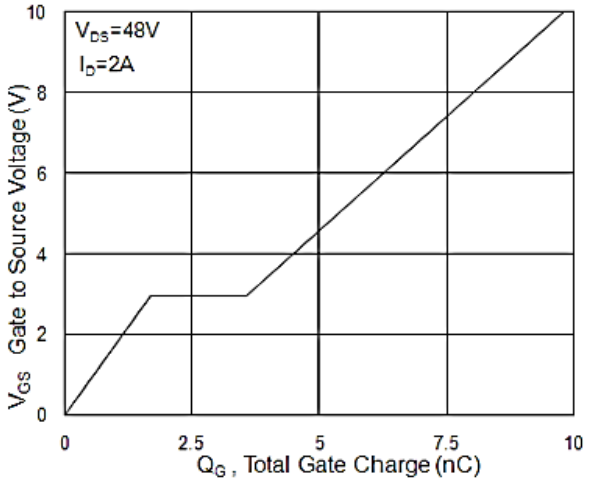



Fig.4 Gate-Charge Characteristics

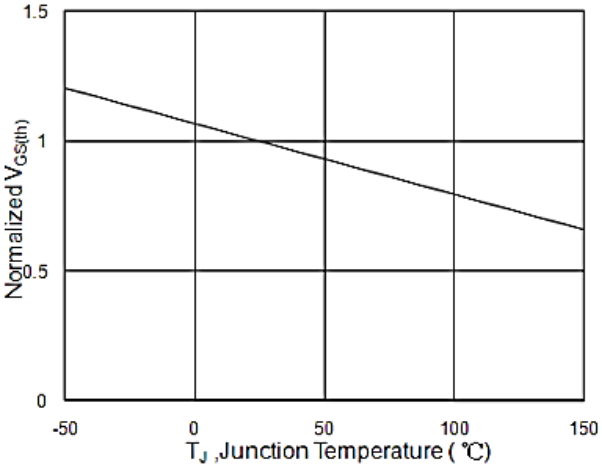



Fig.5 Normalized $V_{GS(th)}$ v.s $T_J$

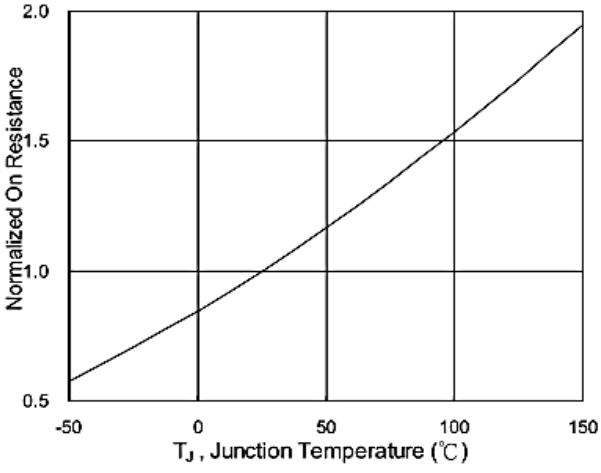



Fig.6 Normalized $R_{DSON}$ v.s $T_J$

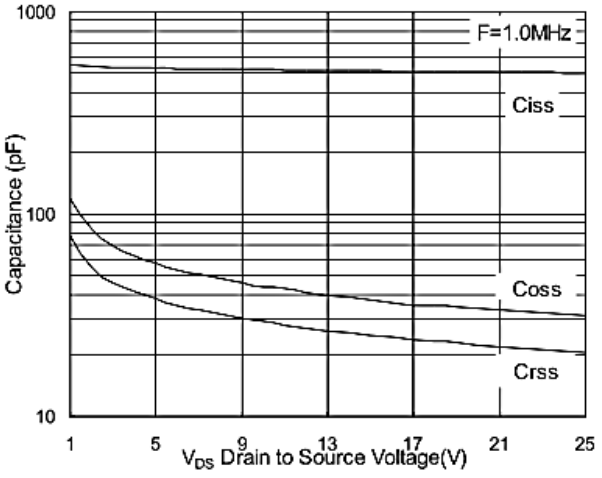



Fig.7 Capacitance

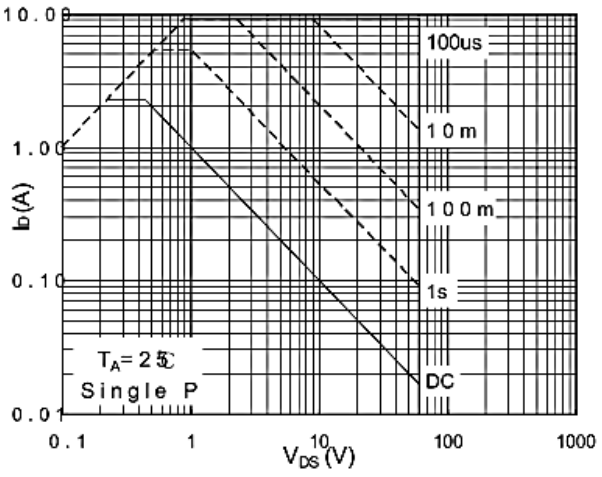



Fig.8 Safe Operating Area

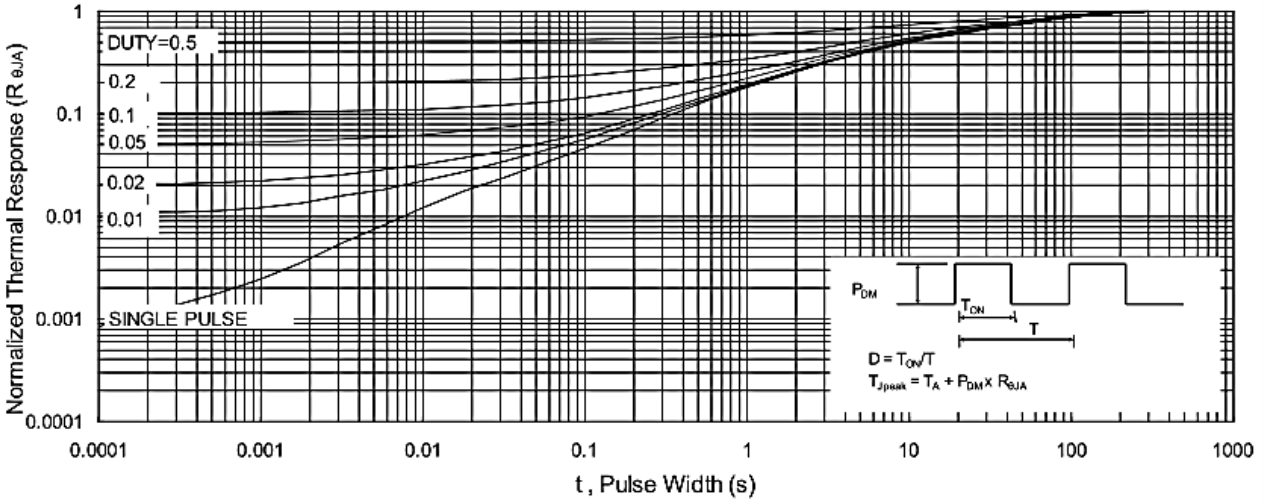



Fig.9 Normalized Maximum Transient Thermal Impedance

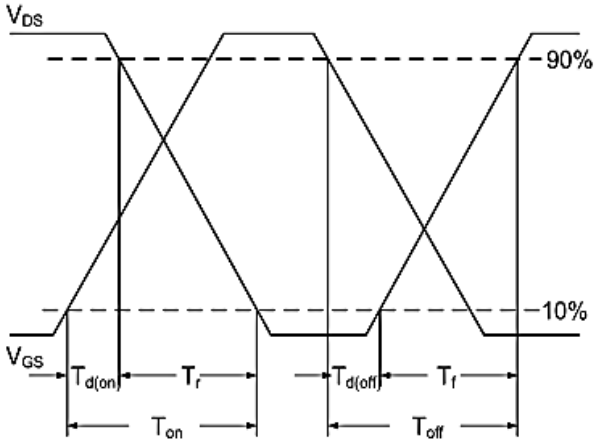



Fig.10 Switching Time Waveform

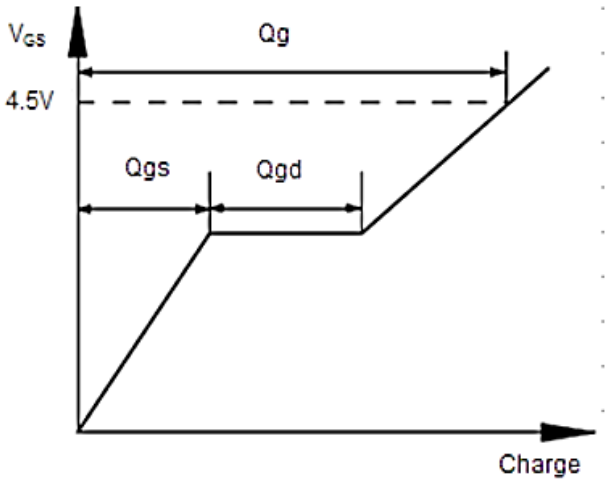
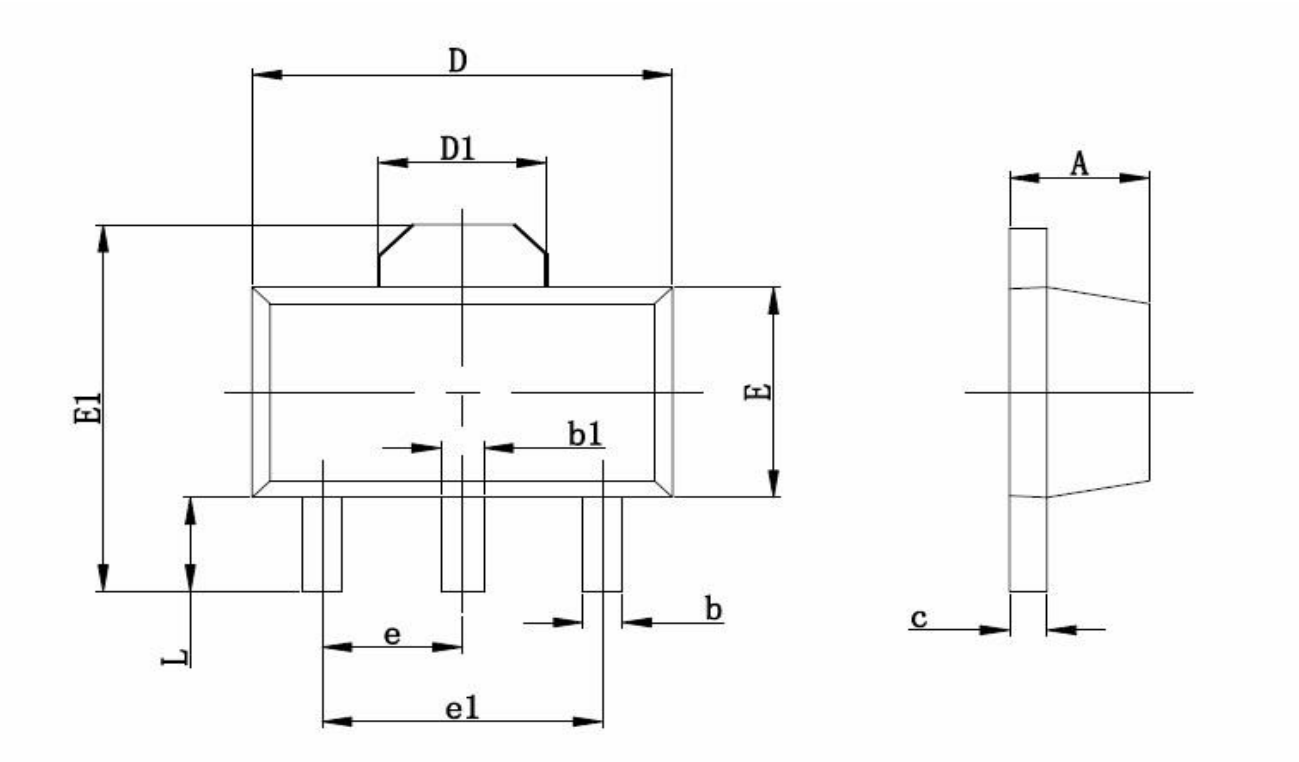



Fig.11 Gate Charge Waveform

## Package Mechanical Data:SOT89-3L




| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 1.400 | 1.600 | 0.055 | 0.063 |
| b | 0.350 | 0.520 | 0.013 | 0.197 |
| b1 | 0.400 | 0.580 | 0.016 | 0.023 |
| c | 0.350 | 0.440 | 0.014 | 0.017 |
| D | 4.400 | 4.600 | 0.173 | 0.181 |
| D1 | 1.550 REF | | 0.061 REF | |
| E | 2.350 | 2.550 | 0.091 | 0.102 |
| E1 | 3.940 | 4.250 | 0.155 | 0.167 |
| e | 1.500 TYP | | 0.060TYP | |
| e1 | 3.000 TYP | | 0.118TYP | |
| L | 0.900 | 1.100 | 0.035 | 0.047 |

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## 60V N-Channel Enhancement Mode MOSFET

| Edition | Date | Change |
|---|---|---|
| Rve1.0 | 2020/5/1 | Initial release |