

#### **Description**

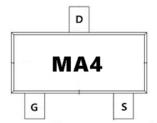
The AP3N10BI uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

# G S

#### **General Features**

 $V_{DS} = 100V I_{D} = 2.8 A$ 

 $R_{DS(ON)}$  < 320m $\Omega$  @  $V_{GS}$ =10V



#### **Application**

Battery protection

Load switch

Uninterruptible power supply



**Package Marking and Ordering Information** 

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Product ID	Pack	Marking	Qty(PCS)		
AP3N10BI	SOT-23	MA4	3000		

#### Absolute Maximum Ratings (TC=25°C unless otherwise specified)

Symbol Parameter		Rating	Units	
V <sub>DS</sub>	Drain-Source Voltage	100	V	
Vgs	Gate-Source Voltage	±20	V	
I <sub>D</sub> @T <sub>A</sub> =25°C	T <sub>A</sub> =25°C Continuous Drain Current, V <sub>GS</sub> @ 10V <sup>1</sup>		А	
I <sub>D</sub> @T <sub>A</sub> =70°C Continuous Drain Current, V <sub>GS</sub> @ 10		1	А	
Ірм	Pulsed Drain Current <sup>2</sup>	5	А	
P <sub>D</sub> @T <sub>A</sub> =25°C	Total Power Dissipation <sup>3</sup>	1	W	
Tstg Storage Temperature Range		-55 to 150	°C	
T <sub>J</sub> Operating Junction Temperature Range		-55 to 150	°C	
Reja	R <sub>θJA</sub> Thermal Resistance Junction-ambient <sup>1</sup>		°C/W	
R <sub>B</sub> JC Thermal Resistance Junction-Case <sup>1</sup>		80	°C/W	



#### Electrical Characteristics (T<sub>J</sub>=25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V , I <sub>D</sub> =250uA	100			V
∆BVpss/∆Tj	BVDSS Temperature Coefficient	Reference to 25°C , I <sub>D</sub> =1mA		0.067		V/°C
		V <sub>GS</sub> =10V , I <sub>D</sub> =1A		260	310	
Rds(on)	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =4.5V , I <sub>D</sub> =0.5A		270	320	mΩ
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =250uA	1.0	1.5	2.5	V
$\triangle V_{GS(th)}$	V <sub>GS(th)</sub> Temperature Coefficient			-4.2		mV/°C
IDSS	Drain-Source Leakage Current	V <sub>DS</sub> =80V , V <sub>GS</sub> =0V , T <sub>J</sub> =25°C			1	uA
IDSS Drain-Source Leakage Current		V <sub>DS</sub> =80V , V <sub>GS</sub> =0V , T <sub>J</sub> =25°C			5	uA
Igss	Gate-Source Leakage Current	V <sub>GS</sub> =±20V , V <sub>DS</sub> =0V			±100	nA
gfs	Forward Transconductance	V <sub>DS</sub> =5V , I <sub>D</sub> =1A		2.4		S
Rg	Gate Resistance	V <sub>DS</sub> =0V , V <sub>GS</sub> =0V , f=1MHz		2.8	5.6	
Qg	Total Gate Charge (10V)			9.7	13.6	
Qgs	Gate-Source Charge	V <sub>DS</sub> =80V , V <sub>GS</sub> =10V , I <sub>D</sub> =1A		1.6	2.2	nC
Qgd	Gate-Drain Charge			1.7	2.4	
Td(on)	Turn-On Delay Time			1.6	3.2	
Tr	Rise Time	V <sub>DD</sub> =50V , V <sub>GS</sub> =10V , —R <sub>G</sub> =3.3 —I <sub>D</sub> =1A		19	34	ns
T <sub>d(off)</sub>	Turn-Off Delay Time			13.6	27	
Tf	Fall Time			19	38	
Ciss	Input Capacitance			508	711	
Coss	Output Capacitance	V <sub>DS</sub> =15V , V <sub>GS</sub> =0V , f=1MHz		29	41	pF
Crss	Reverse Transfer Capacitance	nsfer Capacitance		16.4	23	
Is	Continuous Source Current <sup>1,4</sup>				1.2	Α
Ism	Pulsed Source Current <sup>2,4</sup>	─V <sub>G</sub> =V <sub>D</sub> =0V , Force Current			5	Α
VsD	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V , I <sub>S</sub> =1A , T <sub>J</sub> =25°C			1.2	V
trr	Reverse Recovery Time	IF=1A , dl/dt=100A/μs ,		14		nS
Qrr	Reverse Recovery Charge	T <sub>J</sub> =25°C		9.3		nC

#### Note

<sup>1.</sup> The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.

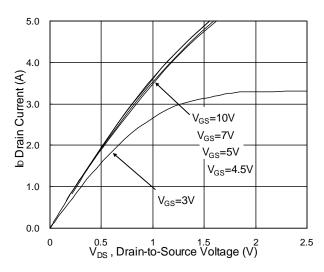
<sup>2.</sup>The data tested by pulsed , pulse width  $\leqq 300 us$  , duty cycle  $\leqq 2\%$ 

<sup>3.</sup> The power dissipation is limited by 150°C junction temperature

<sup>4 .</sup>The data is theoretically the same as  $I_D$  and  $I_{DM}$ , in real applications, should be limited by total power dissipation.



#### **Typical Characteristics**



**Fig.1 Typical Output Characteristics** 

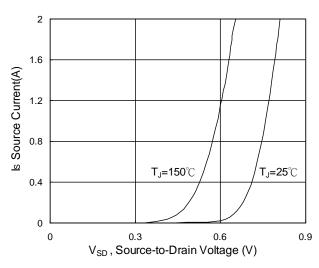


Fig.3 Forward Characteristics of Reverse

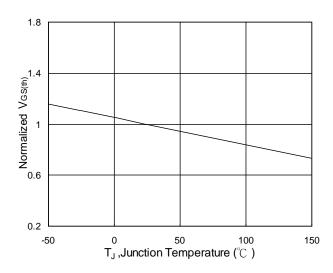


Fig.5 Normalized  $V_{\text{GS(th)}}$  vs.  $T_J$ 

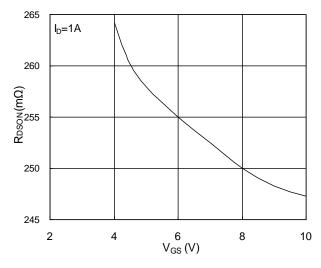


Fig.2 On-Resistance vs. Gate-Source

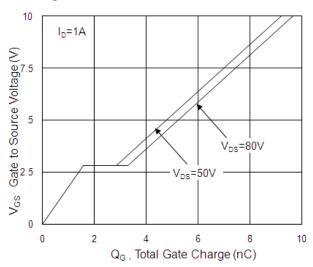


Fig.4 Gate-Charge Characteristics

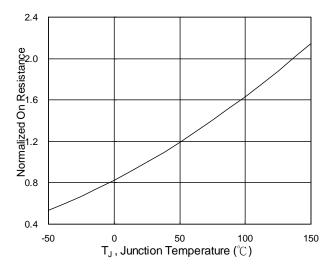
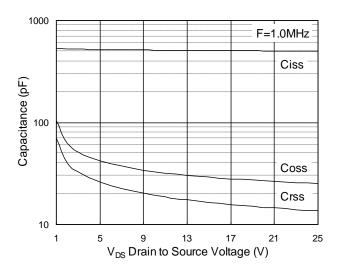


Fig.6 Normalized R<sub>DSON</sub> vs. T<sub>J</sub>







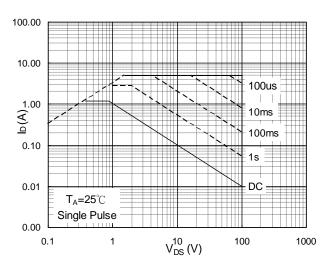


Fig.7 Capacitance

Fig.8 Safe Operating Area

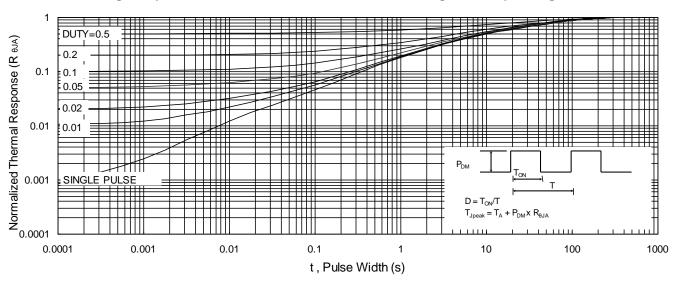
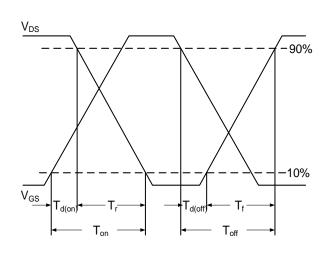


Fig.9 Normalized Maximum Transient Thermal Impedance



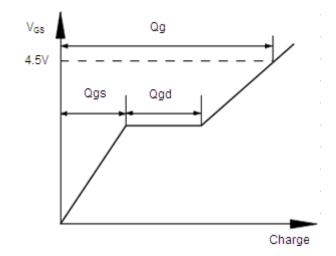
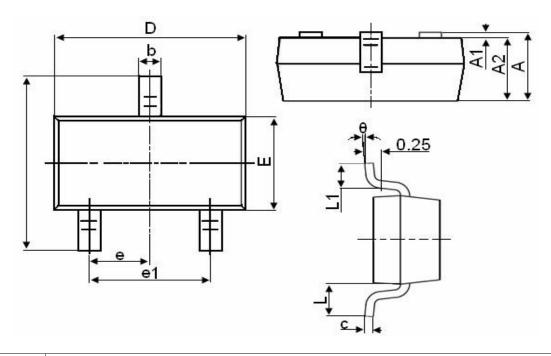


Fig.10 Switching Time Waveform

Fig.11 Gate Charge Waveform



# **SOT-23 Package Information**



Symbol	Dimensions in Millimeters		
Symbol	MIN.	MAX.	
Α	0.900	1.150	
A1	0.000	0.100	
A2	0.900	1.050	
b	0.300	0.500	
С	0.080	0.150	
D	2.800	3.000	
E	1.200	1.400	
E1	2.250	2.550	
е		0.950TYP	
e1	1.800	2.000	
L		0.550REF	
L1	0.300	0.500	
θ	0°	8°	



# 100V N-Channel Enhancement Mode MOSFET Attention

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