

#### Description

The AP15N10D-L uses advanced trench technology to provide excellent  $R_{\text{DS(ON)}}$ , low gate charge and operation with gate voltages as low as 4.5V. This

device is suitable for use as a

Battery protection or in other Switching application.

#### **General Features**

 $V_{DS} = 100V I_{D} = 14.1A$ 

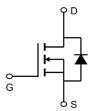
 $R_{DS(ON)}$  < 105m $\Omega$  @  $V_{GS}$ =10V

#### **Application**

Load Switch

**PWM Application** 

Power management







#### **Package Marking and Ordering Information**

Product ID	Pack	Marking	Qty(PCS)	
AP15N10D-L	TO-252-3L	AP15N10D-L XXX YYYY	2500	

#### Absolute Maximum Ratings (T<sub>C</sub>=25°Cunless otherwise noted)

Symbol	Parameter	Rating	Units
VDS	Drain-Source Voltage	100	V
Vgs	Gate-Source Voltage	±20	V
I <sub>D</sub> @T <sub>C</sub> =25°C	Drain Current, V <sub>GS</sub> @ 10V	14.1	Α
I <sub>D</sub> @T <sub>C</sub> =100°C	Drain Current, V <sub>GS</sub> @ 10V	8.1	Α
Ідм	Pulsed Drain Current <sup>1</sup>	28	Α
P <sub>D</sub> @T <sub>C</sub> =25°C	Total Power Dissipation	20.8	W
P <sub>D</sub> @T <sub>A</sub> =25°C	Total Power Dissipation <sup>3</sup>	2	W
Eas	Single Pulse Avalanche Energy <sup>4</sup>	8	mJ
Тѕтс	Storage Temperature Range	-55 to 150	°C
TJ	Operating Junction Temperature Range	-55 to 150	°C
Rthj-c	Maximum Thermal Resistance, Junction-case	6	°C/W
Rthj-a	Maximum Thermal Resistance, Junction-ambient	62.5	°C/W



# **AP15N10D-L**

#### 100V N-Channel Enhancement Mode MOSFET

#### Electrical Characteristics@T<sub>j</sub>=25°C(unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Тур.	Max.	Units
V(BR)DSS	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	100	107	-	V
IDSS	Zero Gate Voltage Drain Current	V <sub>DS</sub> =100V, V <sub>GS</sub> =0V,	-	-	1.0	μΑ
IGSS	Gate to Body Leakage Current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V	-	-	±100	nA
VGS(th)	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.0	1.5	2.5	V
DD0()	Otatia Davia Carras an Basistana antao	V <sub>GS</sub> =10V, I <sub>D</sub> =10A	-	88	105	mΩ
RDS(on)	Static Drain-Source on-Resistance note3	V <sub>GS</sub> =4.5V, I <sub>D</sub> =8A	-	93	125	mΩ
C <sub>iss</sub>	Input Capacitance		-	610	-	pF
Coss	Output Capacitance	$V_{DS}$ =25V, $V_{GS}$ =0V, f=1.0MHz	-	40	-	pF
Crss	Reverse Transfer Capacitance		-	25	-	pF
$Q_g$	Total Gate Charge	V <sub>DS</sub> =30V,	-	12	-	nC
Q <sub>gs</sub>	Gate-Source Charge	I <sub>D</sub> =10A, V <sub>GS</sub> =10V	-	2.2	-	nC
$Q_{gd}$	Gate-Drain("Miller") Charge	VG3 10V	-	2.5	-	nC
td(on)	Turn-on Delay Time		-	7	-	ns
t <sub>r</sub>	Turn-on Rise Time V <sub>DS</sub> =30V, I <sub>D</sub> =5A,		-	5	-	ns
td(off)	Turn-off Delay Time	$R_G=1.8\Omega$ , $V_{GS}=10V$	-	16	-	ns
t <sub>f</sub>	Turn-off Fall Time		-	6	-	ns
IS	Continuous Source Current <sup>1,5</sup>	V <sub>G</sub> =V <sub>D</sub> =0V , Force	-	-	10	Α
ISM	Pulsed Source Current <sup>2,5</sup>	Current	-	-	40	Α
VSD	Diode Forward Voltage <sup>2</sup>	vard Voltage <sup>2</sup> V <sub>GS</sub> =0V, I <sub>S</sub> =10A		-	1.2	V
trr	Body Diode Reverse Recovery Time	1104 dl/dt-1004///-	-	21	-	ns
Qrr	Body Diode Reverse Recovery Charge	l⊧=10A, dl/dt=100A/μs	-	21	-	nC

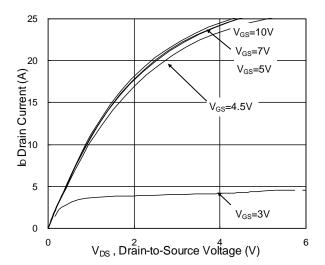
#### Note:

- 1.The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width  $\leq$  300us , duty cycle  $\leq$  2%
- 3. The EAS data shows Max. rating . The test condition is  $V_{DD}$ =25V, $V_{GS}$ =10V,L=0.1mH, $I_{AS}$ =11A
- 4.The power dissipation is limited by 150°C junction temperature
- 5 .The data is theoretically the same as  $I_D$  and  $I_{DM}$ , in real applications, should be limited by total power dissipation.



### **Typical Characteristics**

### **100V N-Channel Enhancement Mode MOSFET**



**Fig.1 Typical Output Characteristics** 

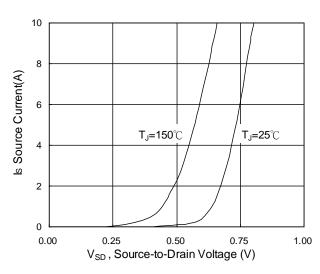


Fig.3 Forward Characteristics Of Reverse

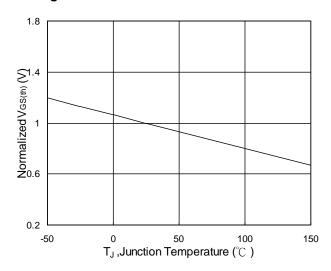


Fig.5 Normalized  $V_{\text{GS(th)}}$  vs.  $T_{\text{J}}$ 

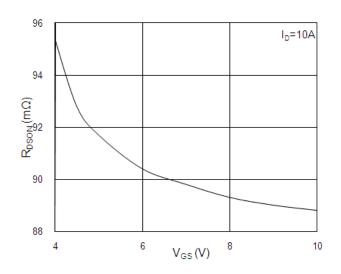


Fig.2 On-Resistance vs. Gate-Source

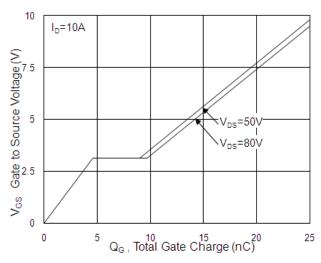


Fig.4 Gate-Charge Characteristics

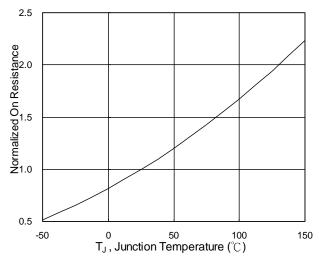
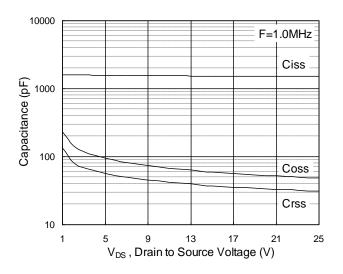


Fig.6 Normalized R<sub>DSON</sub> vs. T<sub>J</sub>







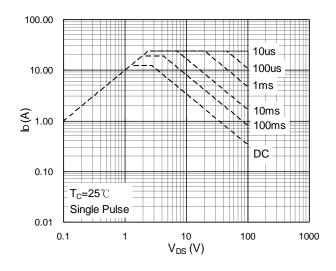


Fig.7 Capacitance

Fig.8 Safe Operating Area

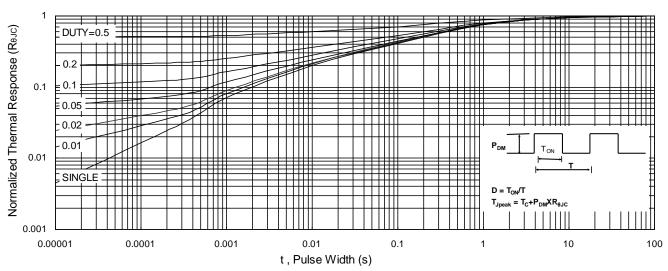


Fig.9 Normalized Maximum Transient Thermal Impedance

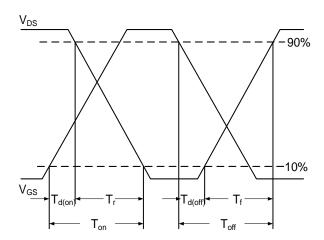


Fig.10 Switching Time Waveform

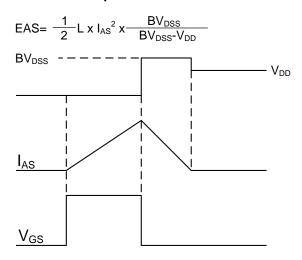
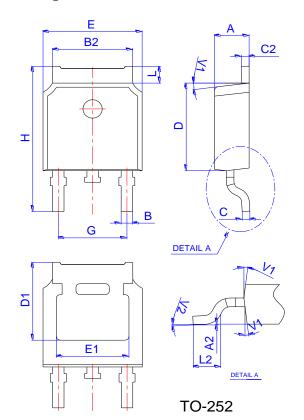


Fig.11 Unclamped Inductive Switching Waveform

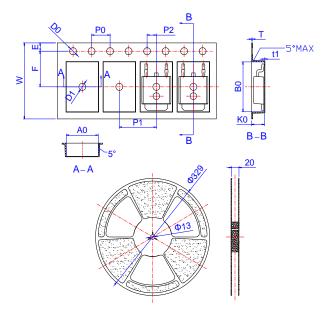


## **Package Mechanical Data**



	Dimensions					
Ref.	Millimeters			Inches		
	Min.	Тур.	Max.	Min.	Тур.	Max.
А	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
В	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
С	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
Н	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°

# **Reel Spectification-TO-252**



	Dimensions					
Ref.	Millimeters			Inches		
	Min.	Тур.	Max.	Min.	Тур.	Max.
W	15.90	16.00	16.10	0.626	0.630	0.634
Е	1.65	1.75	1.85	0.065	0.069	0.073
F	7.40	7.50	7.60	0.291	0.295	0.299
D0	1.40	1.50	1.60	0.055	0.059	0.063
D1	1.40	1.50	1.60	0.055	0.059	0.063
P0	3.90	4.00	4.10	0.154	0.157	0.161
P1	7.90	8.00	8.10	0.311	0.315	0.319
P2	1.90	2.00	2.10	0.075	0.079	0.083
A0	6.85	6.90	7.00	0.270	0.271	0.276
В0	10.45	10.50	10.60	0.411	0.413	0.417
K0	2.68	2.78	2.88	0.105	0.109	0.113
Т	0.24		0.27	0.009		0.011
t1	0.10			0.004		
10P0	39.80	40.00	40.20	1.567	1.575	1.583





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# **AP15N10D-L**

# **100V N-Channel Enhancement Mode MOSFET**

Edition	Date	Change
Rve3.8	2018/1/31	Initial release
Rve3.9	2019/12/01	Reduce RDS(on)

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