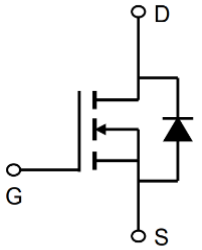
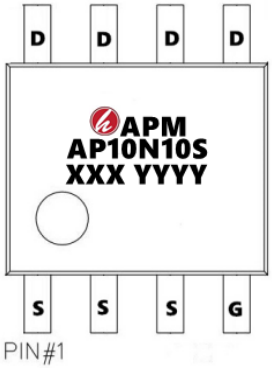
AP10N10S

100V N-Channel Enhancement Mode MOSFET

Description

The AP10N10S uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.





General Features

V_{DS} = 100V I_D =12.3A

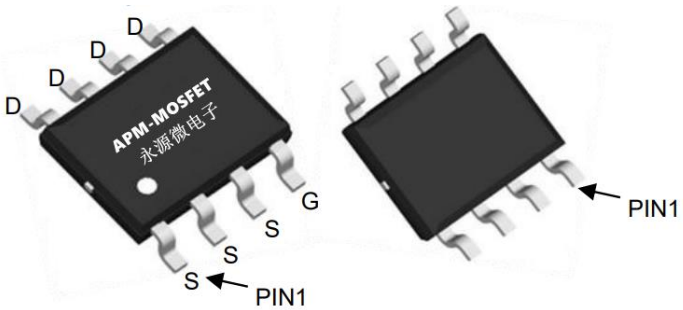
$R_{DS(ON)}$ < 110mΩ@ V_{GS}=10V （Type：93mΩ）

Application

Automative lighting

Load switch

PSE



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP10N10S	SOP-8L	AP10N10S XXX YYYY	3000

Absolute Maximum Ratings (TC=25℃unless otherwise noted)

Symbol	Parameter	Rating	Units
VDS	Drain-Source Voltage	100	V
VGS	Gate-Source Voltage	±20	V
I_D@T_C=25℃	Drain Current, V_{GS} @ 10V	12.3	A
I_D@T_C=100℃	Drain Current, V_{GS} @ 10V	6.5	A
IDM	Pulsed Drain Current[1]	24	A
P_D@T_C=25℃	Total Power Dissipation	30	W
P_D@T_A=25℃	Total Power Dissipation[3]	2.7	W
TSTG	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃
RθJA	Maximum Thermal Resistance, Junctionambient	85	℃/W
RθJC	Maximum Thermal Resistance, Junction-case	5.1	℃/W

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Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Type	Max.	Units
V(BR)DSS	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	100	107	-	V
IDSS	Zero Gate Voltage Drain Current	V_{DS}=100V, V_{GS}=0V,	-	-	1.0	μA
IGSS	Gate to Body Leakage Current	V_{DS}=0V, V_{GS}=±20V	-	-	±100	nA
VGS(th)	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	1.0	1.5	2.5	V
RDS(on)	Static Drain-Source on-Resistance	V_{GS}=10V, I_D=5A	-	93	110	mΩ
		V_{GS}=4.5V, I_D=3A	-	100	140	mΩ
Ciss	Input Capacitance	V_{DS}=25V, V_{GS}=0V, f=1.0MHz	-	645	-	pF
Coss	Output Capacitance		-	38	-	pF
Crss	Reverse Transfer Capacitance		-	33	-	pF
Q_g	Total Gate Charge	V_{DS}=30V, I_D=5A, V_{GS}=10V	-	12	-	nC
Qgs	Gate-Source Charge		-	2.2	-	nC
Qgd	Gate-Drain("Miller") Charge		-	2.5	-	nC
td(on)	Turn-on Delay Time	V_{DS}=30V, I_D=10A, R_G=1.8Ω, V_{GS}=10V	-	7	-	ns
tr	Turn-on Rise Time		-	5	-	ns
td(off)	Turn-off Delay Time		-	16	-	ns
t_f	Turn-off Fall Time		-	6	-	ns
IS	Maximum Continuous Drain to Source Diode Forward Current		-	-	10	A
ISM	Maximum Pulsed Drain to Source Diode Forward Current		-	-	40	A
VSD	Drain to Source Diode Forward Voltage	V_{GS}=0V, I_S=10A	-	-	1.2	V
trr	Body Diode Reverse Recovery Time	I_F=10A, dI/dt=100A/μs	-	21	-	ns
Qrr	Body Diode Reverse Recovery Charge		-	21	-	nC

Note :

1、The data tested by surface mounted on a 1 inch 2 FR-4 board with 2OZ copper.

2、The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%

3、The power dissipation is limited by 150℃ junction temperature

4、The data is theoretically the same as I D and I DM , in real applications , should be limited by total power dissipation.

Typical Characteristics

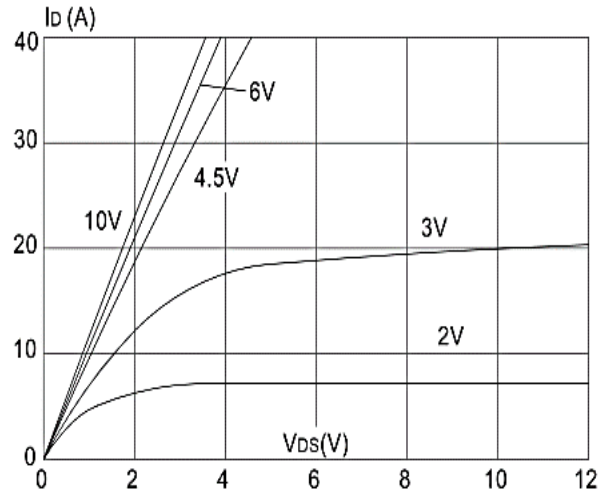


Figure1: Output Characteristics

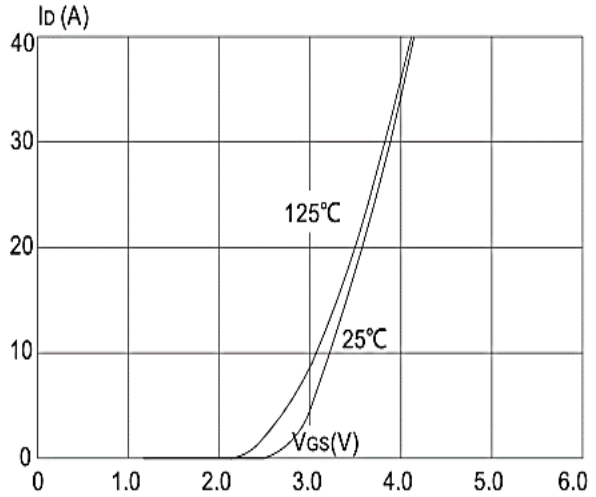


Figure 2: Typical Transfer Characteristics

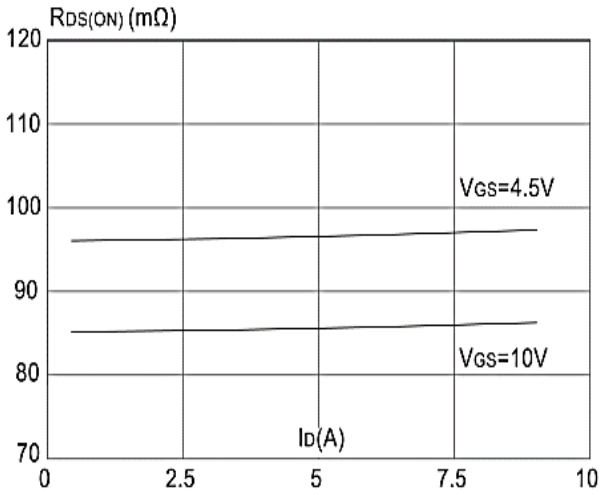


Figure 3:On-resistance vs. Drain Current

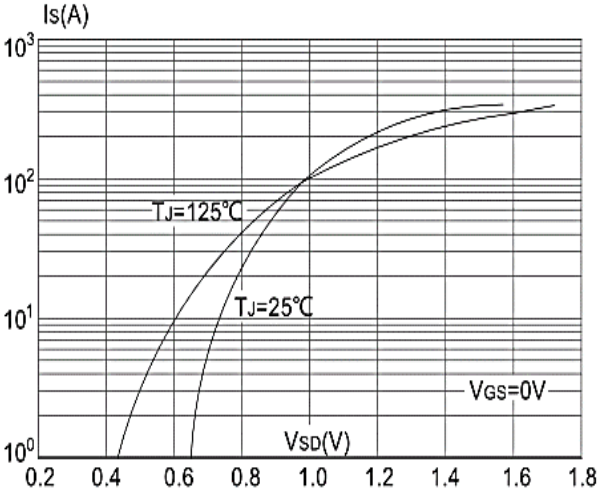


Figure 4: Body Diode Characteristics

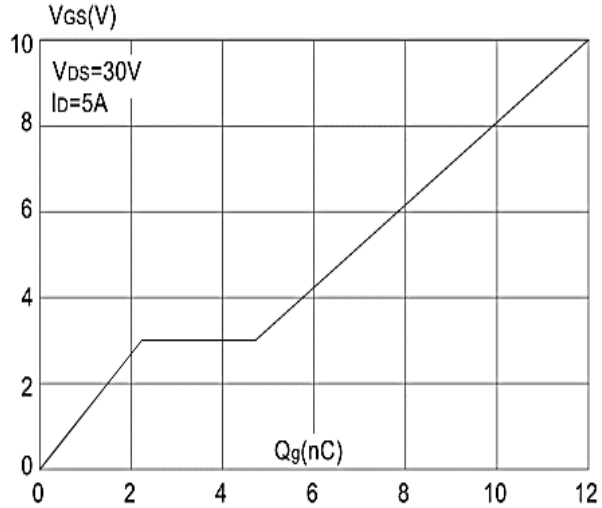


Figure 5: Gate Charge Characteristics

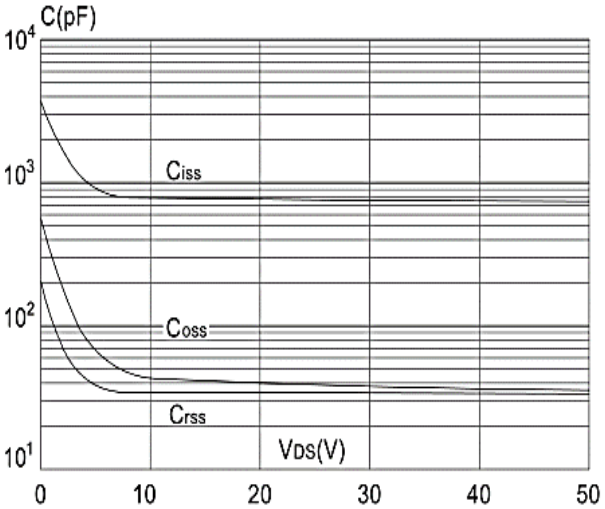


Figure 6: Capacitance Characteristics

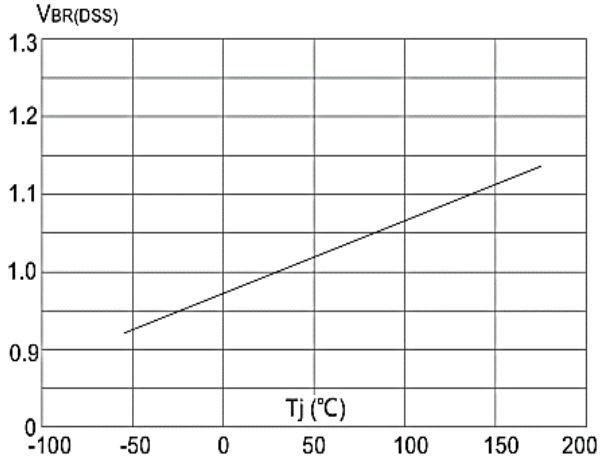


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

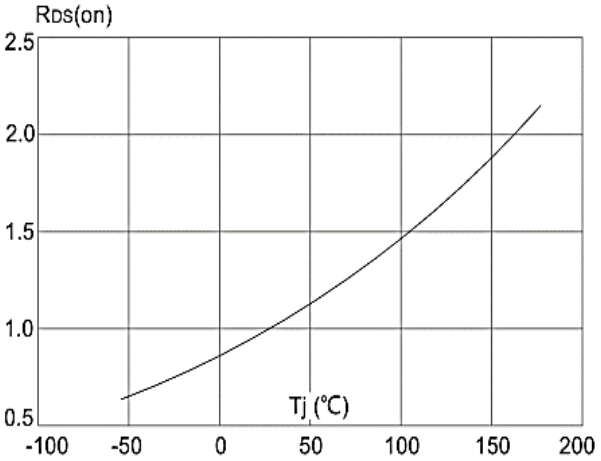


Figure 8: Normalized on Resistance vs. Junction Temperature

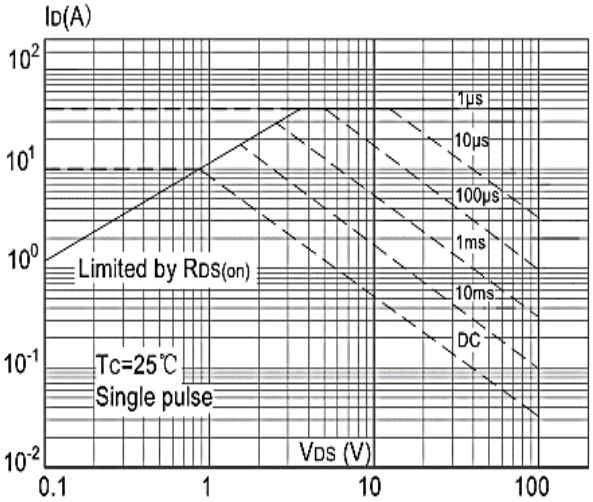


Figure 9: Maximum Safe Operating Area

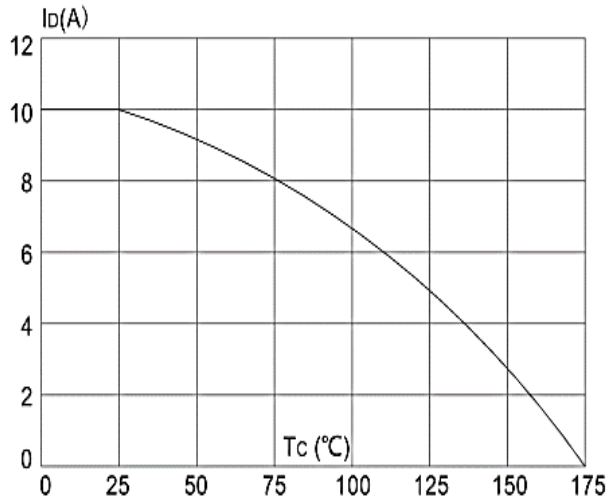


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

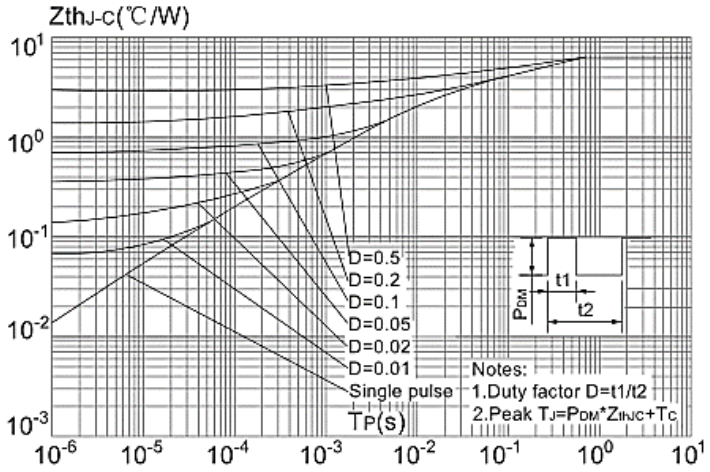
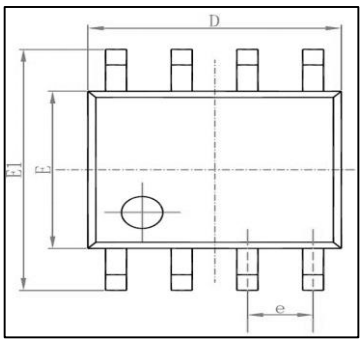
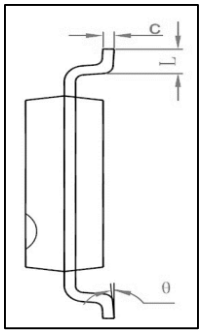
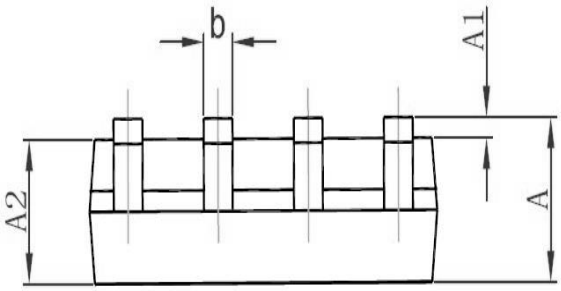


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Case

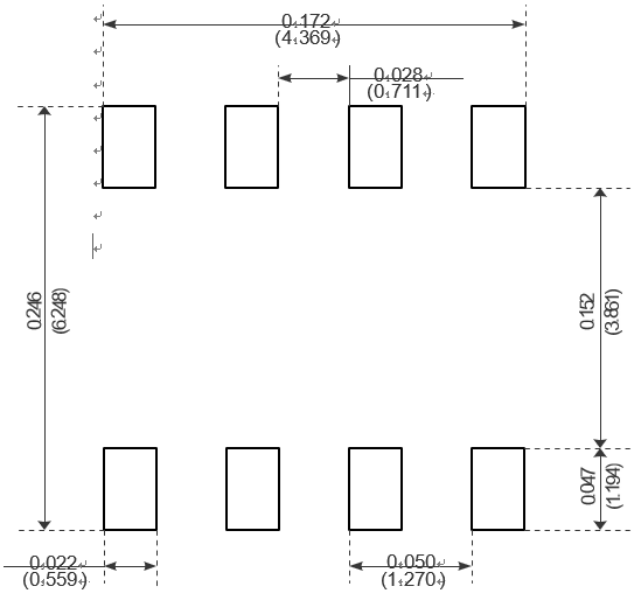
Package Mechanical Data-SOP-8







Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



Recommended Minimum Pads

100V N-Channel Enhancement Mode MOSFET

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Edition	Date	Change
Rve1.0	2020/1/31	Initial release