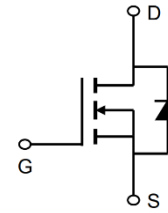


200V N-Channel Enhancement Mode MOSFET

Description

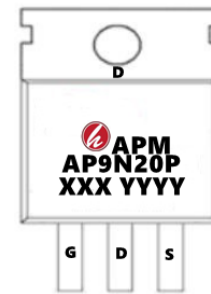
The AP9N20D is silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency.



General Features

$V_{DS} = 200V$ $I_D = 9A$

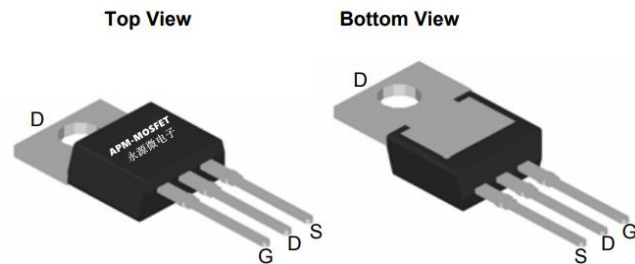
$R_{DS(ON)} < 300m\Omega$ @ $V_{GS}=10V$ (Type: 230m Ω)



Application

Uninterruptible Power Supply(UPS)

Power Factor Correction (PFC)



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP9N20P	TO-220-3L	AP9N20P XXX YYYY	1000

Absolute Maximum Ratings ($T_C=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Value	Unit
		TO-220-3L	
V_{DS}	Drain-Source Voltage ($V_{GS} = 0V$)	200	V
I_D	Continuous Drain Current	9	A
I_{DM}	Pulsed Drain Current (note1)	36	A
V_{GS}	Gate-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy (note2)	100	mJ
I_{AR}	Avalanche Current (note1)	7.5	A
E_{AR}	Repetitive Avalanche Energy (note1)	8.1	mJ
P_D	Power Dissipation ($T_C = 25^\circ C$)	74	W
T_J, T_{stg}	Operating Junction and Storage Temperature Range	-55~+150	$^\circ C$
R_{thJC}	Thermal Resistance, Junction-to-Case	1.7	$^\circ C/W$
R_{thJA}	Thermal Resistance, Junction-to-Ambient	62.5	$^\circ C/W$

200V N-Channel Enhancement Mode MOSFET

Electrical Characteristics (T_J=25°C, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
V(BR)DSS	Drain-Source Breakdown Voltage	VGS = 0V, ID = 250μA	200	222	--	V
IDSS	Zero Gate Voltage Drain Current	VDS = 200V, VGS = 0V, T _J = 25°C	--	--	5	μA
IDSS	Zero Gate Voltage Drain Current	VDS = 160V, VGS = 0V, T _J = 125°C	--	--	100	
IGSS	Gate-Source Leakage	VGS = ±20V	--	--	±100	nA
VGS(th)	Gate-Source Threshold Voltage	VDS = VGS, ID = 250μA	2.0	3.5	4.0	V
RDS(on)	Drain-Source On-Resistance	VGS = 10V, ID = 4.5A	--	0.23	0.3	Ω
Ciss	Input Capacitance	VGS = 0V, VDS = 25V, f = 1.0MHz	--	684	--	pF
Coss	Output Capacitance		--	103	--	
Crss	Reverse Transfer Capacitance		--	37	--	
Qg	Total Gate Charge	VDD = 160V, ID = 9.0A, VGS = 10V	--	23	--	nC
Qgs	Gate-Source Charge		--	2.5	--	
Qgd	Gate-Drain Charge		--	10	--	
td(on)	Turn-on Delay Time	VDD = 100V, ID = 9.0A, RG = 25 Ω	--	12	--	ns
tr	Turn-on Rise Time		--	22	--	
td(off)	Turn-off Delay Time		--	50	--	
tf	Turn-off Fall Time		--	48	--	
IS	Continuous Body Diode Current	TC = 25 °C	--	--	9	A
ISM	Pulsed Diode Forward Current		--	--	36	
VSD	Body Diode Voltage	T _J = 25°C, ISD = 9A, VGS = 0V	--	--	1.4	V
trr	Reverse Recovery Time	VGS = 0V, IS = 9A, diF/dt = 100A /μs	--	190	--	ns
Qrr	Reverse Recovery Charge		--	1.7	--	μC

Note :

- 1、 The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2、 The EAS data shows Max. rating . IAS = 7.5A, VDD = 50V, RG = 25 Ω, Starting T_J = 25 °C
- 3、 The test condition is Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 1%
- 4、 The power dissipation is limited by 150°C junction temperature
- 5、 The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

Typical Characteristics

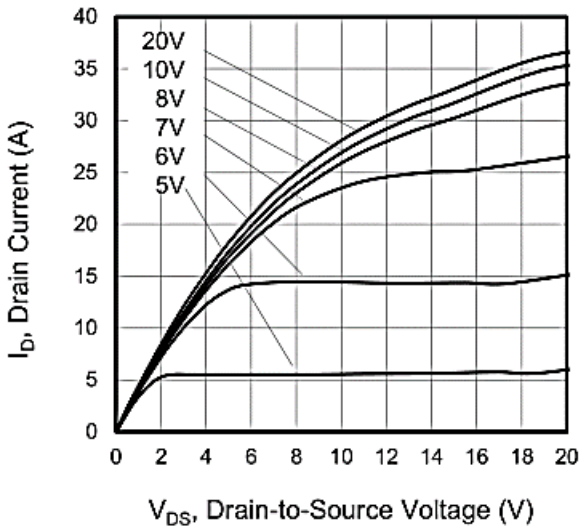


Figure 1. Output Characteristics ($T_J = 25^\circ\text{C}$)

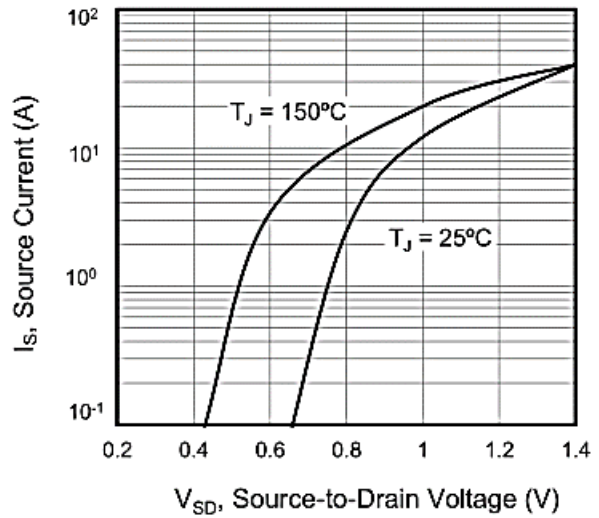


Figure 2. Body Diode Forward Voltage

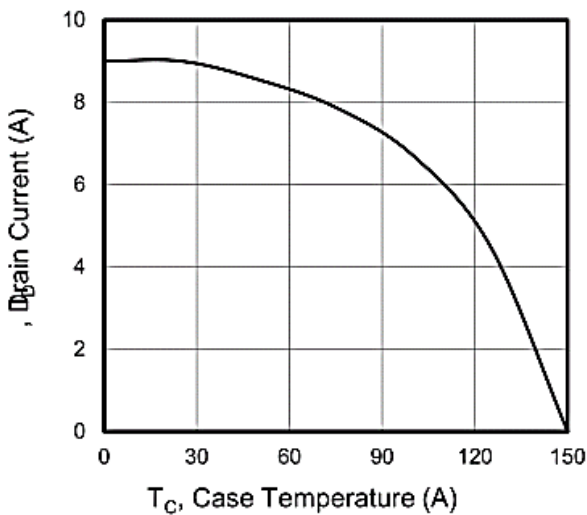


Figure 3. Drain Current vs. Temperature

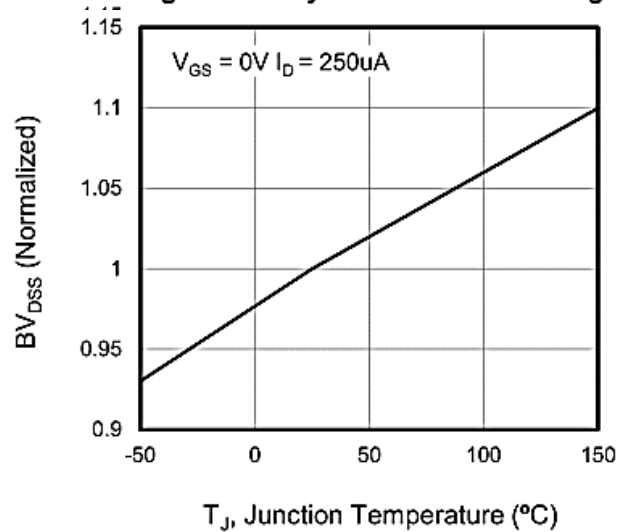


Figure 4. BV_{DSS} Variation vs. Temperature

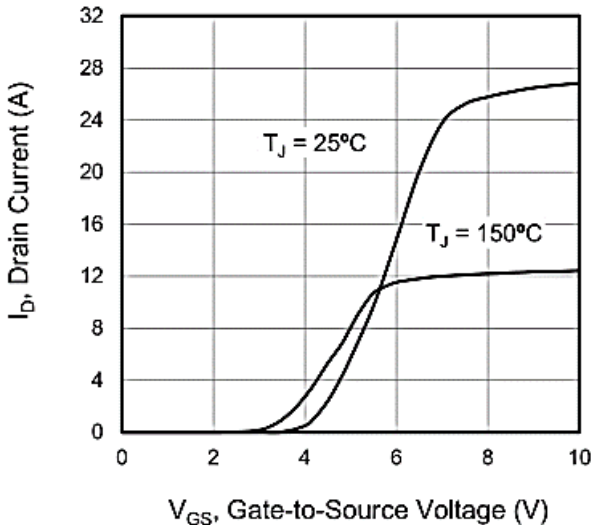


Figure 5. Transfer Characteristics

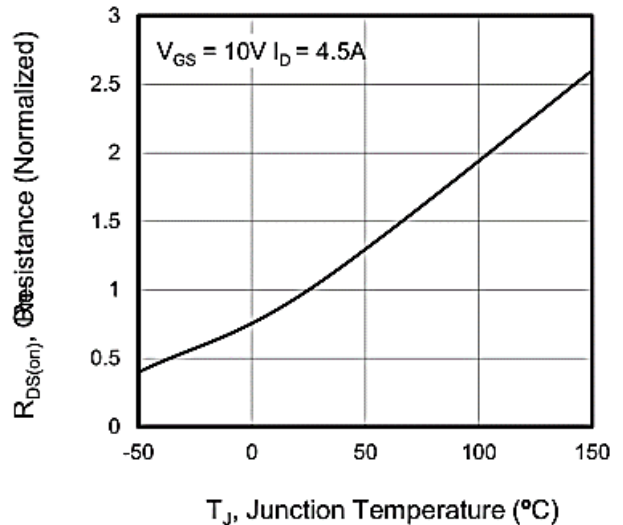


Figure 6. On-Resistance vs. Temperature



200V N-Channel Enhancement Mode MOSFET

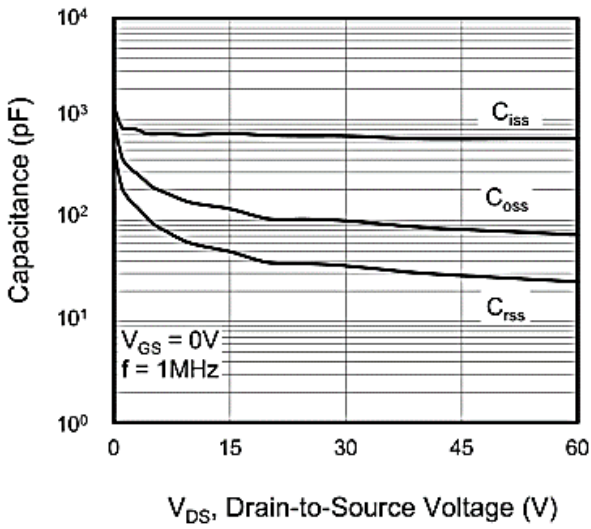


Figure 7. Capacitance

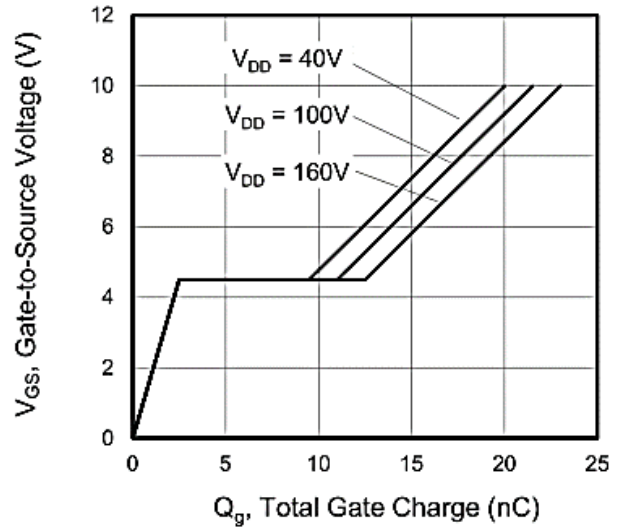


Figure 8. Gate Charge

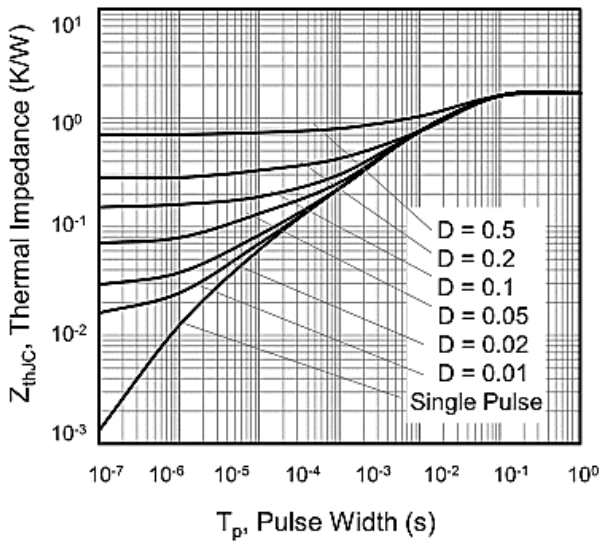
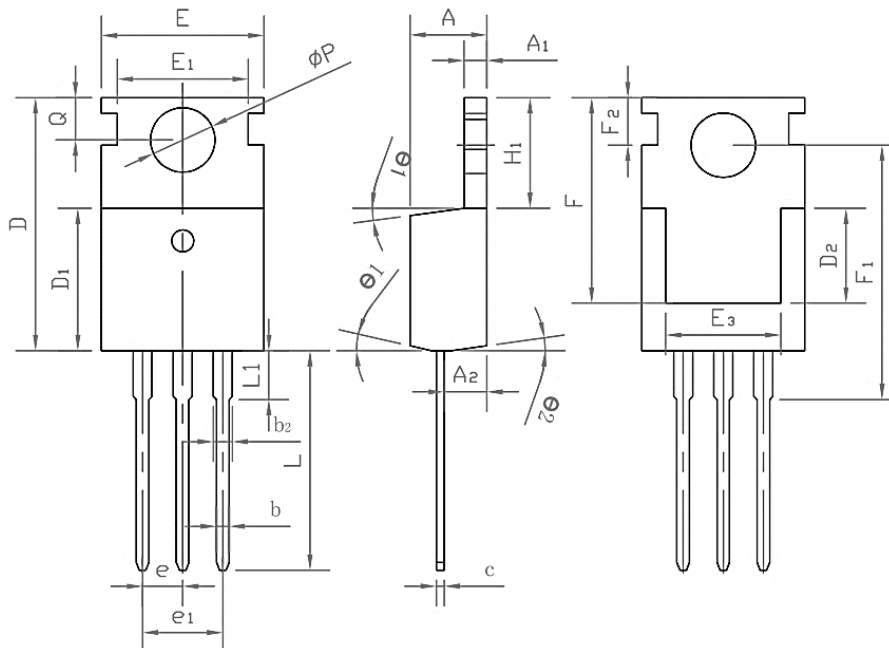


Figure 10. Transient Thermal Impedance

Package Mechanical Data-TO-220-3L-SLK



Symbol	Common		
	mm		
	Mim	Nom	Max
A	4.27	4.57	4.87
A1	1.15	1.30	1.45
A2	2.10	2.40	2.70
b	0.70	0.80	1.00
b2	1.17	1.27	1.50
D	0.40	0.50	0.65
D1	8.80	9.10	9.40
D2	5.70	6.70	7.00
E	9.70	10.00	10.30
E1	-	8.70	-
E2	9.63	10.00	10.35
E3	7.00	8.00	8.40
e		0.37	
e1		0.10	
H1	6.00	6.50	6.85
L	12.75	13.50	13.90
L1	-	3.10	3.40
Phi _p	3.45	3.60	3.75
Q	2.60	2.80	3.00
theta ₁	4°	7°	10°
theta ₂	0°	3°	6°
F	13.30	13.50	13.70
F1	15.50	15.90	16.30
F2	2.80	3.00	3.20

200V N-Channel Enhancement Mode MOSFET**Attention**

1, Any and all APM Microelectronics products described or contained herein do not have specifications that can handle applications that require extremely high levels of reliability, such as life support systems, aircraft's control systems, or other applications whose failure can be reasonably expected to result in serious physical and/or material damage. Consult with your APM Microelectronics representative nearest you before using any APM Microelectronics products described or contained herein in such applications.

2, APM Microelectronics assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all APM Microelectronics products described or contained herein.

3, Specifications of any and all APM Microelectronics products described or contained here instipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer's products or equipment.

4, APM Microelectronics Semiconductor CO., LTD. strives to supply high quality high reliability products. However, any and all semiconductor products fail with some probability. It is possible that these probabilistic failures could give rise to accidents or events that could endanger human lives that could give rise to smoke or fire, or that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.

5, In the event that any or all APM Microelectronics products (including technical data, services) described or contained herein are controlled under any of applicable local export control laws and regulations, such products must not be exported without obtaining the export license from the authorities concerned in accordance with the above law.

6, No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written permission of APM Microelectronics Semiconductor CO., LTD.

7, Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. APM Microelectronics believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

8, Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the APM Microelectronics product that you intend to use.

200V N-Channel Enhancement Mode MOSFET

Edition	Date	Change
Rve1.0	2021/1/31	Initial release

Copyright Attribution "APM-Microelectronice"

