

### -30V P-Channel Enhancement Mode MOSFET

#### Description

The AP9435A uses advanced trench technology

to provide excellent  $R_{\text{DS}(\text{ON})},$  low gate charge and

operation with gate voltages as low as 4.5V. This

device is suitable for use as a

Battery protection or in other Switching application.

#### **General Features**

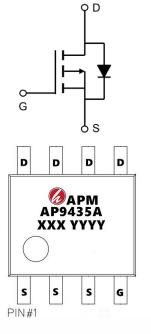
V<sub>DS</sub> = -30V I<sub>D</sub> =-6A

 $R_{DS(ON)} < 55m\Omega @ V_{GS}=10V$ 

#### Application

Battery protection

Load switch Uninterruptible power supply





#### Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)		
AP9435A	SOP-8	AP9435A XXXX YYYY	3000		
Absolute Maximum Ratings (T <sub>c</sub> =25 <sup>°</sup> C unless otherwise noted)					
Symbol	Parameter	Max.	Units		
VDSS	Drain-Source Voltage	-30	V		
VGSS	Gate-Source Voltage	±20	V		
I₀@Tc=25℃	Continuous Drain Current, V <sub>GS</sub> @ -10V <sup>1</sup>	-6.0	А		
I₀@Tc=100°C	Continuous Drain Current, V <sub>GS</sub> @ -10V <sup>1</sup>	-3.3	А		
IDM	Pulsed Drain Current note1	-20.4	А		
PD	Power Dissipation $T_A = 25^{\circ}C$ 2.15V		W		
RθJA	Thermal Resistance, Junction to Ambient	58	°C/W		
TJ, TSTG	Operating and Storage Temperature Range	-55 to +150	℃		

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Symbol	Parameter	<b>Test Condition</b>	Min.	Тур.	Max.	Units
V(BR)DSS	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> = -250µA	-30	-33	-	V
IDSS	Zero Gate Voltage Drain Current	$V_{DS}$ = -30V, $V_{GS}$ = 0V,	-	-	-1	μA
IGSS	Gate to Body Leakage Current	$V_{DS}$ =0V, $V_{GS}$ = ±20V	-	-	±100	nA
VGS(th)	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250µA	-1.0	-1.6	-2.5	V
RDS(on)	Static Drain-Source on-Resistance note2 -	V <sub>GS</sub> =-10V, I <sub>D</sub> =-5A	-	43	55	mΩ
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-4A	-	65	90	
Ciss	Input Capacitance		-	596	-	pF
Coss	Output Capacitance	$V_{DS}$ = -15V, $V_{GS}$ = 0V, f = 1.0MHz	-	95	-	pF
Crss	Reverse Transfer Capacitance		-	68	-	pF
Qg	Total Gate Charge		-	6.8	-	nC
Qgs	Gate-Source Charge	V <sub>DS</sub> = -15V, I <sub>D</sub> = -5.1A, V <sub>GS</sub> = -10V	-	1	-	nC
Q <sub>gd</sub>	Gate-Drain("Miller") Charge		-	1.4	-	nC
td(on)	Turn-on Delay Time		-	14	-	ns
tr	Turn-on Rise Time	V <sub>DD</sub> = -15V, I <sub>D</sub> = -1A,	-	61	-	ns
td(off)	Turn-off Delay Time	V <sub>GS</sub> =-10V, R <sub>GEN</sub> =2.5Ω	-	19	-	ns
t <sub>f</sub>	Turn-off Fall Time		-	10	-	ns
IS	Maximum Continuous Drain to Source Diode Forward Current		-	-	-5.1	А
ISM	Maximum Pulsed Drain to Source Diode Forward Current		-	-	-20.4	А
VSD	Drain to Source Diode Forward Voltage	V <sub>GS</sub> = 0V, I <sub>S</sub> = -5.1A	-	-0.8	-1.2	V

#### Electrical Characteristics (TJ=25 °C, unless otherwise noted)

Note :

 $1_{\mbox{\tiny V}}$  The data tested by surface mounted on a 1 inch 2 FR-4 board with 2OZ copper.

2、The data tested by pulsed , pulse width  $\,\leq\,$  300us , duty cycle  $\,\leq\,$  2%

3、The EAS data shows Max. rating . The test condition is VDD=-25V,VGS=-10V,L=0.1mH,IAS=-5A

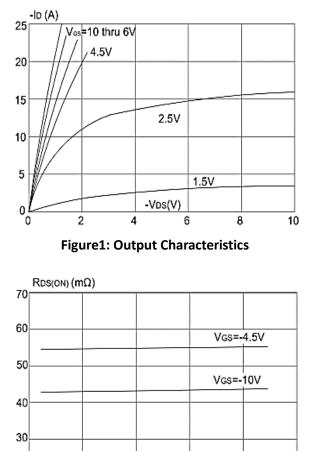
 $4\,{\scriptstyle \sim}\,$  The power dissipation is limited by  $150\,{\rm ^\circ C}$  junction temperature

5. The data is theoretically the same as ID and IDM, in real applications, should be limited by total power dissipation.

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#### **Typical Characteristics**



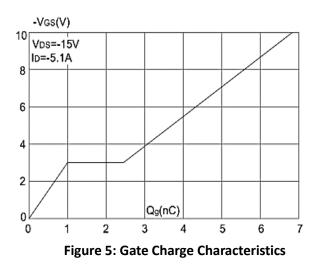
6

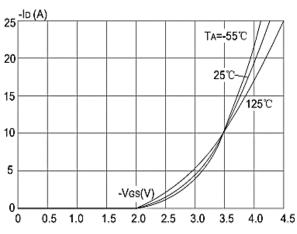
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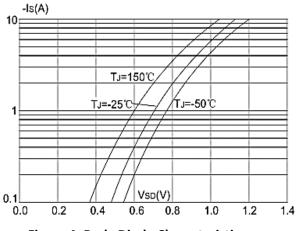
-ID(A)

4

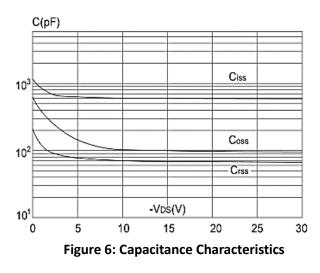










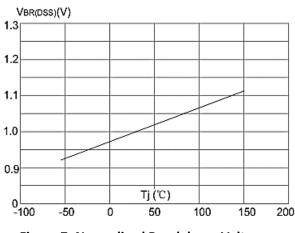


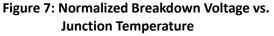
20l

2



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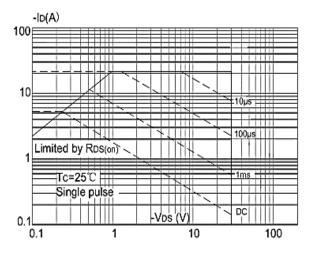


Figure 9: Maximum Safe Operating Area vs. Case Temperature

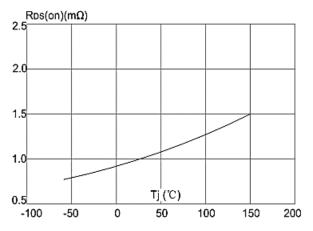


Figure 8: Normalized on Resistance vs Junction Temperature

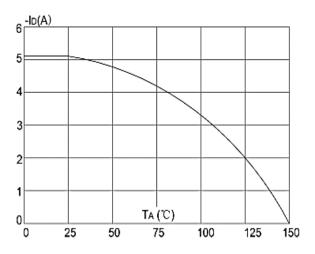
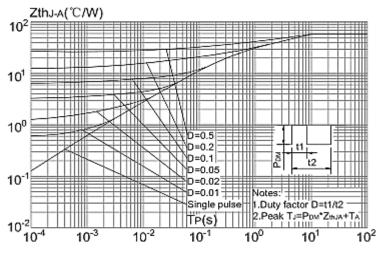


Figure 10: Maximum Continuous Drain Current





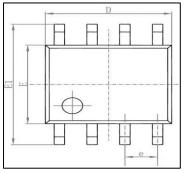


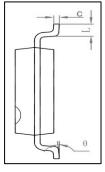


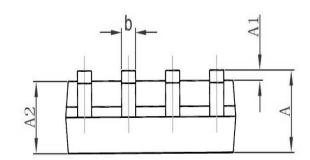
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Transient Thermal Impedance, Junction-to-Case

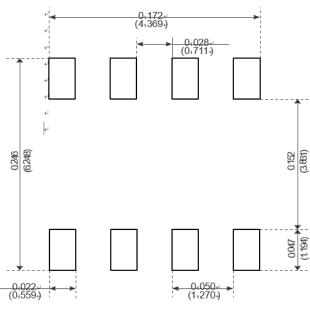
# Package Mechanical Data-SOP-8







Cumb a l	Dimensions In	n Millimeters	Dimensions	In Inches
Symbol	Min	Max	Min	Max
А	1.350	1.750	0.053	0.069
A1	0.100	0. 250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0. 330	0.510	0.013	0.020
С	0.170	0. 250	0.006	0.010
D	4. 700	5.100	0. 185	0.200
E	3.800	4.000	0.150	0. 157
E1	5.800	6.200	0. 228	0. 244
e	1. 270	(BSC)	0.050	(BSC)
L	0. 400	1. 270	0.016	0.050
θ	<b>0</b> °	8°	<b>0</b> °	8°



Recommended Minimum Pads.

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## -30V P-Channel Enhancement Mode MOSFET

Edition	Date	Change
Rve3.8	2018/11/31	Initial release
Rve3.9	2020/5/31	Reduce RDS(on)

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AP9435A RVE3.9