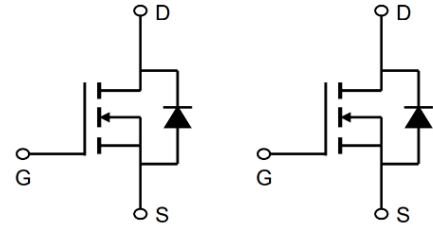


60V N+N-Channel Enhancement Mode MOSFET

Description

The AP6946A uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a

Battery protection or in other Switching application.



General Features

$V_{DS} = 60V$ $I_D = 7.2A$

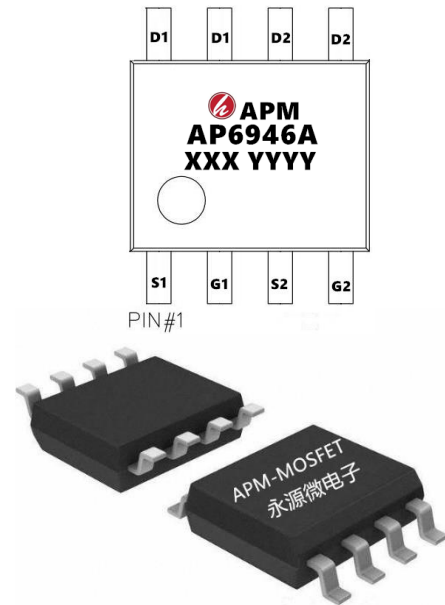
$R_{DS(ON)} < 35m\Omega @ V_{GS}=10V$

Application

Battery protection

Load switch

Uninterruptible power supply



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP6946A	SOP-8	AP6946A XXX YYYY	3000

Absolute Maximum Ratings ($T_C=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Rating	Units
V _{DS}	Drain-Source Voltage	60	V
V _{GS}	Gate-Source Voltage	±20	V
$I_D@T_A=25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^1$	7.2	A
$I_D@T_A=70^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^1$	4.8	A
IDM	Pulsed Drain Current ²	14.6	A
EAS	Single Pulse Avalanche Energy ³	21.5	mJ
IAS	Avalanche Current	20.6	A
$P_D@T_A=25^\circ\text{C}$	Total Power Dissipation ⁴	1.2	W
TSTG	Storage Temperature Range	-55 to 150	°C
T _J	Operating Junction Temperature Range	-55 to 150	°C
R _{θJA}	Thermal Resistance Junction-Ambient ¹	62.5	°C/W
R _{θJC}	Thermal Resistance Junction-Case ¹	36	°C/W

60V N+N-Channel Enhancement Mode MOSFET

Electrical Characteristics (T_J=25°C, unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V(BR)DSS	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	60	65	-	V
IDSS	Zero Gate Voltage Drain Current	V _{DS} =60V, V _{GS} =0V,	-	-	1.0	μA
IGSS	Gate to Body Leakage Current	V _{DS} =0V, V _{GS} =±20V	-	-	±100	nA
VGS(th)	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.0	1.6	2.5	V
RDS(on)	Static Drain-Source on-Resistance note3	V _{GS} =10V, I _D =10A	-	28	35	mΩ
		V _{GS} =4.5V, I _D =5A	-	33	45	
C _{iss}	Input Capacitance	V _{DS} =25V, V _{GS} =0V, f=1.0MHz	-	1148	-	pF
C _{oss}	Output Capacitance		-	58.5	-	pF
C _{rss}	Reverse Transfer Capacitance		-	49.4	-	pF
Q _g	Total Gate Charge	V _{DS} =30V, I _D =10A, V _{GS} =10V	-	20.3	-	nC
Q _{gs}	Gate-Source Charge		-	3.7	-	nC
Q _{gd}	Gate-Drain("Miller") Charge		-	5.3	-	nC
td(on)	Turn-on Delay Time	V _{DS} =30V, I _D =20A, R _G =1.8Ω, V _{GS} =10V	-	7.6	-	ns
t _r	Turn-on Rise Time		-	20	-	ns
td(off)	Turn-off Delay Time		-	15	-	ns
t _f	Turn-off Fall Time		-	24	-	ns
IS	Maximum Continuous Drain to Source Diode Forward Current		-	-	20	A
ISM	Maximum Pulsed Drain to Source Diode Forward Current		-	-	80	A
VSD	Drain to Source Diode Forward Voltage	V _{GS} =0V, I _S =20A	-	-	1.2	V
trr	Body Diode Reverse Recovery Time	I _F =20A, dI/dt=100A/μs	-	29	-	ns
Qrr	Body Diode Reverse Recovery Charge		-	43	-	nC

Notes:

- 1、 Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
- 2、 EAS condition : T_J =25°C, V_{DD} =30V, V_G =10V, L=0.5mH, R_G=25Ω, I_{AS} =8.5A
- 3、 Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%

60V N+N-Channel Enhancement Mode MOSFET

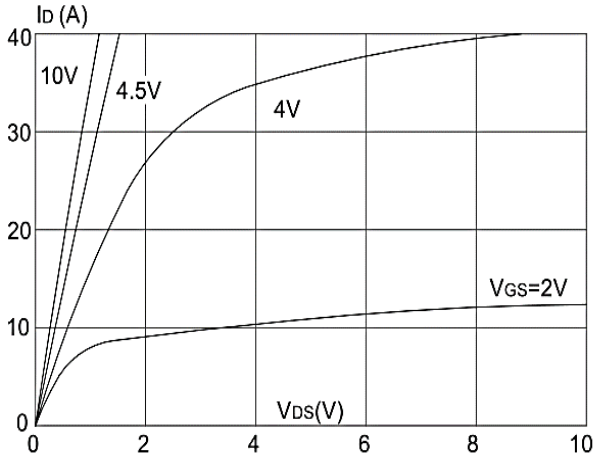


Figure 1: Output Characteristics

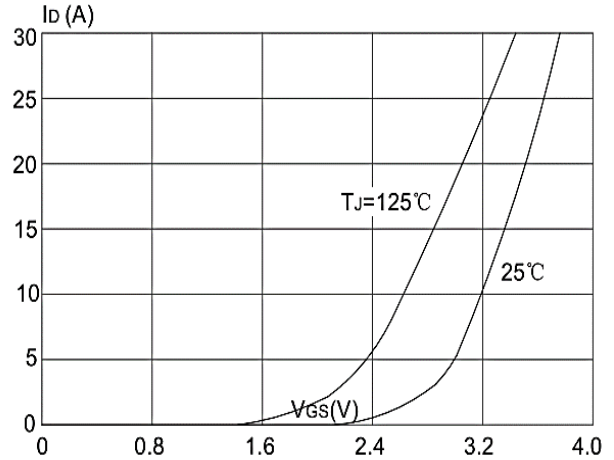


Figure 2: Typical Transfer Characteristics

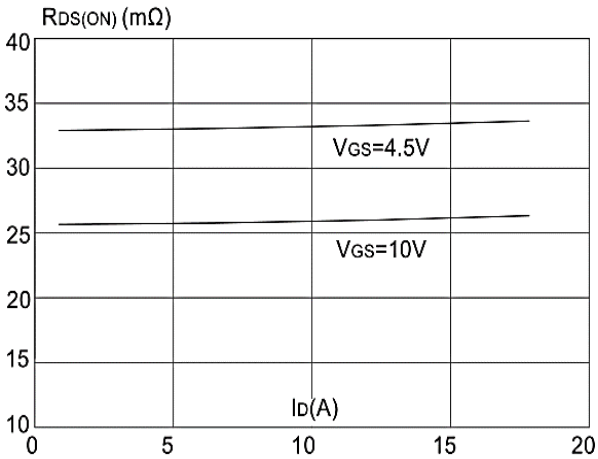


Figure 3: On-resistance vs. Drain Current

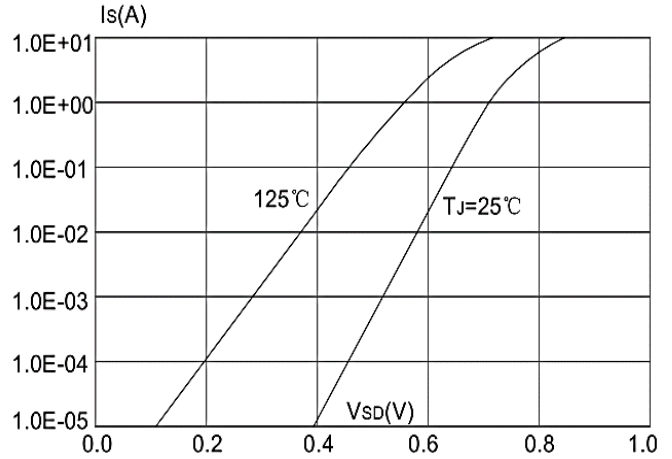


Figure 4: Body Diode Characteristics

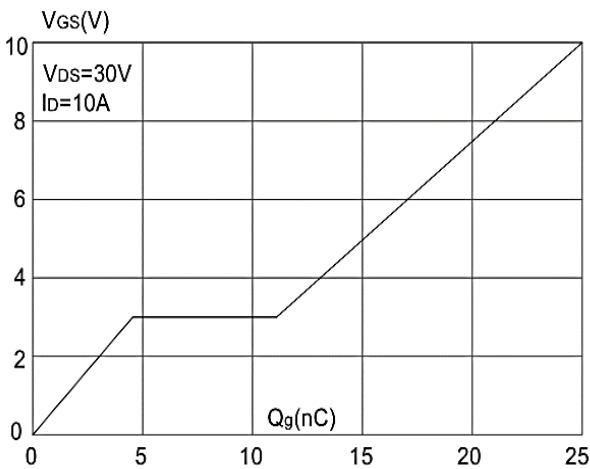


Figure 5: Gate Charge Characteristics

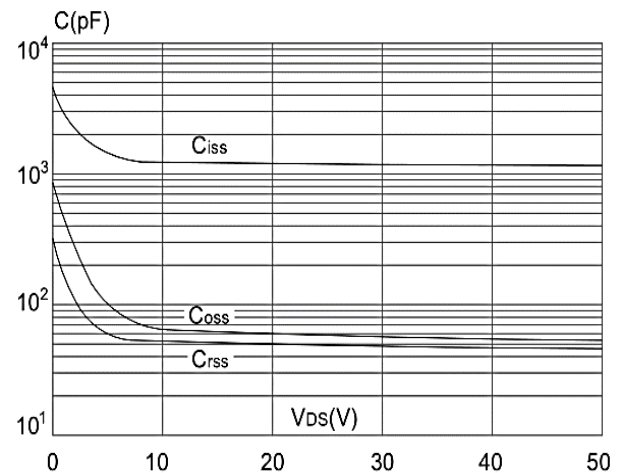


Figure 6: Capacitance Characteristics



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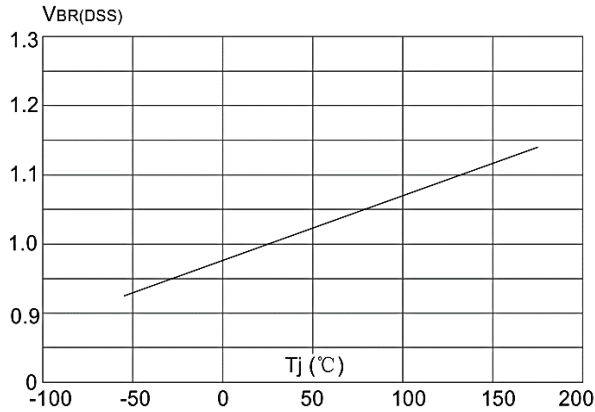


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

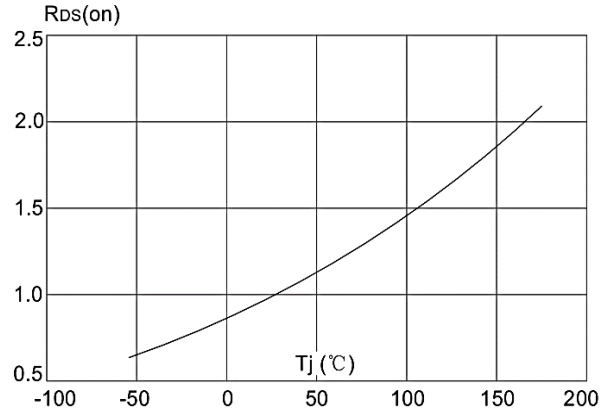


Figure 8: Normalized on Resistance vs. Junction Temperature

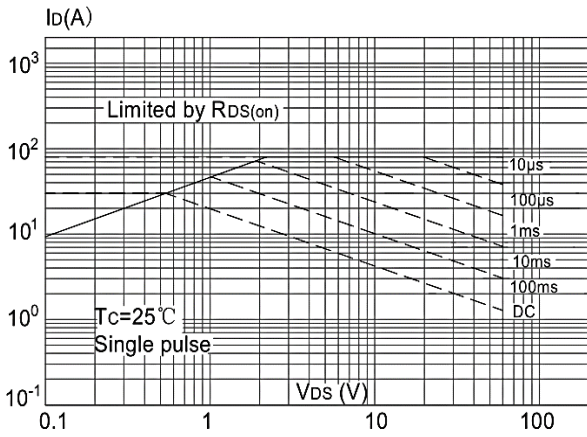


Figure 9: Maximum Safe Operating Area vs. Case Temperature

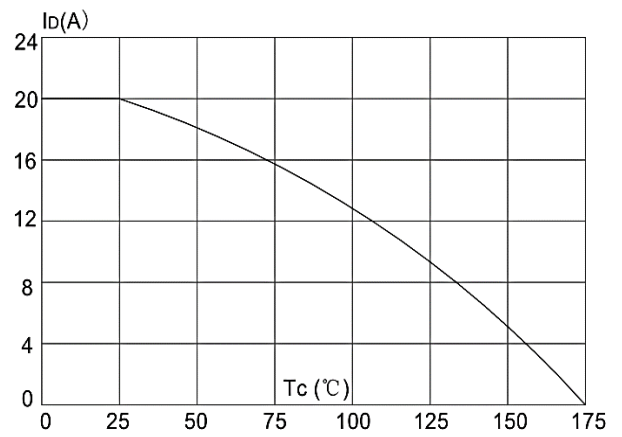


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

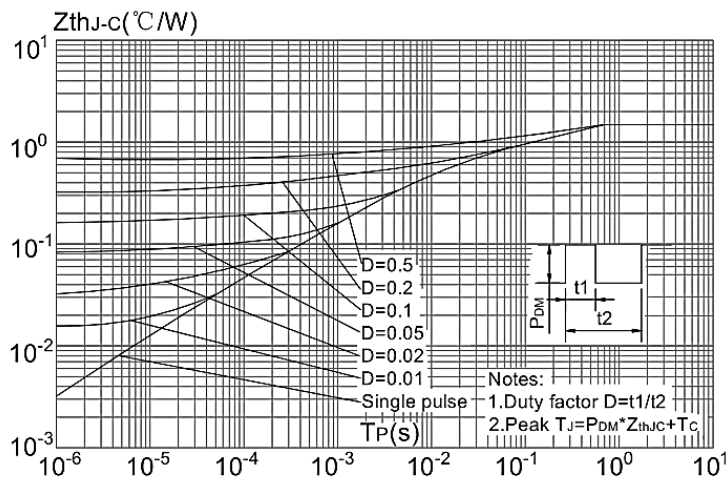
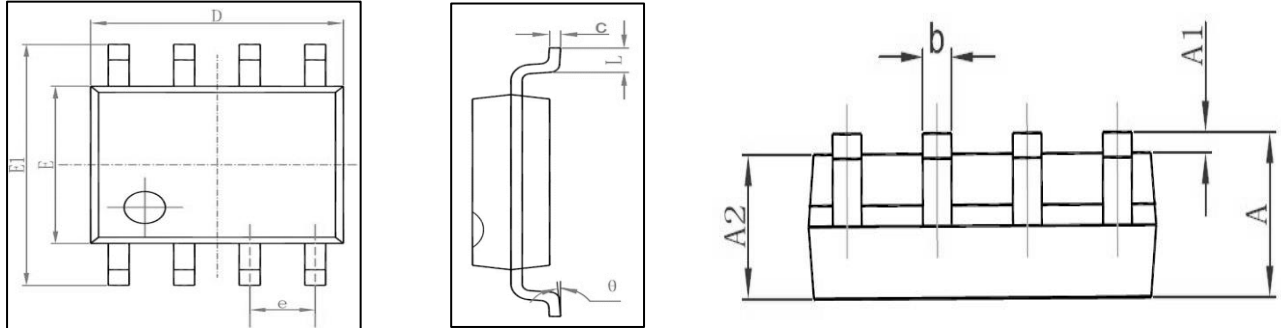
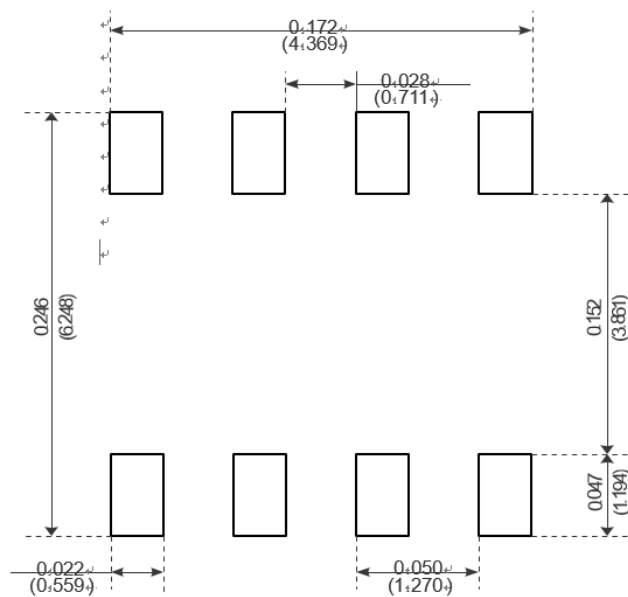


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Case

Package Mechanical Data-SOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



Recommended Minimum Pads

60V N+N-Channel Enhancement Mode MOSFET**Attention**

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Edition	Date	Change
Rve1.0	2020/6/11	Initial release

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