

## -100V P-Channel Enhancement Mode MOSFET

### Description

The AP50P10P uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a

Battery protection or in other Switching application.

### **General Features**

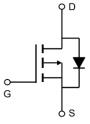
V<sub>DS</sub> = -100V I<sub>D</sub> =-50 A

 $R_{DS(ON)} < 50m\Omega @ V_{GS}=10V$ 

### Application

Battery protection

Load switch Uninterruptible power supply







#### Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP50P10D	TO-220-3L	AP50P10P XXX YYYY	1000

### Absolute Maximum Ratings (Tc=25°Cunless otherwise noted)

Parameter	Rating	Units
Drain-Source Voltage	-100	V
Gate-Source Voltage	±20	V
Continuous Drain Current, V <sub>GS</sub> @ -10V <sup>1</sup>	-50	А
Continuous Drain Current, $V_{GS}$ @ -10V <sup>1</sup>	-23	А
Pulsed Drain Current <sup>2</sup>	-100	А
Single Pulse Avalanche Energy <sup>3</sup>	345	mJ
Avalanche Current	28	А
Total Power Dissipation <sup>4</sup>	104	W
Storage Temperature Range -55 to 15		°C
Operating Junction Temperature Range	-55 to 150	°C
Thermal Resistance Junction-Ambient <sup>1</sup>	62	°C/W
Thermal Resistance Junction-Case <sup>1</sup>	1.2	°C/W
	Drain-Source Voltage   Gate-Source Voltage   Continuous Drain Current, V <sub>GS</sub> @ -10V <sup>1</sup> Continuous Drain Current, V <sub>GS</sub> @ -10V <sup>1</sup> Pulsed Drain Current <sup>2</sup> Single Pulse Avalanche Energy <sup>3</sup> Avalanche Current   Total Power Dissipation <sup>4</sup> Storage Temperature Range   Operating Junction Temperature Range   Thermal Resistance Junction-Ambient <sup>1</sup>	Drain-Source Voltage-100Gate-Source Voltage±20Continuous Drain Current, VGS @ -10V1-50Continuous Drain Current, VGS @ -10V1-23Pulsed Drain Current2-100Single Pulse Avalanche Energy3345Avalanche Current28Total Power Dissipation4104Storage Temperature Range-55 to 150Operating Junction Temperature Range-55 to 150Thermal Resistance Junction-Ambient 162



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## **Electrical Characteristics** (at $T_j=25$ °C unless otherwise specified )

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V , I <sub>D</sub> =-250uA	-100			V
		V <sub>GS</sub> =-10V , I <sub>D</sub> =-10A		42	50	
RDS(ON)	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =-4.5V , I <sub>D</sub> =-8A		46	55	${\tt m}\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}$ , $I_{D}$ =-250 $uA$	-1.2	-1.8	-2.5	V
IDSS	Drain-Source Leakage Current	$V_{DS}$ =-100V , $V_{GS}$ =0V , T <sub>J</sub> =25°C			-50	uA
lgss	Gate-Source Leakage Current	$V_{GS}=\pm20V$ , $V_{DS}=0V$			±100	nA
gfs	Forward Transconductance	V <sub>DS</sub> =-10V , I <sub>D</sub> =-10A		32		S
Qg	Total Gate Charge			92		
Qgs	Gate-Source Charge	V <sub>DS</sub> =-80V , V <sub>GS</sub> =-10V , I <sub>D</sub> =-14A		17.5		nC
Qgd	Gate-Drain Charge			14		
Td(on)	Turn-On Delay Time			20.5		ns
Tr	Rise Time	V <sub>DD</sub> =-50V , V <sub>GS</sub> =-10V ,		32.2		
Td(off)	Turn-Off Delay Time	R <sub>G</sub> =3.3 , I <sub>D</sub> =-14A		123		
T <sub>f</sub>	Fall Time	1D14A		63.7		
Ciss	Input Capacitance			6516		
Coss	Output Capacitance			223		pF
Crss	Reverse Transfer Capacitance			125		
ls	Continuous Source Current <sup>1,5</sup>	V <sub>G</sub> =V <sub>D</sub> =0V , Force Current			-35	А
Vsd	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V , I <sub>S</sub> =-1A , T <sub>J</sub> =25°C			1.2	V
trr	Reverse Recovery Time	IF=-14A , di/dt=-100A/µs ,		31.2		nS
Qrr	Reverse Recovery Charge	TJ=25°C		31.97		nC

Note :

1. The data tested by surface mounted on a 1 inch FR-4 board with 2OZ copper.

2.The data tested by pulsed , pulse width  $\leq$  300us , duty cycle  $\leq$  2%

3.The EAS data shows Max. rating . The test condition is V<sup>DD</sup>=-25V,V<sup>GS</sup>=-10V,L=0.88mH,I<sup>AS</sup>=-28A

4.The power dissipation is limited by 150°C junction temperature

5 .The data is theoretically the same as  $I_{\text{D}}$  and  $I_{\text{DM}}$  , in real applications , should be limited by total power dissipation.

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# **AP50P10**P

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### **Typical Characteristics**

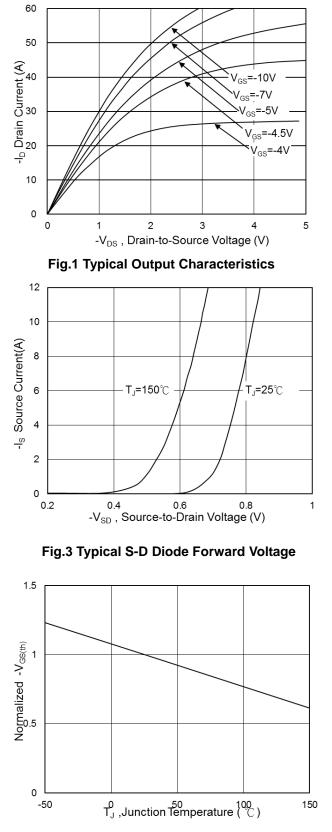


Fig.5 Normalized  $V_{GS(th)}$  vs.  $T_J$ 

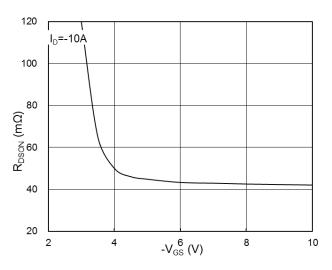


Fig.2 On-Resistance vs. G-S Voltage

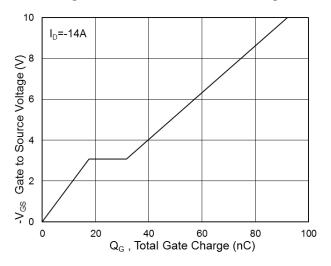
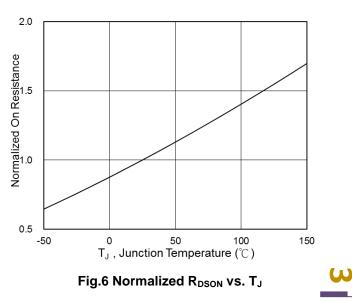


Fig.4 Gate-Charge Characteristics





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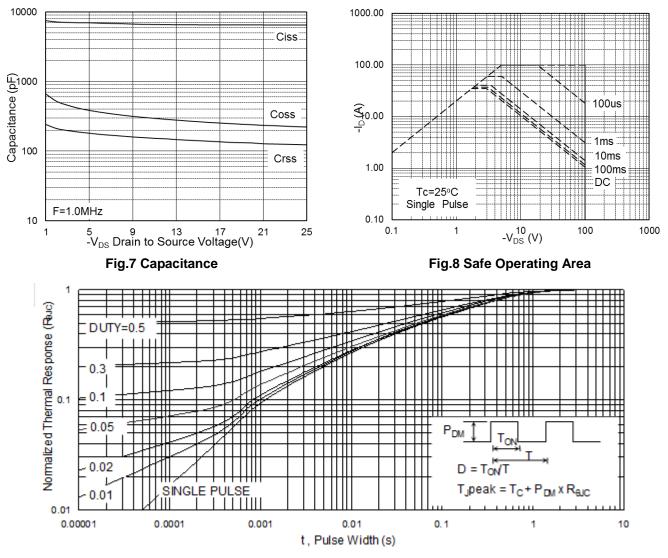


Fig.9 Normalized Maximum Transient Thermal Impedance

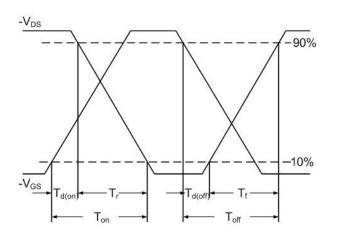
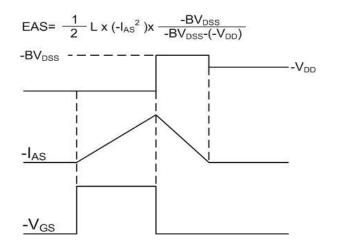


Fig.10 Switching Time Waveform

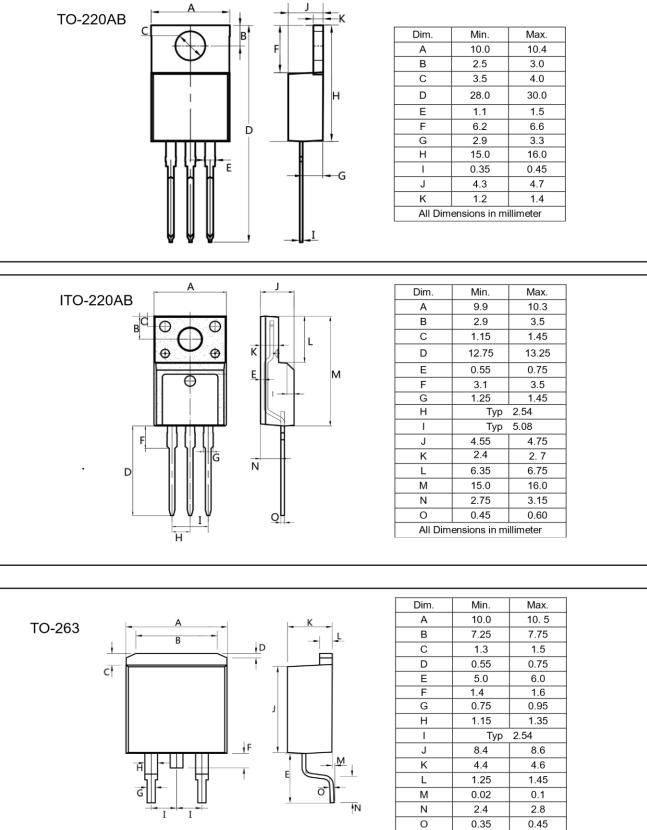


### Fig.11 Unclamped Inductive Waveform





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All Dimensions in millimeter

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