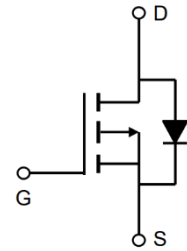


## -100V P-Channel Enhancement Mode MOSFET

### Description

The AP50P10NF uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.



### General Features

$V_{DS} = -100V$   $I_D = -50A$

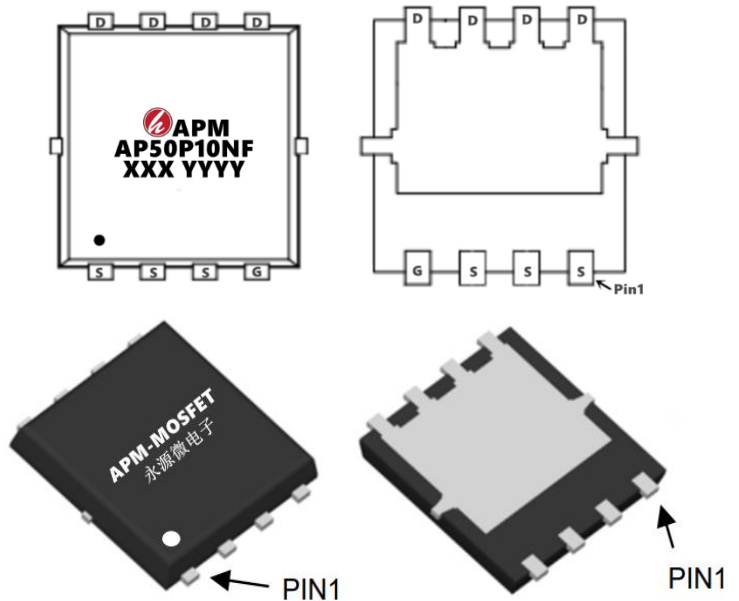
$R_{DS(ON)} < 52m\Omega$  @  $V_{GS}=10V$  (Type: 40m $\Omega$ )

### Application

Brushless motor

Load switch

Uninterruptible power supply



### Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP50P10NF	PDFN5*6-8L	AP50P10NF XXX YYYY	5000

### Absolute Maximum Ratings ( $T_C=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	-100	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D@T_C=25^\circ C$	Continuous Drain Current, $V_{GS}$ @ -10V <sup>1</sup>	-50	A
$I_D@T_C=100^\circ C$	Continuous Drain Current, $V_{GS}$ @ -10V <sup>1</sup>	-28	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	-150	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	87	mJ
$I_{AS}$	Avalanche Current	-35	A
$P_D@T_C=25^\circ C$	Total Power Dissipation <sup>4</sup>	140	W
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ C$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup>	25	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case <sup>1</sup>	1.1	$^\circ C/W$

## -100V P-Channel Enhancement Mode MOSFET

### P-Channel Electrical Characteristics (T<sub>J</sub> =25 °C, unless otherwise noted)

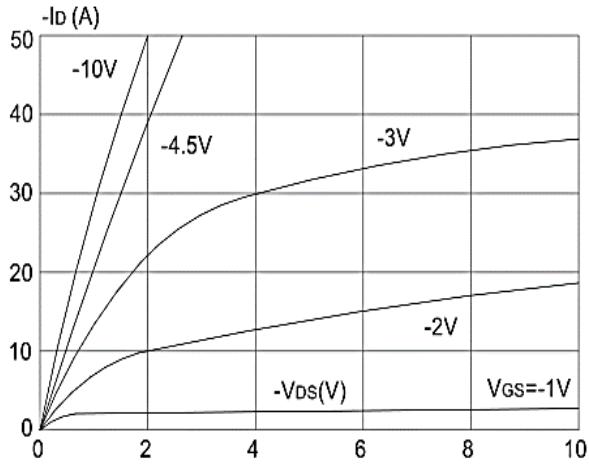
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V(BR)DSS	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =-250μA	-100	-	-	V
IDSS	Zero Gate Voltage Drain Current	V <sub>DS</sub> =-100V, V <sub>GS</sub> =0V,	-	-	-1.0	μA
IGSS	Gate to Body Leakage Current	V <sub>DS</sub> =0V, V <sub>GS</sub> = ±20V	-	-	±100	nA
VGS(th)	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250μA	-1.0	-1.6	-2.5	V
RDS(on)	Static Drain-Source on-Resistance	V <sub>GS</sub> =-10V, I <sub>D</sub> =-20A	-	40	52	mΩ
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-10A	-	44	62	
Ciss	Input Capacitance	V <sub>DS</sub> =-50V, V <sub>GS</sub> =0V, f=1.0MHz	-	2120	-	pF
Coss	Output Capacitance		-	194	-	pF
Crss	Reverse Transfer Capacitance		-	13	-	pF
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =-50V, I <sub>D</sub> =-5A, V <sub>GS</sub> =-10V	-	40	-	nC
Q <sub>gs</sub>	Gate-Source Charge		-	7.8	-	nC
Q <sub>gd</sub>	Gate-Drain("Miller") Charge		-	8.6	-	nC
td(on)	Turn-on Delay Time	V <sub>DD</sub> =-50V, I <sub>D</sub> =-5A, R <sub>G</sub> =6Ω, V <sub>GS</sub> =-10V	-	13	-	ns
t <sub>r</sub>	Turn-on Rise Time		-	39	-	ns
td(off)	Turn-off Delay Time		-	100.1	-	ns
t <sub>f</sub>	Turn-off Fall Time		-	105.3	-	ns
IS	Maximum Continuous Drain to Source Diode Forward Current		-	-	-35	A
ISM	Maximum Pulsed Drain to Source Diode Forward Current		-	-	-140	A
VSD	Drain to Source Diode Forward Voltage	V <sub>GS</sub> =0V, I <sub>S</sub> =-30A	-	-	-1.2	V
t <sub>rr</sub>	Body Diode Reverse Recovery Time	T <sub>J</sub> =25°C, I <sub>F</sub> =-5A, dI/dt=100A/μs	-	104	-	ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge		-	280	-	nC

Note :

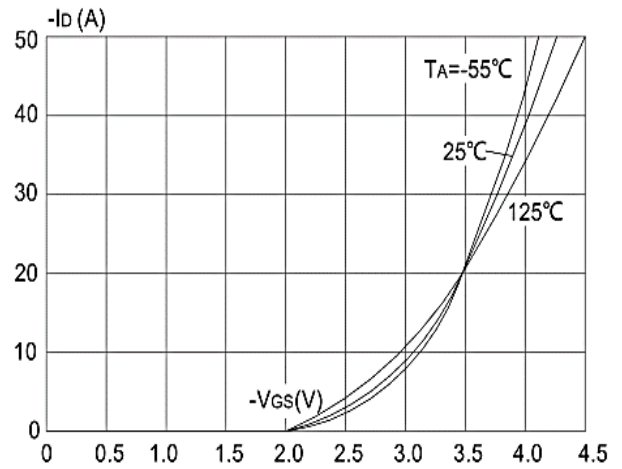
- 1、 The data tested by surface mounted on a 1 inch 2 FR-4 board with 2OZ copper.
- 2、 The data tested by pulsed , pulse width ≅ 300us , duty cycle ≅ 2%
- 3、 The EAS data shows Max. rating . The test condition is V DD =-25V, V GS =-10V, L=0.1mH, IAS =-24A
- 4、 The power dissipation is limited by 150 °C junction temperature
- 5、 The data is theoretically the same as I D and I DM , in real applications , should be limited by total power dissipation.

**-100V P-Channel Enhancement Mode MOSFET**

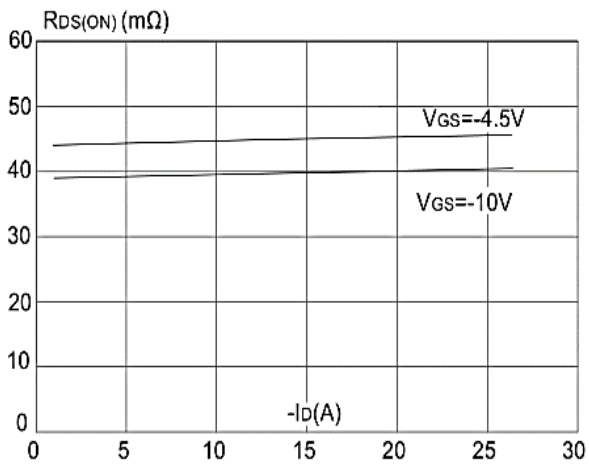
**Typical Characteristics**



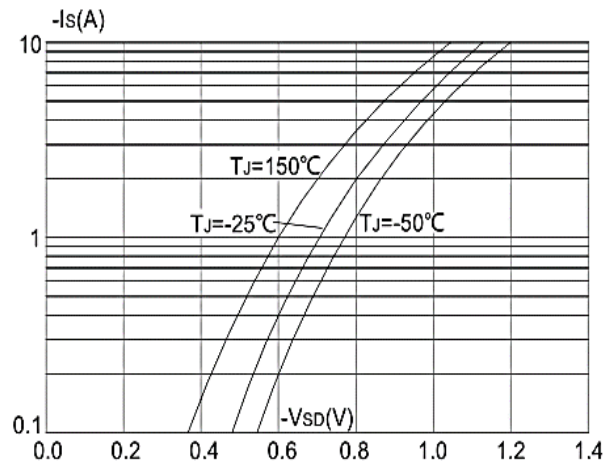
**Figure 1: Output Characteristics**



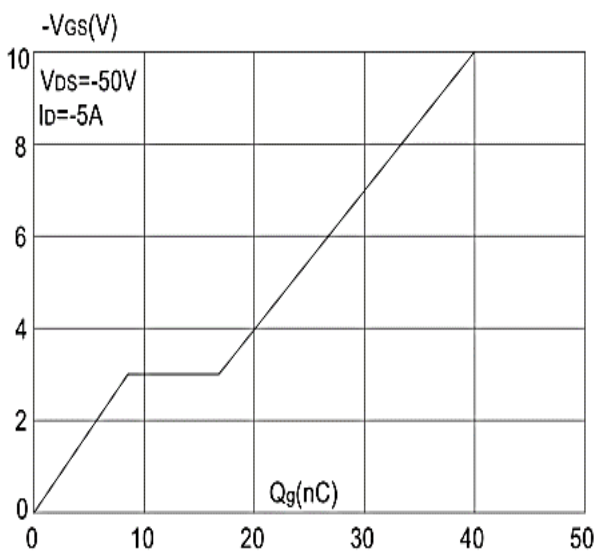
**Figure 2: Typical Transfer Characteristics**



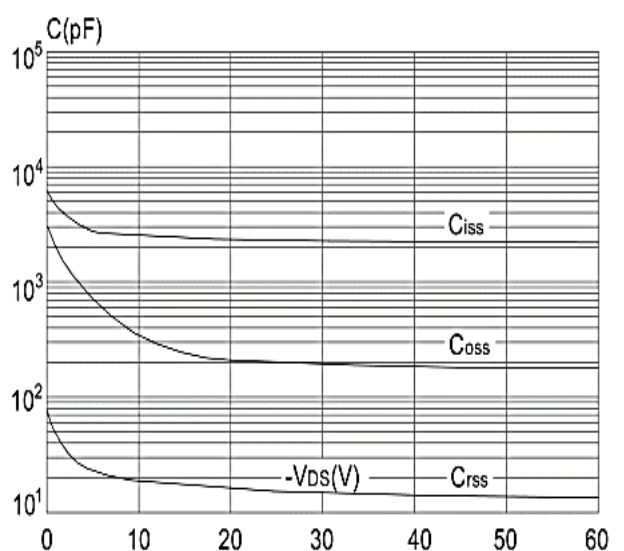
**Figure 3: On-resistance vs. Drain Current**



**Figure 4: Body Diode Characteristics**

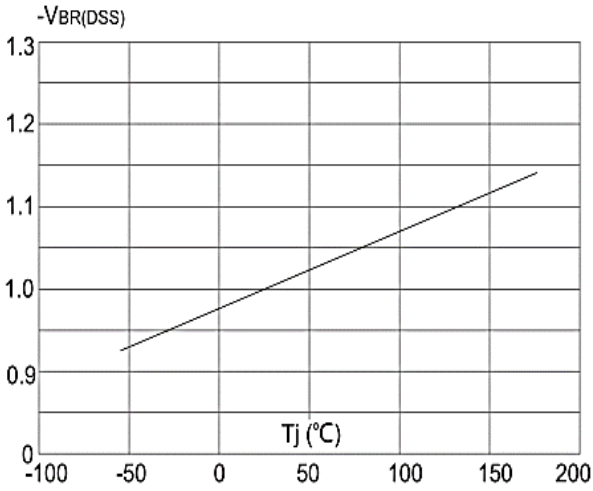


**Figure 5: Gate Charge Characteristics**

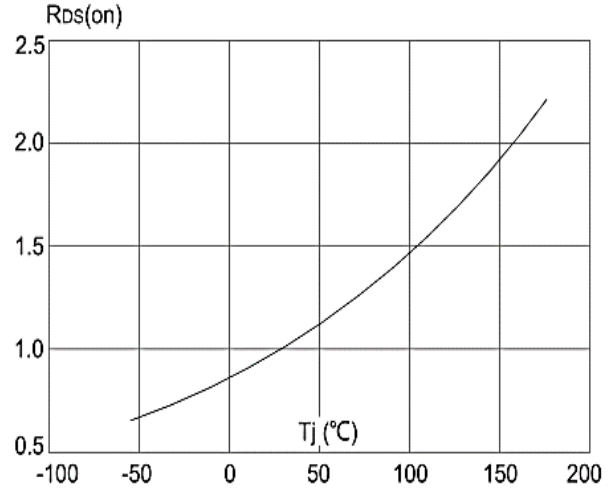


**Figure 6: Capacitance Characteristics**

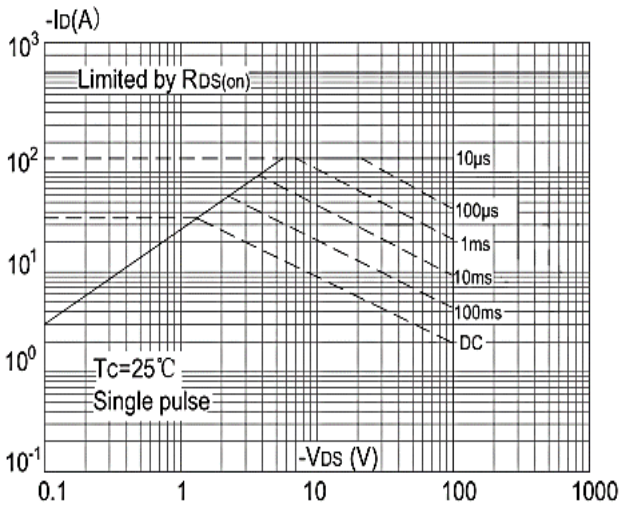
**-100V P-Channel Enhancement Mode MOSFET**



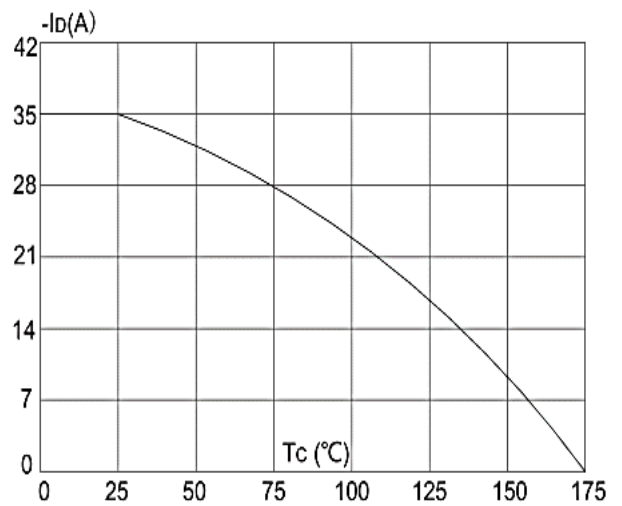
**Figure 7: Normalized Breakdown Voltage vs Junction Temperature**



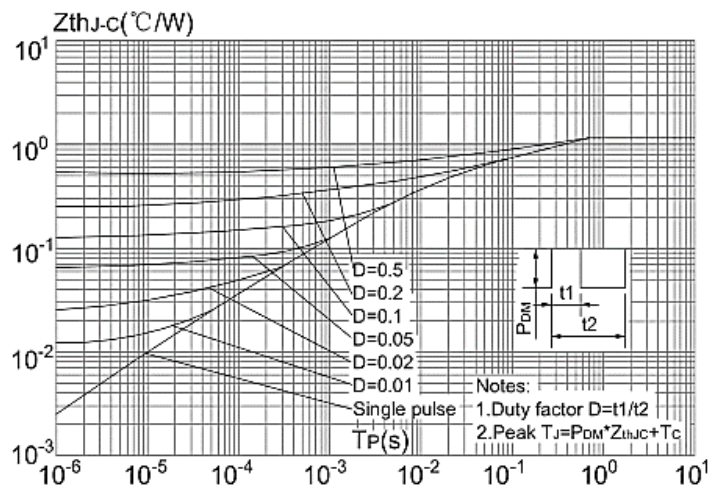
**Figure 8: Normalized on Resistance vs. Junction Temperature**



**Figure 9: Maximum Safe Operating Area**

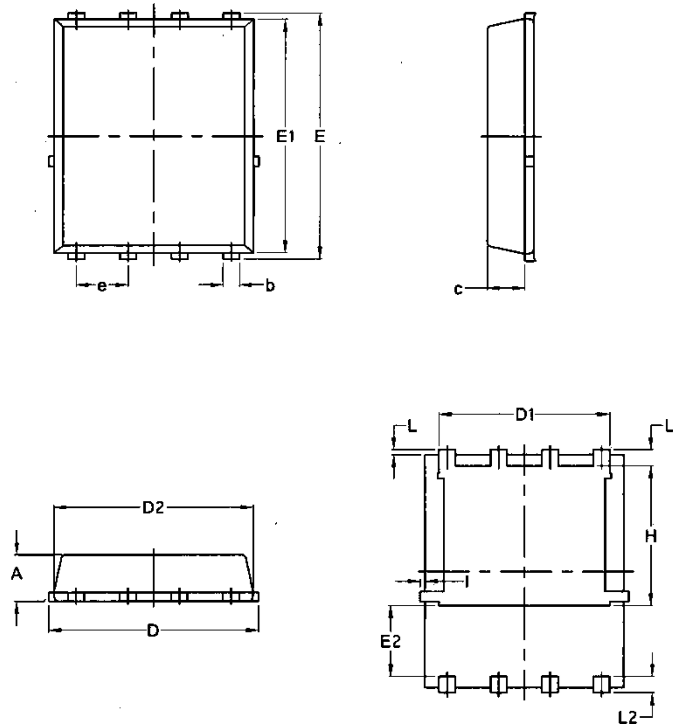


**Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature**



**Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Ambien**

### Package Mechanical Data-DFN5\*6-8L-JQ Single



Symbol	Common			
	mm		Inch	
	Min	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070

**-100V P-Channel Enhancement Mode MOSFET****Attention**

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**-100V P-Channel Enhancement Mode MOSFET**

<b>Edition</b>	<b>Date</b>	<b>Change</b>
Rve1.0	2021/4/13	Initial release

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