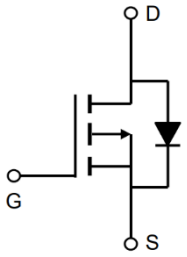
AP50P02DF

-20V P-Channel Enhancement Mode MOSFET

Description

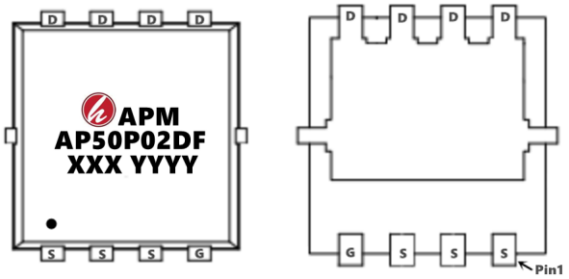
The AP50P02DF uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.



General Features

V_{DS} = -20V I_D =-50A

$R_{DS(ON)}$ < 9mΩ @ V_{GS}=-4.5V (Type: 6.8mΩ)



Application

Battery protection

Load switch

Uninterruptible power supply

Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP50P02DF	PDFN3*3-8L	AP50P02DF XXX YYYY	5000

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Symbol	Parameter	Rating	Units
VDS	Drain-Source Voltage	-20	V
VGS	Gate-Source Voltage	±12	V
I_D@T_C=25℃	Continuous Drain Current, V_{GS} @ -4.5V[1]	-50	A
I_D@T_C=70℃	Continuous Drain Current, V_{GS} @ -4.5V[1]	-18	A
IDM	Pulsed Drain Current[2]	-100	A
P_D@T_C=25℃	Total Power Dissipation[3]	29	W
P_D@T_C=70℃	Total Power Dissipation[3]	19	W
TSTG	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃
$R_{\theta}JA$	Thermal Resistance Junction-Ambient [1]	75	℃/W
$R_{\theta}JA$	Thermal Resistance Junction-Ambient [1] (t ≤10s)	40	℃/W
$R_{\theta}JC$	Thermal Resistance Junction-Case[1]	4.2	℃/W

Electrical Characteristics (T_J=25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=-250uA	-20	-22	---	V
△BVDSS/△TJ	BV_{DSS} Temperature Coefficient	Reference to 25℃ , I_D=-1mA	---	-0.012	---	V/℃
RDS(ON)	Static Drain-Source On-Resistance[2]	V_{GS}=-4.5V , I_D=-15A	---	6.8	9	mΩ
RDS(ON)	Static Drain-Source On-Resistance[2]	V_{GS}=-2.5V , I_D=-10A	---	8.2	11	
VGS(th)	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =-250uA	-0.3	0.6	-1.0	V
△$V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	2.94	---	mV/℃
IDSS	Drain-Source Leakage Current	V_{DS}=-20V , V_{GS}=0V , T_J=25℃	---	---	1	uA
IGSS	Gate-Source Leakage Current	V_{GS}=±12V , V_{DS}=0V	---	---	±100	nA
gfs	Forward Transconductance	V_{DS}=-5V , I_D=-10A	---	43	---	S
Q_g	Total Gate Charge (-4.5V)	V_{DS}=-15V , V_{GS}=-4.5V , I_D=-10A	---	63	---	nC
Qgs	Gate-Source Charge		---	9.1	---	
Qgd	Gate-Drain Charge		---	13	---	
Td(on)	Turn-On Delay Time	V_{DD}=-10V , V_{GS}=-4.5V , R_G=3.3Ω, I_D=-10A	---	15.8	---	ns
T_r	Rise Time		---	76.8	---	
Td(off)	Turn-Off Delay Time		---	193	---	
T_f	Fall Time		---	186.4	---	
Ciss	Input Capacitance	V_{DS}=-15V , V_{GS}=0V , f=1MHz	---	5783	---	pF
Coss	Output Capacitance		---	509	---	
Crss	Reverse Transfer Capacitance		---	431	---	
IS	Continuous Source Current[1,4]	V_G=V_D=0V , Force Current	---	---	-10.7	A
ISM	Pulsed Source Current[2,4]		---	---	-60	A
VSD	Diode Forward Voltage[2]	V_{GS}=0V , I_S=-1A , T_J=25℃	---	---	-1.2	V
trr	Reverse Recovery Time	IF=-10A , dI/dt=100A/μs , T_J =25℃	---	27	---	nS
Q_{rr}	Reverse Recovery Charge		---	17.8	---	nC

Note :

1、The data tested by surface mounted on a 1 inch 2 FR-4 board with 2OZ copper.

2、The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%

3、The power dissipation is limited by 150℃ junction temperature

4、The data is theoretically the same as I D and I DM , in real applications , should be limited by total power dissipation.

Typical Characteristics

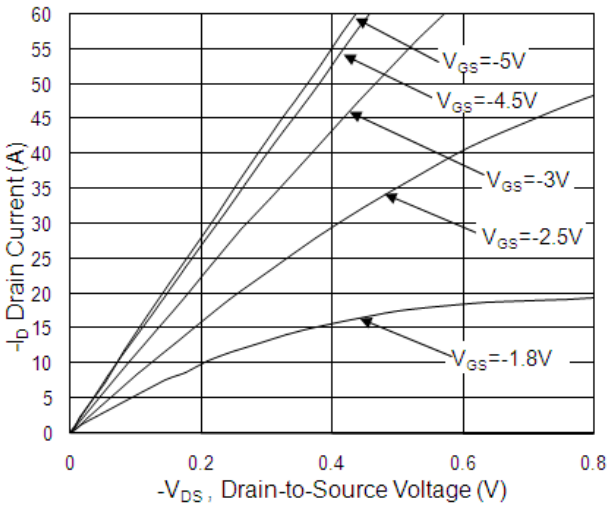


Fig.1 Typical Output Characteristics

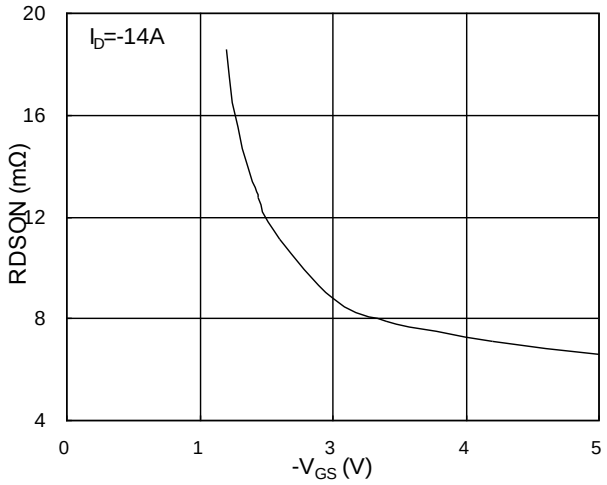


Fig.2 On-Resistance vs. G-S Voltage

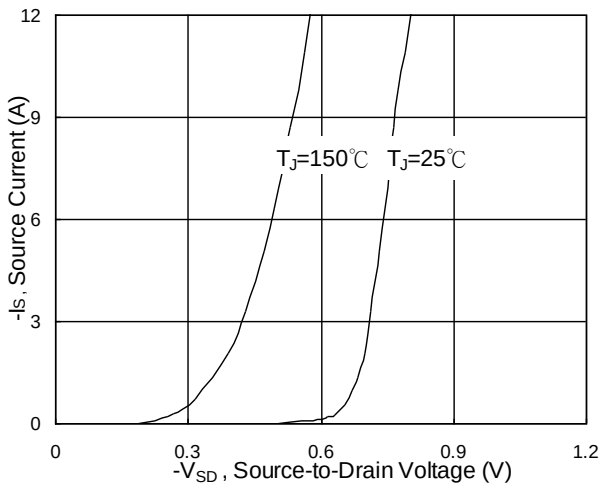


Fig.3 Forward Characteristics of Reverse

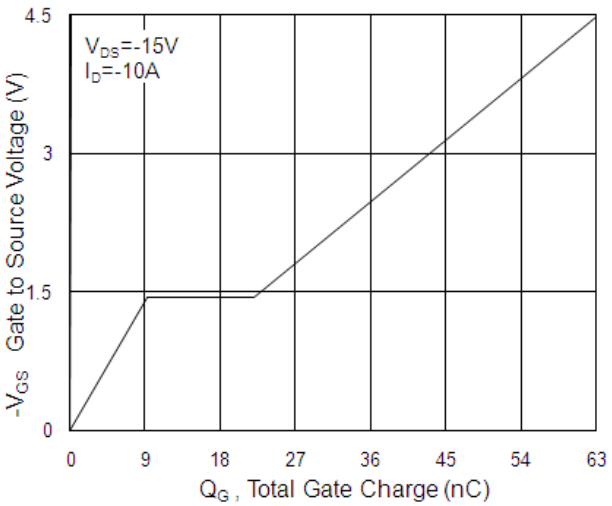


Fig.4 Gate-charge Characteristics

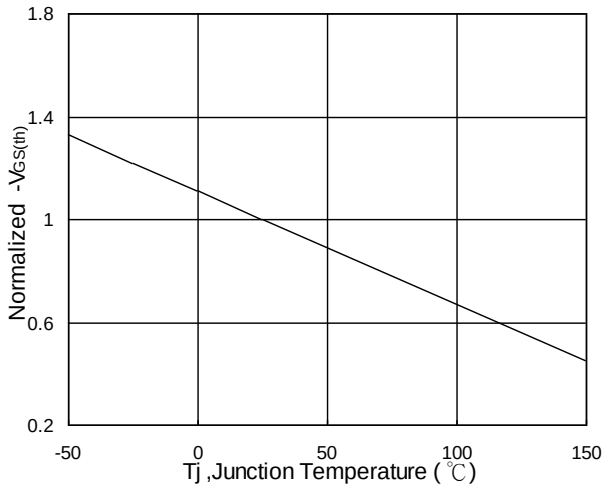


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

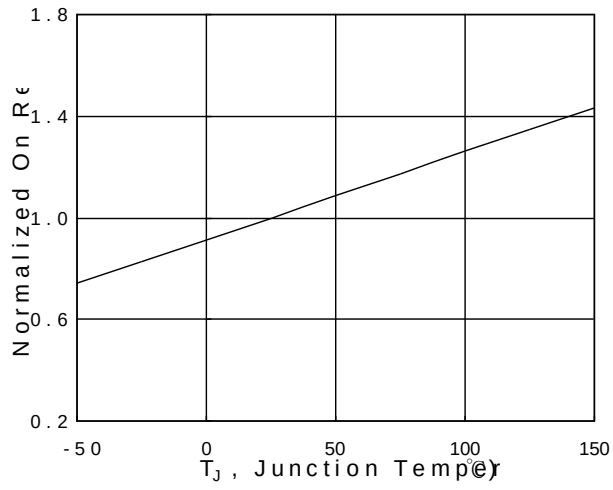


Fig.6 Normalized R_{DSON} vs. T_J

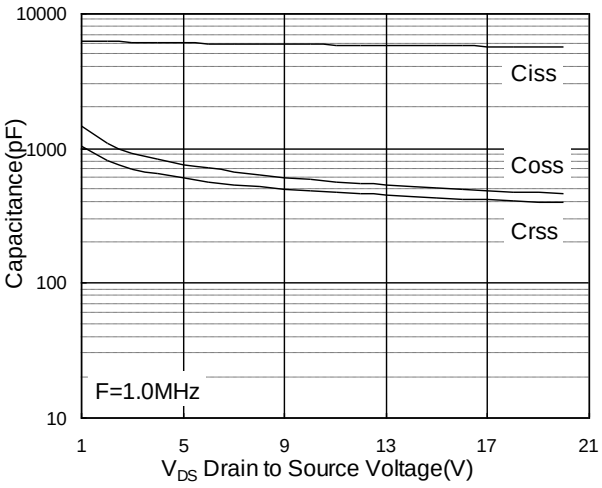


Fig.7 Capacitance

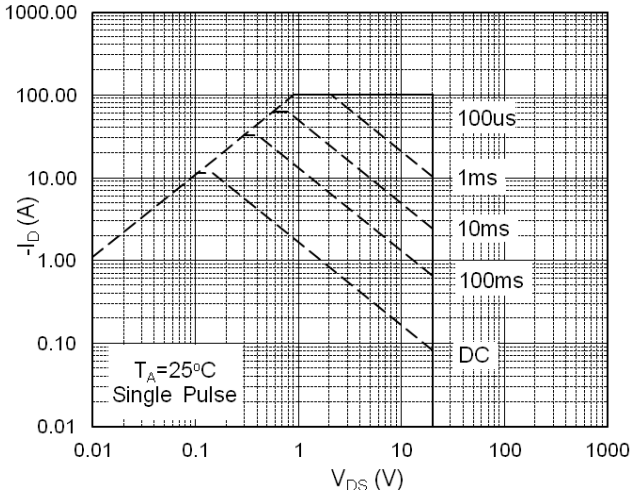


Fig.8 Safe Operating Area

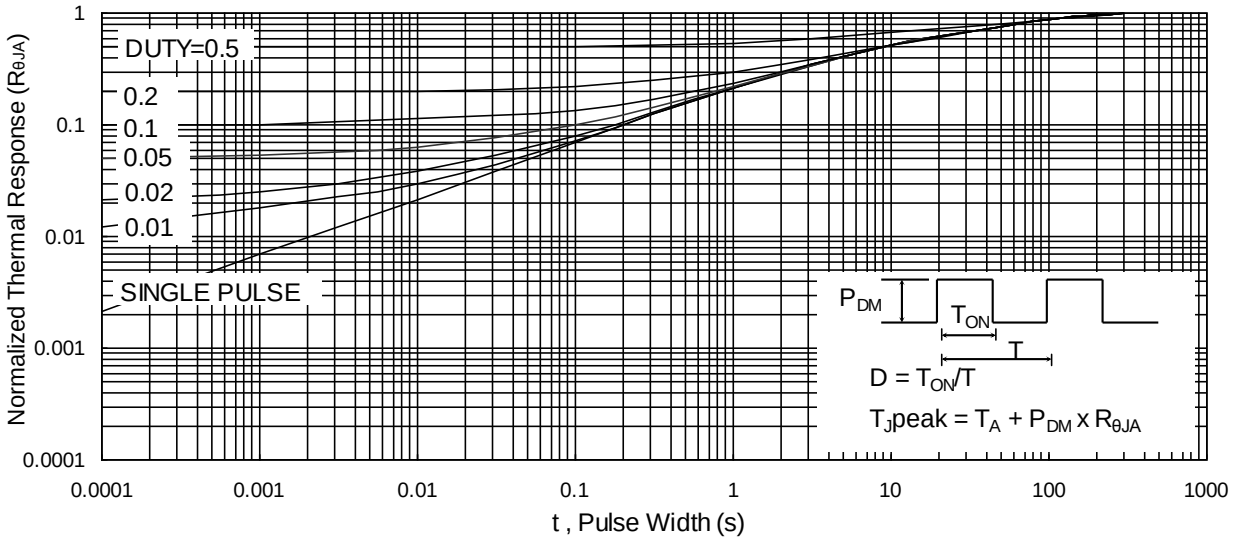


Fig.9 Normalized Maximum Transient Thermal Impedance

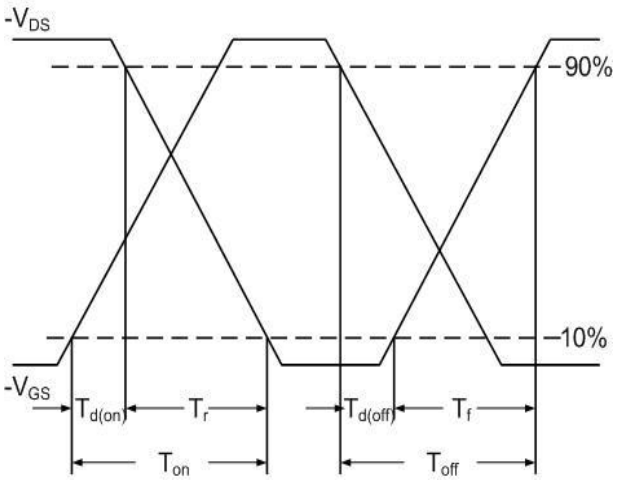


Fig.10 Switching Time Waveform

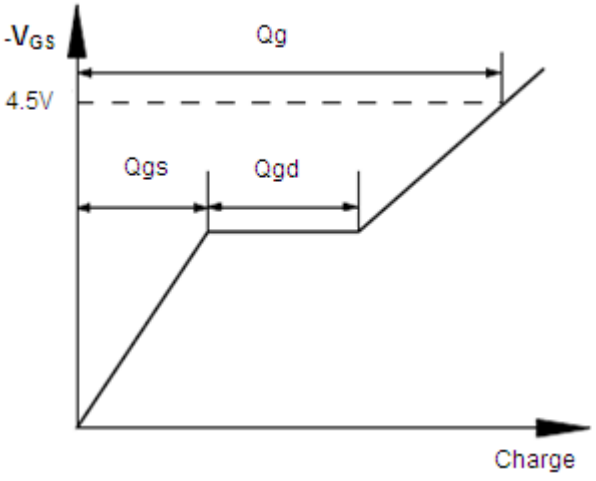
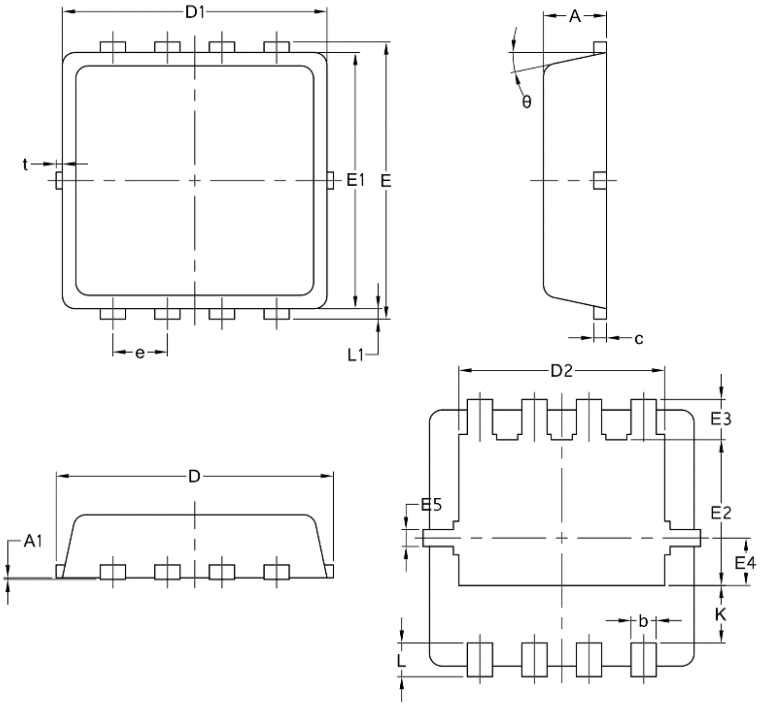


Fig.11 Gate Charge Waveform

Package Mechanical Data-DFN3*3-8L-JQ Single



Symbol	Common		
	mm		
	Mim	Nom	Max
A	0.70	0.75	0.85
A1	/	/	0.05
b	0.20	0.30	0.40
c	0.10	0.152	0.25
D	3.15	3.30	3.45
D1	3.00	3.15	3.25
D2	2.29	2.45	2.65
E	3.15	3.30	3.45
E1	2.90	3.05	3.20
E2	1.54	1.74	1.94
E3	0.28	0.48	0.65
E4	0.37	0.57	0.77
E5	0.10	0.20	0.30
e	0.60	0.65	0.70
K	0.59	0.69	0.89
L	0.30	0.40	0.50
L1	0.06	0.125	0.20
t	0	0.075	0.13
Φ	10	12	14

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-20V P-Channel Enhancement Mode MOSFET

Edition	Date	Change
Rve1.0	2018/1/31	Initial release