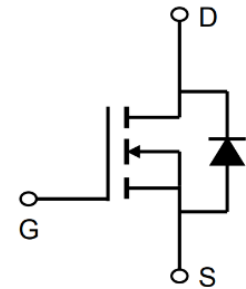


200V N-Channel Enhancement Mode MOSFET

Description

The AP50N20MP is silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency.



General Features

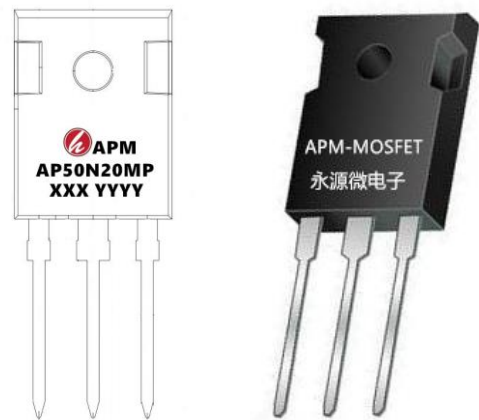
$V_{DS} = 200V, I_D = 50A$

$R_{DS(ON)} < 60m\Omega @ V_{GS} = 10V$

Application

Power amplifier

motor drive



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP50N20MP	TO-247-3L	AP50N20MP XXX YYYY	600

Absolute Maximum Ratings $T_C = 25^\circ C$, unless otherwise noted

Symbol	Parameter	Rating	Units
VDSS	Drain-Source Voltage	200	V
ID	Continuous Drain Current	50	A
IDM	Pulsed Drain Current	160	A
VGSS	Gate-Source Voltage	± 20	V
EAS	Single Pulse Avalanche Energy	191	mJ
IAS	Avalanche Current	31	A
EAR	Repetitive Avalanche Energy	124	mJ
PD	Power Dissipation ($T_C = 25^\circ C$)	104	W
TJ, Tstg	Operating Junction and Storage Temperature Range	-55~+150	$^\circ C$
RthJC	Thermal Resistance, Junction-to-Case	1.2	$^\circ C/W$
RthJA	Thermal Resistance, Junction-to-Ambient	60	$^\circ C/W$

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Electrical Characteristics at $T_j=25\text{ }^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	200	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 200V, V_{GS} = 0V, T_J = 25^\circ C$	--	--	1	μA
I_{DSS}		$V_{DS} = 200V, V_{GS} = 0V, T_J = 125^\circ C$	--	--	100	
I_{GSS}	Gate-Source Leakage	$V_{GS} = \pm 20V, V_{DS} = 0V$	--	--	± 100	nA
$V_{GS(th)}$	Gate-Source Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	2.0	--	4.0	V
$R_{DS(on)}$	Drain-Source On-Resistance (Note4)	$V_{GS} = 10V, I_D = 20A$	--	50	60	m Ω
gfs	Forward Transconductance (Note4)	$V_{DS} = 25V, I_D = 20A$	--	16	--	S
C_{iss}	Input Capacitance	$V_{GS} = 0V,$ $V_{DS} = 25V, f = 1.0MHz$	--	2800	--	μF
C_{oss}	Output Capacitance		--	355	--	
C_{rss}	Reverse Transfer Capacitance		--	101	--	
Q_g	Total Gate Charge	$V_{DD} = 160V, I_D = 40A,$	--	154	--	nC
Q_{gs}	Gate-Source Charge		--	13	--	
Q_{gd}	Gate-Drain Charge		--	58	--	
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 160V, I_D = 40A,$ $V_{GS} = 15V, R_G = 25\Omega$	--	46	--	ns
t_r	Turn-on Rise Time		--	54	--	
$t_{d(off)}$	Turn-off Delay Time		--	360	--	
t_f	Turn-off Fall Time		--	96	--	
I_{SD}	Continuous Source Current	Integral PN-diode in MOSFET	--	--	40	A
I_{SM}	Pulsed Source Current		--	--	160	
V_{SD}	Body Forward Voltage	$I_S = 20A, V_{GS} = 0V$	--	--	1.4	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0V, I_F = 10A,$ $di_F/dt = 100A/\mu s$	--	152	--	ns
Q_{rr}	Reverse Recovery Charge		--	1	--	μC

Notes:

- 1、Repetitive Rating: Pulse width limited by maximum junction temperature
- 2、L = 1mH, $V_{DD} = 30V$, $R_G = 25\ \Omega$, Starting $T_J = 25\text{ }^\circ\text{C}$
- 3、Pulse Test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 1\%$

200V N-Channel Enhancement Mode MOSFET

Electrical Characteristics Diagrams

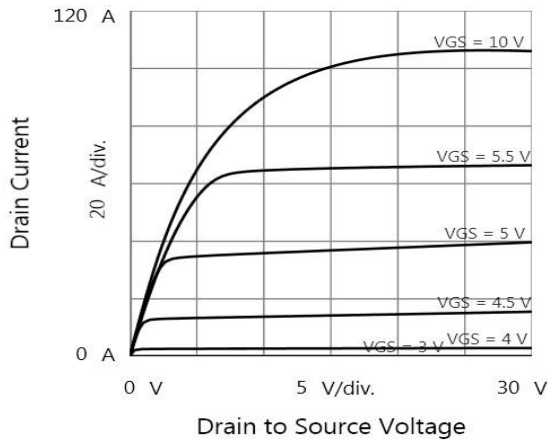


Figure 1. Output Characteristics ($T_J = 25^\circ\text{C}$)

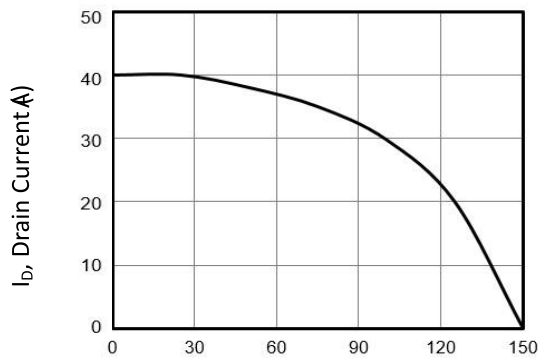


Figure 5. Drain to Source Voltage vs. Gate to Source Voltage

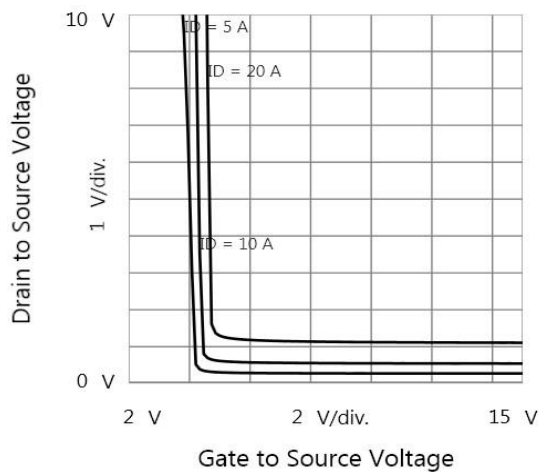


Figure 6. Body Diode Forward Characteristics

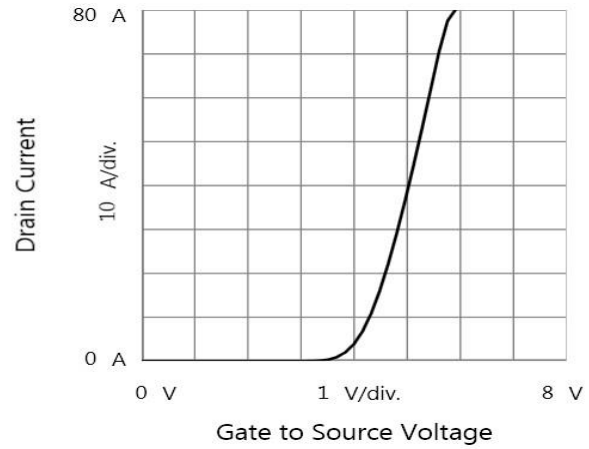
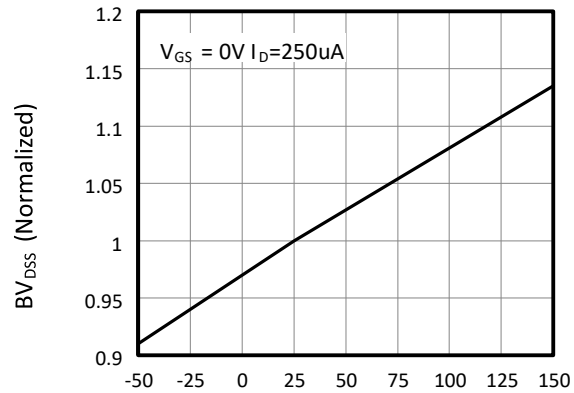


Figure 2. Transfer Characteristics



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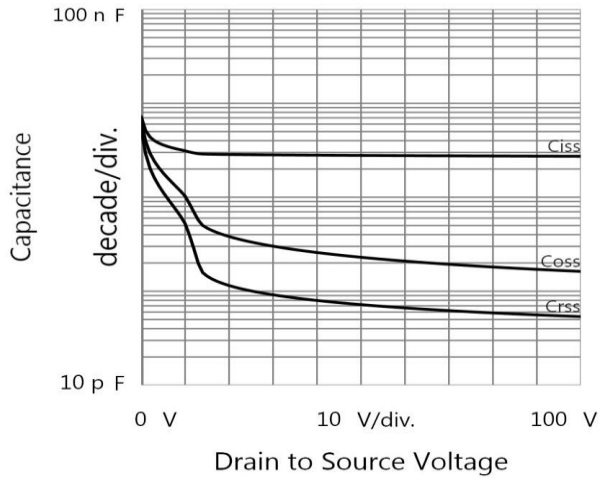


Figure 7. Capacitance

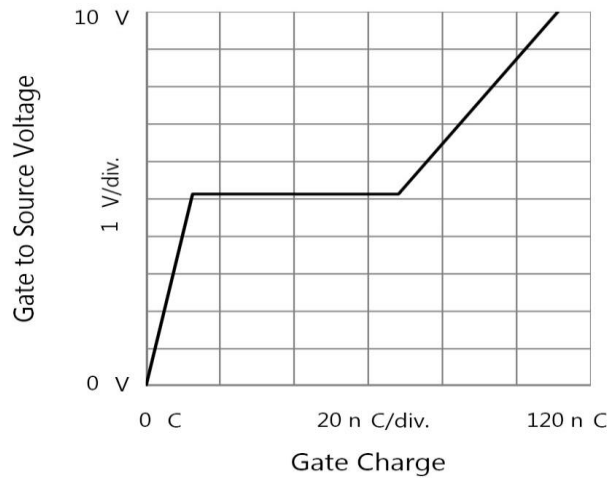


Figure 8. Gate Charge

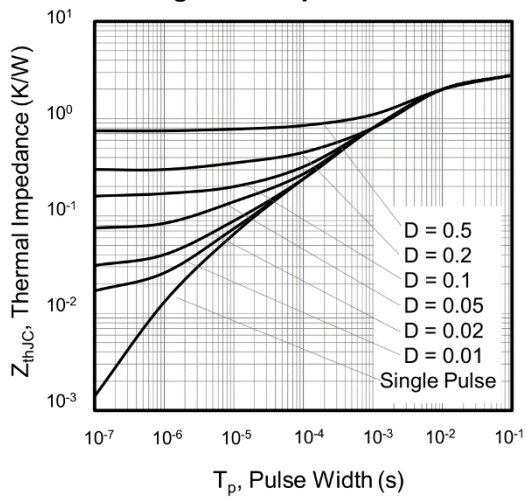
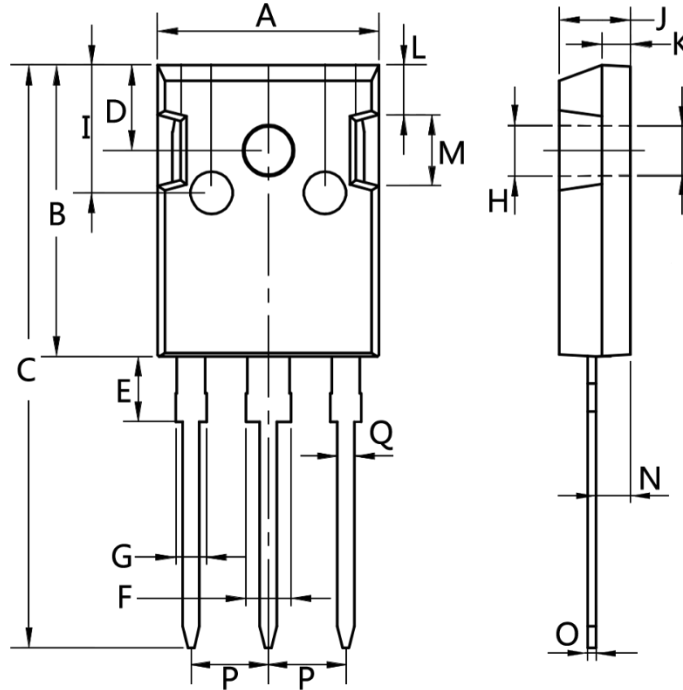


Figure 9. Transient Thermal Impedance

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Package Mechanical Data-TO-247-LX



Dim.	Min.	Max.
A	15.0	16.0
B	20.0	21.0
C	41.0	42.0
D	5.0	6.0
E	4.0	5.0
F	2.5	3.5
G	1.75	2.5
H	3.0	3.5
I	8.0	10.0
J	4.9	5.1
K	1.9	2.1
L	3.5	4.0
M	4.75	5.25
N	2.0	3.0
O	0.55	0.75
P	Typ 5.08	
Q	1.2	1.3

200V N-Channel Enhancement Mode MOSFET**Attention**

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AP50N20MP

200V N-Channel Enhancement Mode MOSFET

Edition	Date	Change
Rve1.0	2019/4/31	Initial release

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