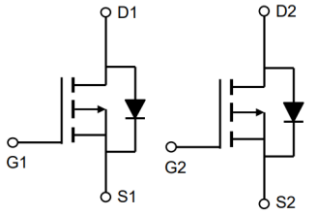
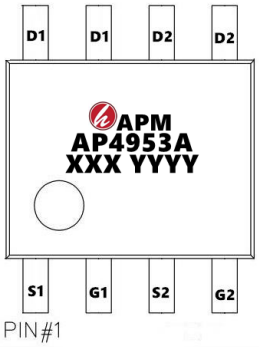
AP4953A

-30V P+P-Channel Enhancement Mode MOSFET

Description

The AP4953A uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.





General Features

V_{DS} = -30V I_D =-7A

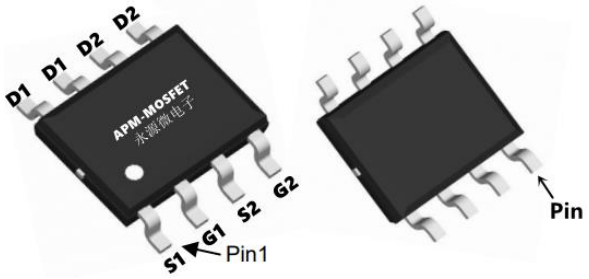
$R_{DS(ON)}$ < 48mΩ @ V_{GS}=10V （**Type：37mΩ**）

Application

Lithium battery protection

Wireless impact

Mobile phone fast charging



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP4953A	SOP-8	AP4953A XXX YYYY	3000

Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-30	V
V_{GS}	Gate-Source Voltage	±20	V
I_D@T_A=25℃	Continuous Drain Current, -V_{GS} @ -10V[1]	-7	A
I_D@T_A=70℃	Continuous Drain Current, -V_{GS} @ -10V[1]	-4.3	A
I_{DM}	Pulsed Drain Current[2]	-21	A
EAS	Single Pulse Avalanche Energy[3]	81.2	mJ
P_D@T_A=25℃	Total Power Dissipation[4]	1.5	W
T_{STG}	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃
$R_{\theta JA}$	Thermal Resistance Junction-Ambient [1]	85	℃/W
$R_{\theta JC}$	Thermal Resistance Junction-Case[1]	25	℃/W

Electrical Characteristics (T_J=25 ℃, unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V(BR)DSS	Drain-Source Breakdown Voltage	V_{GS}= 0V, I_D= -250μA	-30	-33	-	V
IDSS	Zero Gate Voltage Drain Current	V_{DS}= -30V, V_{GS}= 0V	-	-	-1	μA
IGSS	Gate-Source Leakage	V_{DS}= 0V, V_{GS}= ±20V	-	-	±100	nA
VGS(th)	Gate-Source Threshold Voltage[3]	V_{DS}= V_{GS}, I_D= -250μA	-1	-1.6	-2.5	V
RDS(on)	Drain-Source on-State Resistance[3]	V_{GS}= -10V, I_D= -4.1A	-	37	48	mΩ
		V_{GS}= -4.5V, I_D= -3.0A	-	58	65	
Ciss	Input Capacitance	V_{GS} = 0V , V_{DS} = -15V, f= 1.0MHz	-	530	-	pF
Coss	Output Capacitance		-	70	-	
Crss	Reverse Transfer Capacitance		-	56	-	
td(on)	Turn-on Delay Time[4]	V_{GS}= -10V, V_{DS}= -15V , R_L= 15Ω,R_{GEN}= 2.5Ω	-	14	-	nS
tr	Rise Time[4]		-	61	-	
td(off)	Turn-off Delay Time[4]		-	19	-	
tf	Fall Time[4]		-	10	-	
Q_g	Total Gate Charge[4]	V_{GS} = -10V, V_{DS} = -15V, I_D = -4.1A	-	6.8	-	nC
Qgs	Gate−Source Charge[4]		-	1.0	-	
Qgd	Gate−Drain Charge[4]		-	1.4	-	
VSD	Diode Forward Voltage	I_S = -4.1A, V_{GS} = 0V	-	-	-1.2	V

Note :

1、The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper.

2、The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%

3、The power dissipation is limited by 150℃ junction temperature

4、The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

Typical Characteristics

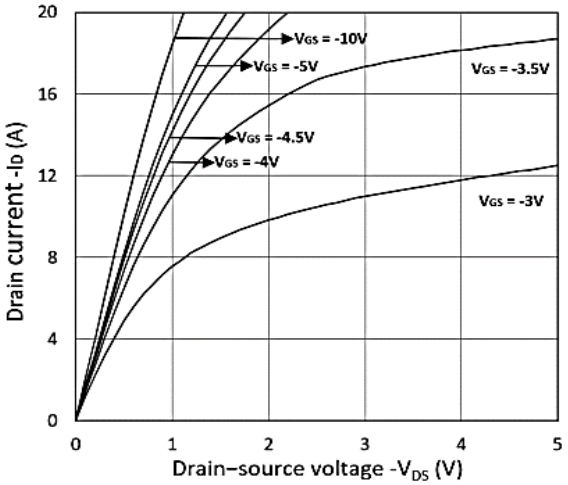


Figure 1. Output Characteristics

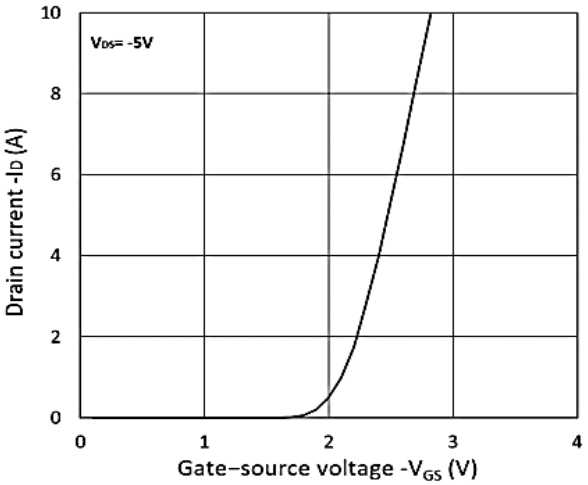


Figure 2. Transfer Characteristics

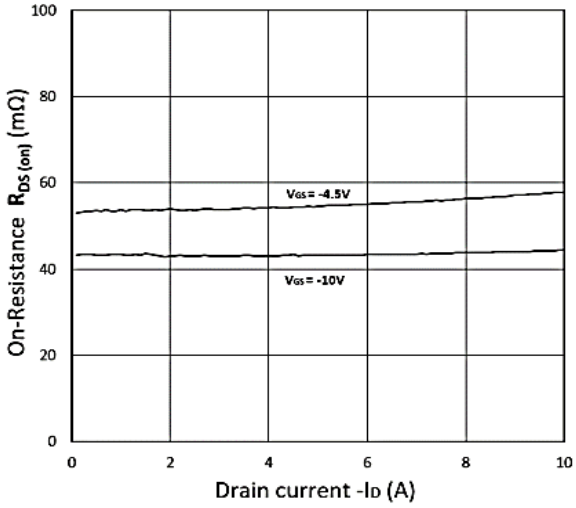


Figure 3. RDS(ON) vs. ID

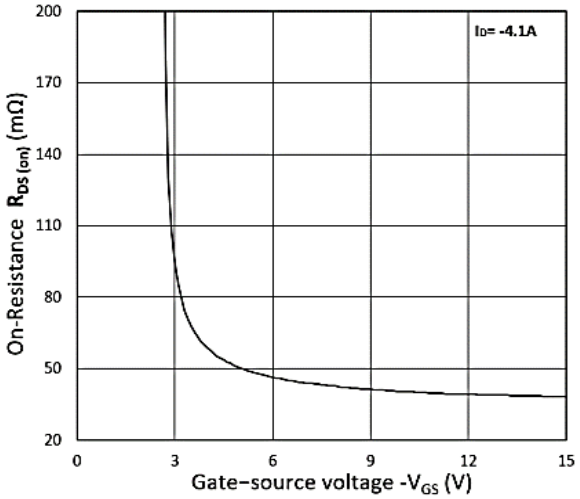


Figure 4. R DS(ON) vs. V GS

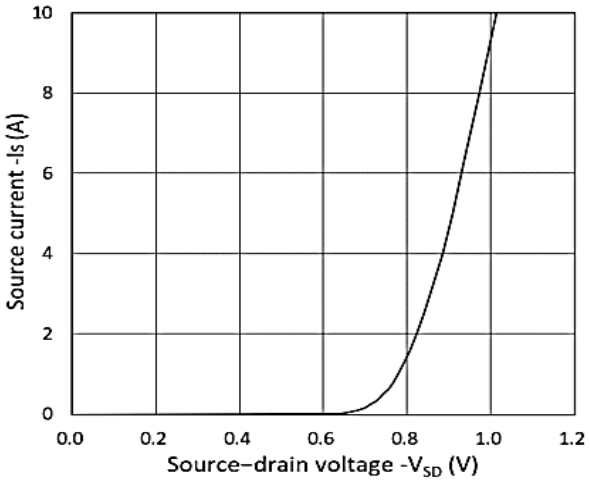


Figure 5.IS vs. VSD

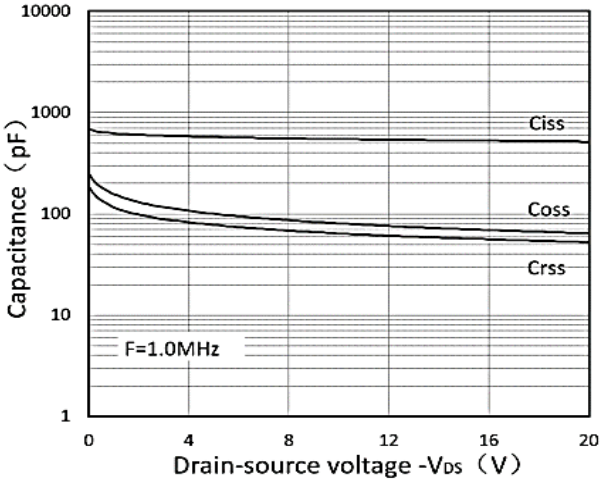


Figure 6. Capacitance Characteristics

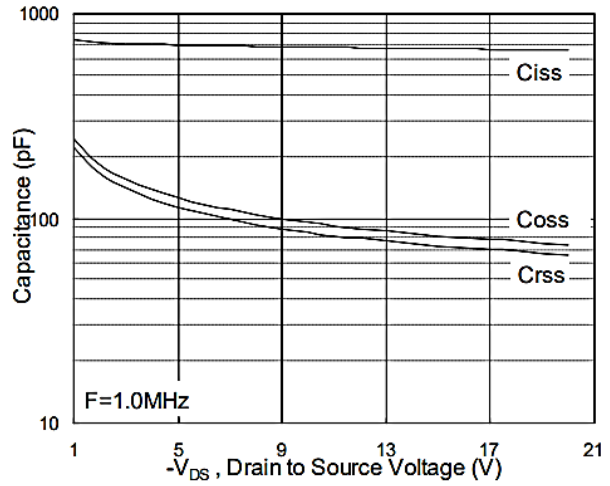


Figure 7 Capacitance

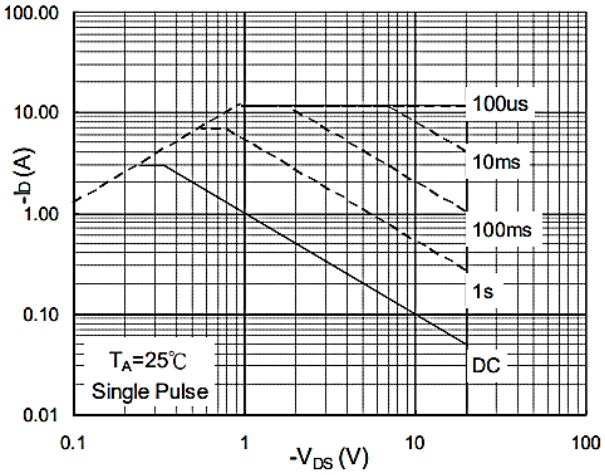


Figure 8 Safe Operating Area

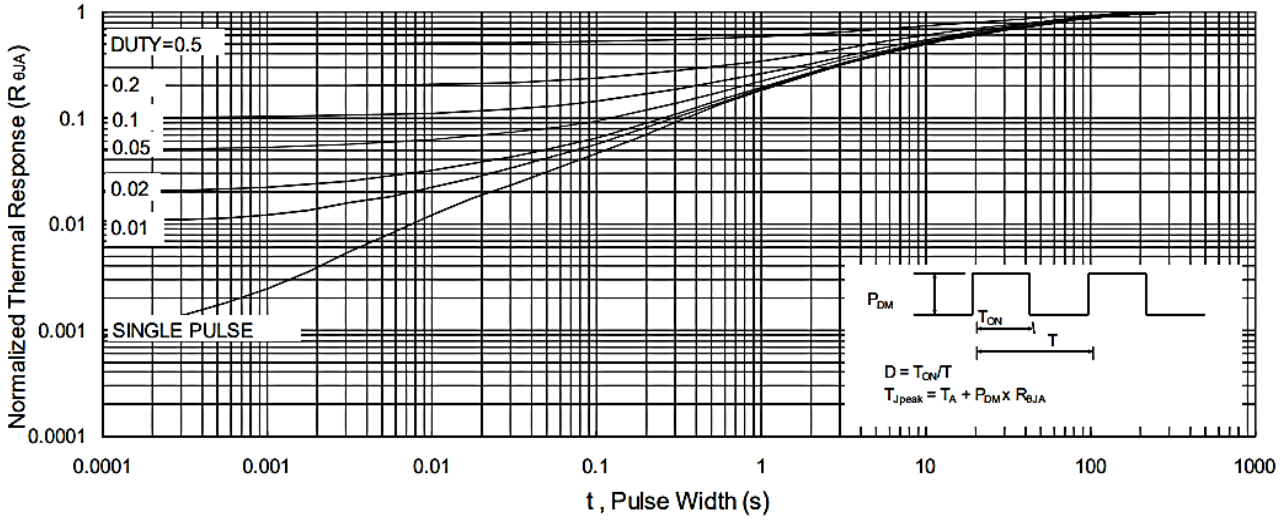


Figure 9 Normalized Maximum Transient Thermal Impedance

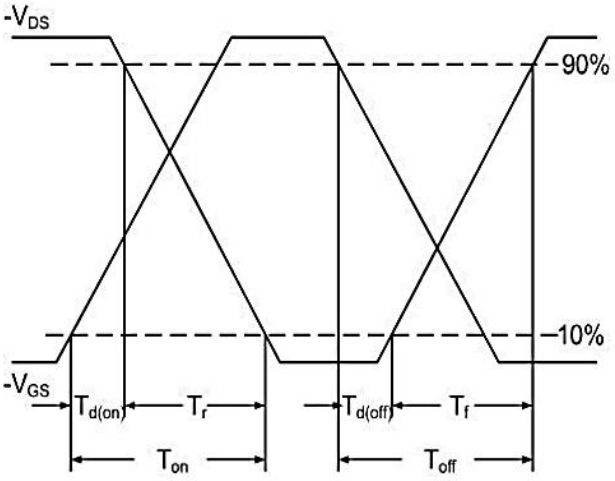


Figure 10 Switching Time Waveform

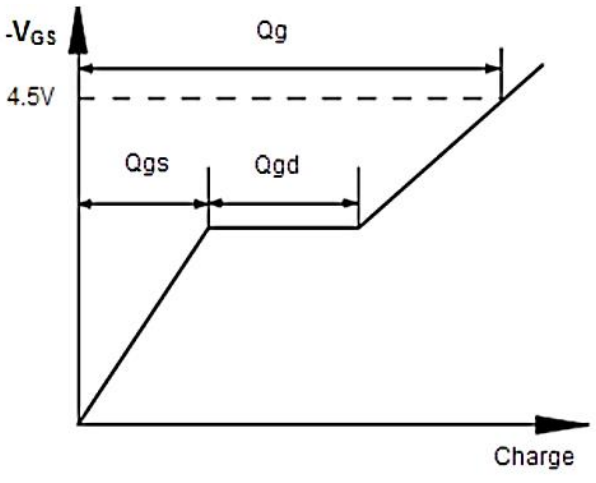
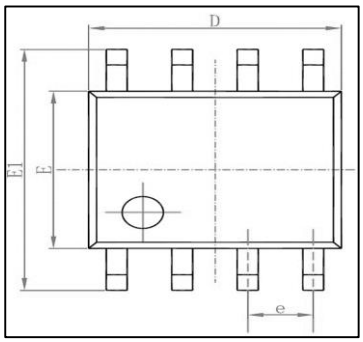
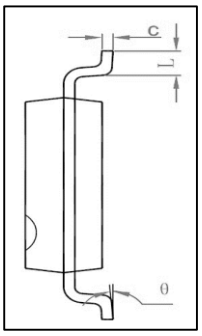
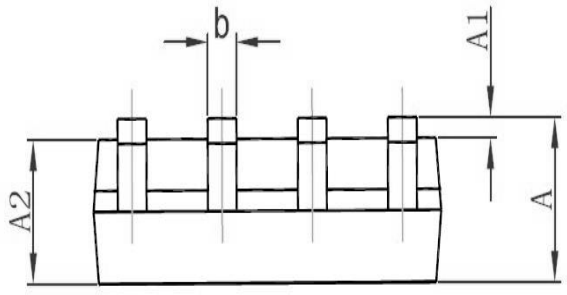


Figure 11 Gate Charge Waveform

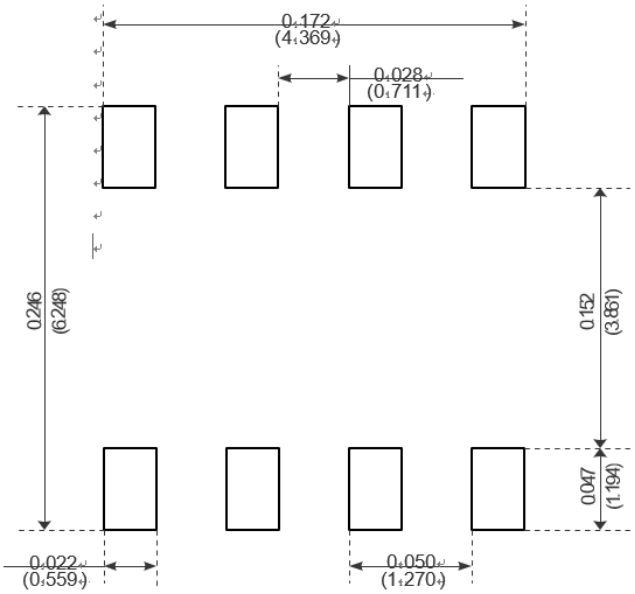
Package Mechanical Data-SOP-8L







Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



Recommended Minimum Pads

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-30V P+P-Channel Enhancement Mode MOSFET

Edition	Date	Change
Rve3.8	2020/1/31	Initial release
Rve3.9	2021/11/31	Reduce RDS