

Description

The AP4435B uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

 $V_{DS} = -30V I_{D} = -9.3A$

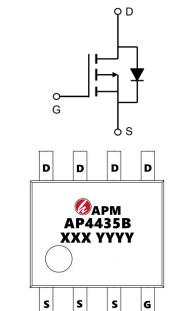
 $R_{DS(ON)}\,{<}20m\Omega\;@\;V_{GS}{=}\text{-}10V\;\;(\text{Type: }16m\Omega)$

Application

Lithium battery protection

Wireless impact

Mobile phone fast charging





PIN#1

Package Marking and Ordering Information

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Product ID	Pack	Marking	Qty(PCS)	
AP4435B	SOP-8L	AP4435B XXX YYYY	3000	

Absolute Maximum Ratings (TC=25°Cunless otherwise noted)

Symbol	Parameter	Rating	Units
VDS	Drain-Source Voltage	-30	V
VGS	Gate-Source Voltage	±20	V
I _D @T _A =25℃	Continuous Drain Current, V _{GS} @ -10V ¹	-9.3	Α
I _D @T _A =70°C	Continuous Drain Current, V _{GS} @ -10V ¹	-7.0	Α
IDM	Pulsed Drain Current ²	-50	А
P _D @T _A =25℃	Total Power Dissipation ⁴	3.1	W
P _D @T _A =70°C	Total Power Dissipation ⁴	2	W
TSTG	Storage Temperature Range	-55 to 150	$^{\circ}$
TJ	Operating Junction Temperature Range	-55 to 150	$^{\circ}$
R₀JA	Thermal Resistance Junction-Ambient ¹(t≦ 10s)	33.8	°C/W
R₀JC	Thermal Resistance Junction-Case ¹	24	°C∕W



Electrical Characteristics (T_J=25°C, unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Тур.	Max.	Units
V(BR)DSS	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D = -250μA	-30	-33	-	V
IDSS	Zero Gate Voltage Drain Current	V _{DS} = -30V, V _{GS} =0V,	-	-	-1	μA
IGSS	Gate to Body Leakage Current	V _{DS} =0V, V _{GS} = ±20V	-	-	±100	nA
VGS(th)	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D = -250µA	-1.2	-1.5	-2.5	V
DDS(on)	Chatia Dunius Courses on Decistors and Co	V _{GS} = -10V, I _D = -10A	ı	16	20	mΩ
RDS(on)	Static Drain-Source on-Resistance note3	V _{GS} = -4.5V, I _D = -5A	-	25	30	
Ciss	Input Capacitance	V _{DS} = -15V, V _{GS} =0V, f=1.0MHz	-	1550	-	pF
Coss	Output Capacitance		-	327	-	pF
Crss	Reverse Transfer Capacitance	1- 1.0IVII 12	ı	278	-	pF
Qg	Total Gate Charge	V _{DS} = -15V, I _D = -9.1A,	-	30	-	nC
Q _{gs}	Gate-Source Charge		-	5.3	-	nC
Q _{gd}	Gate-Drain("Miller") Charge	V _{GS} = -10V	-	7.6	-	nC
td(on)	Turn-on Delay Time		-	14	-	ns
tr	Turn-on Rise Time	V _{DD} = -15V, I _D = -6A,	-	20	-	ns
td(off)	Turn-off Delay Time	V_{GS} = -10V, R_{GEN} =2.5 Ω	-	95	-	ns
t _f	Turn-off Fall Time		-	65	-	ns
IS	Maximum Continuous Drain to Source Diode Forward Current		-	-	-10	Α
ISM	Maximum Pulsed Drain to Source Diode Forward Current		-	-	-40	Α
VSD	Drain to Source Diode Forward Voltage V _{GS} =0V, I _S = -11A		-	-0.8	-1.2	V

Note:

- 1. The data tested by surface mounted on a 1 inch 2 FR-4 board with 2OZ copper.
- $2\sqrt{100}$ The data tested by pulsed , pulse width ≤ 300 us , duty cycle $\leq 2\%$
- 3 The EAS data shows Max. rating . The test condition is VDD=-25V,VGS=-10V,L=0.1mH,IAS=-5A
- 4. The power dissipation is limited by 150 $\!\!\!\!^{\,\circ}\!\!\!\!^{\,\circ}$ junction temperature
- 5. The data is theoretically the same as ID and IDM, in real applications, should be limited by total power dissipation.



Typical Characteristics

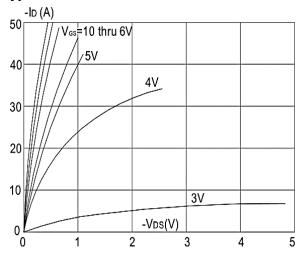


Figure1: Output Characteristics

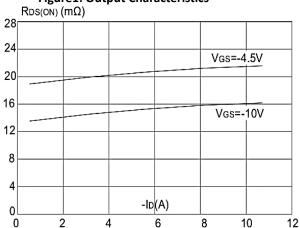


Figure 3:On-resistance vs. Drain Current

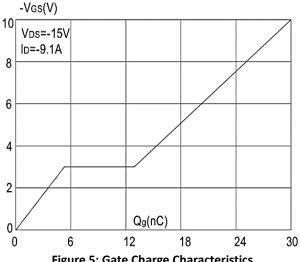


Figure 5: Gate Charge Characteristics

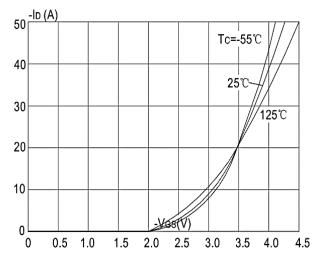


Figure 2: Typical Transfer Characteristics

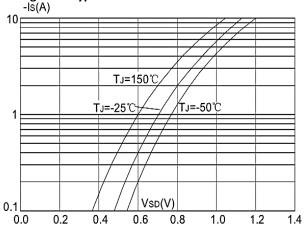


Figure 4: Body Diode Characteristics

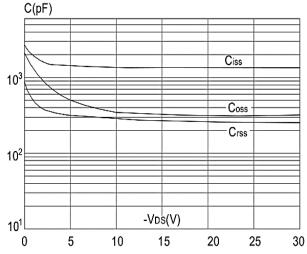


Figure 6: Capacitance Characteristics



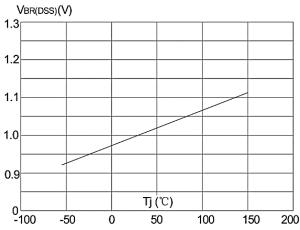


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

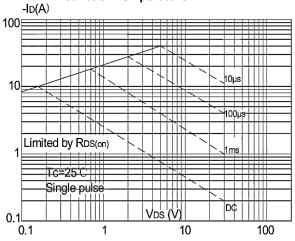


Figure 9: Maximum Safe Operating Area

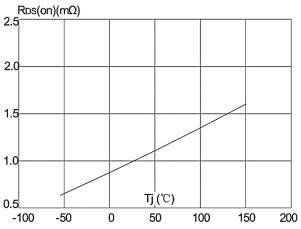


Figure 8: Normalized on Resistance vs. Junction Temperature

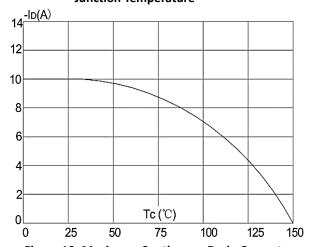


Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature

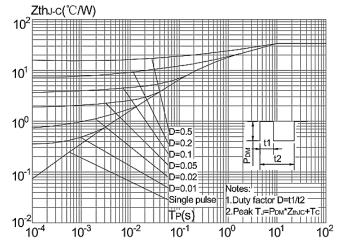
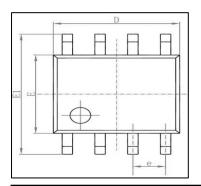
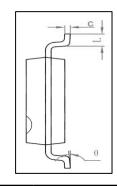


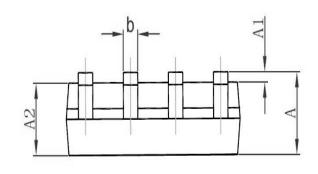
Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Ambient



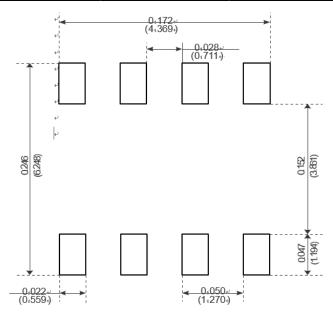
Package Mechanical Data-SOP-8







Cl	Dimensions Ir	n Millimeters	Dimensions	In Inches
Symbol	Min	Max	Min	Max
Α	1. 350	1. 750	0. 053	0.069
A1	0. 100	0. 250	0. 004	0. 010
A2	1. 350	1. 550	0. 053	0. 061
b	0. 330	0. 510	0. 013	0. 020
С	0. 170	0. 250	0.006	0. 010
D	4. 700	5. 100	0. 185	0. 200
E	3. 800	4. 000	0. 150	0. 157
E1	5. 800	6. 200	0. 228	0. 244
е	1. 270 (BSC)		0. 050 (BSC)	
L	0. 400	1. 270	0. 016	0.050
θ	0°	8°	0°	8°



Recommended Minimum Pads-



-30V P-Channel Enhancement Mode MOSFET Attention

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Edition	Date	Change
Rve1.0	2020/7/31	Initial release

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