

# AP4407B

#### Description

The AP4407B uses advanced trench technology

to provide excellent  $R_{\text{DS}(\text{ON})},$  low gate charge and

operation with gate voltages as low as 4.5V. This

device is suitable for use as a

Battery protection or in other Switching application.

#### **General Features**

V<sub>DS</sub> = -30V I<sub>D</sub> =-11.3A

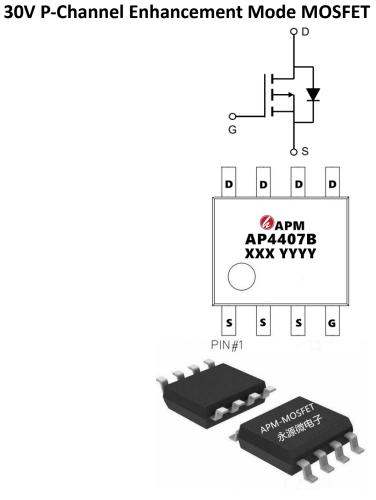
 $R_{DS(ON)}$  <16m $\Omega$  @ V<sub>GS</sub>=-10V

#### Application

Lithium battery protection

Wireless impact

Mobile phone fast charging



#### Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP4407B	SOP-8L	AP4407B XXX YYYY	3000

#### Absolute Maximum Ratings (TC=25°C unless otherwise noted)

Symbol	Parameter	Rating	Units
VDS	Drain-Source Voltage	-30	V
VGS	Gate-Source Voltage	±20	V
I <b>⊳@T</b> A <b>=25°</b> C	Continuous Drain Current, V <sub>GS</sub> @ -10V <sup>1</sup>	-11.3	А
I <b>⊳@T</b> A <b>=70</b> ℃	Continuous Drain Current, V <sub>GS</sub> @ -10V <sup>1</sup>	-8.6	А
IDM	Pulsed Drain Current <sup>2</sup>	-50	А
EAS	Single Pulse Avalanche Energy <sup>3</sup>	72.2	mJ
IAS	Avalanche Current	-38	A
P <b>D@T</b> A=25℃	Total Power Dissipation <sup>4</sup>	3.1	W
P <b></b> @T <sub>A</sub> =70℃	Total Power Dissipation <sup>4</sup>	2	W
TSTG	Storage Temperature Range	-55 to 150	°C
TJ	Operating Junction Temperature Range	-55 to 150	°C
R₀JA	Thermal Resistance Junction-Ambient <sup>1</sup> 75		°C <b>/W</b>
R₀JA	Thermal Resistance Junction-Ambient $^{1}(t \le 10s)$ 40		°C/W
R₀JC	Thermal Resistance Junction-Case <sup>1</sup>	24	°C/W

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#### **30V P-Channel Enhancement Mode MOSFET**

#### Electrical Characteristics (TJ=25°C, unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Тур.	Max.	Units
V(BR)DSS	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> = -250µA	-30	-33	-	V
IDSS	Zero Gate Voltage Drain Current	V <sub>DS</sub> = -30V, V <sub>GS</sub> =0V,	-	-	-1	μA
IGSS	Gate to Body Leakage Current	V <sub>DS</sub> =0V, V <sub>GS</sub> = ±20V	-	-	±100	nA
VGS(th)	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> = -250µA	-1.0	-1.5	-2.5	V
RDS(on)	Static Drain-Source on-Resistance note3	V <sub>GS</sub> = -10V, I <sub>D</sub> = -10A	-	11.5	16	mΩ
		V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -5A	-	16	25	
Ciss	Input Capacitance		-	2130	-	pF
Coss	Output Capacitance	V <sub>DS</sub> = -15V, V <sub>GS</sub> =0V, f=1.0MHz	-	280	-	pF
Crss	Reverse Transfer Capacitance	1-1.00012	-	252	-	pF
Qg	Total Gate Charge		-	22	-	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>DS</sub> = -15V, I <sub>D</sub> = -5A, V <sub>GS</sub> = -10V	-	4	-	nC
Q <sub>gd</sub>	Gate-Drain("Miller") Charge	VGS10V	-	5.8	-	nC
td(on)	Turn-on Delay Time		-	9	-	ns
tr	Turn-on Rise Time	V <sub>DD</sub> = -15V, I <sub>D</sub> = -10A,	-	13	-	ns
td(off)	Turn-off Delay Time	$V_{GS}$ = -10V, $R_{GEN}$ =2.5 $\Omega$	-	48	-	ns
t <sub>f</sub>	Turn-off Fall Time		-	20	-	ns
IS	Maximum Continuous Drain to Source Diode Forward Current		-	-	-11	А
ISM	Maximum Pulsed Drain to Source Diode Forward Current		-	-	-44	А
VSD	Drain to Source Diode Forward Voltage V <sub>GS</sub> =0V, I <sub>S</sub> = -11A		-	-0.8	-1.2	V

Note :

1. The data tested by surface mounted on a 1 inch 2 FR-4 board with 2OZ copper.

2. The data tested by pulsed , pulse width  $\, \leq \,$  300us , duty cycle  $\, \leq \,$  2%

3、The EAS data shows Max. rating . The test condition is VDD=-25V,VGS=-10V,L=0.1mH,IAS=-8A

4. The power dissipation is limited by 150  $^\circ\!\mathrm{C}$  junction temperature

5. The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.



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### **Typical Characteristics**

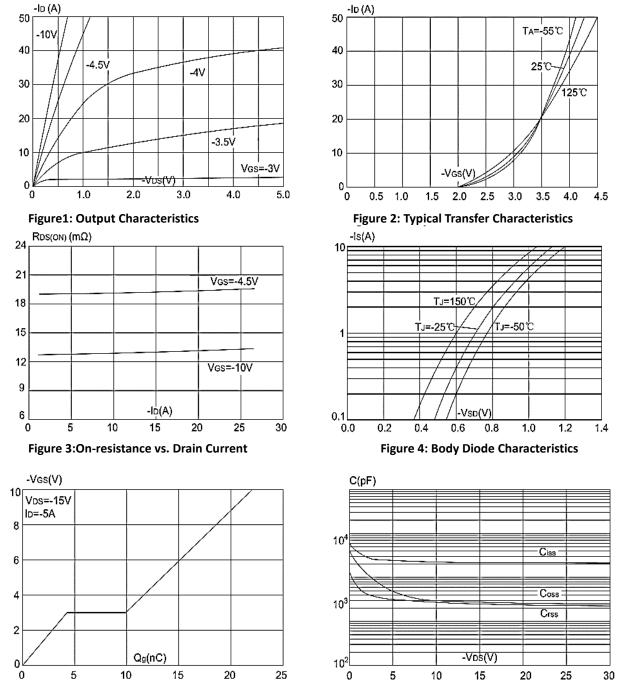


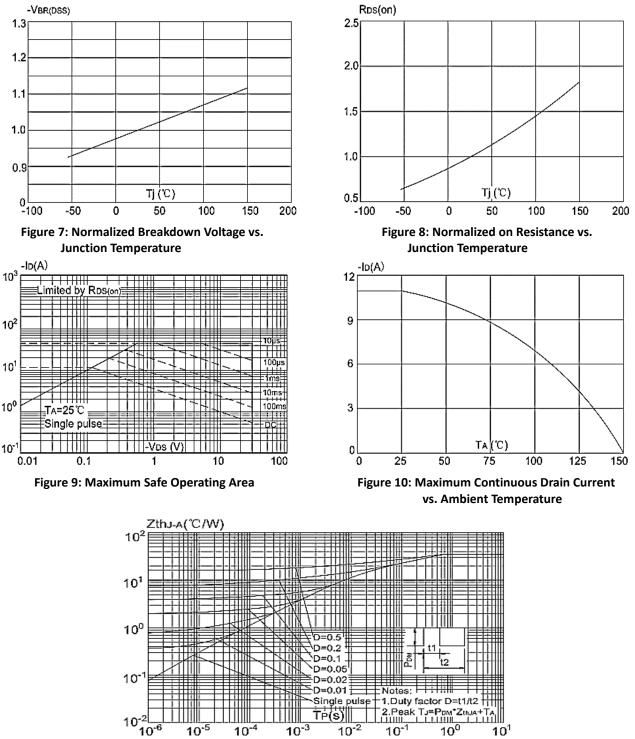
Figure 5: Gate Charge Characteristics



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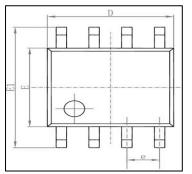
Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

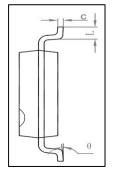


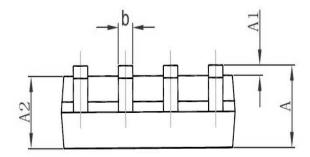
# AP4407B

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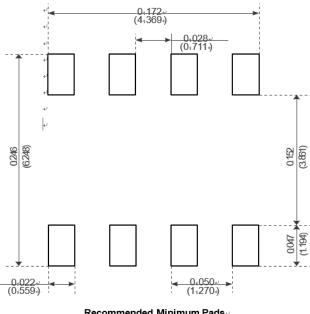
## Package Mechanical Data-SOP-8







C	Dimensions Ir	n Millimeters	Dimensions	In Inches
Symbol	Min	Max	Min	Max
A	1.350	1. 750	0. 053	0.069
A1	0.100	0. 250	0.004	0. 010
A2	1.350	1.550	0. 053	0. 061
b	0. 330	0. 510	0.013	0. 020
с	0. 170	0. 250	0.006	0. 010
D	4. 700	5. 100	0. 185	0. 200
E	3.800	4.000	0. 150	0. 157
E1	5.800	6.200	0. 228	0. 244
е	1.270	(BSC)	0.050	(BSC)
L	0.400	1. 270	0.016	0.050
θ	0°	8°	0 °	8°



Recommended Minimum Pads.

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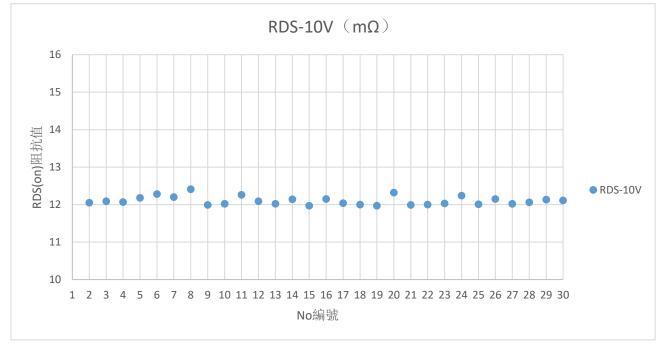
Edition	Date	Change
Rve1.0	2020/7/31	Initial release

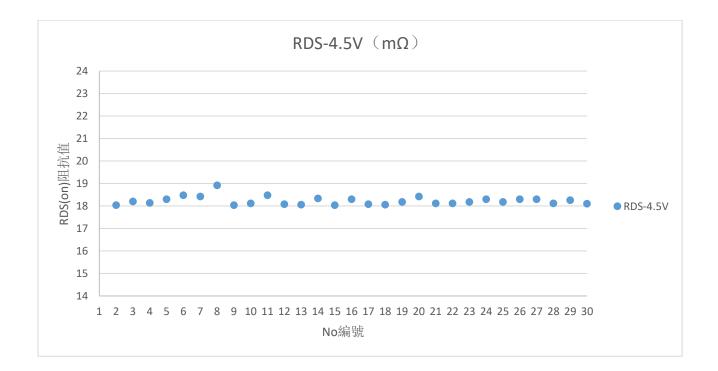
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### **30V P-Channel Enhancement Mode MOSFET**

### Test Report For 30PCS (30pcs 典型測試報告)







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