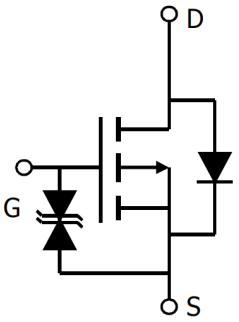
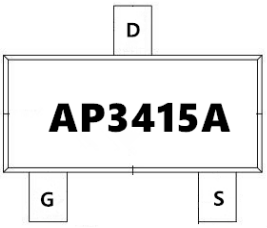
AP3415A

-20V P-Channel Enhancement Mode MOSFET

Description

The AP3415A uses advanced trench
It utilizes the latest processing techniques
to achieve the high cell density and reduces the
on-resistance with high repetitive avalanche rating.
These features combine to make this design
an extremely efficient and reliable device for use
in power switching application and a wide variety
of other applications





General Features

V_{DS} = -20V,I_D = -4.2A

$R_{DS(ON)}$ < 37mΩ @ V_{GS}=4.5V

ESD=3000V HBM

Application

Advanced MOSFET process technology

Special designed for PWM, load switching and
general purpose applications

Ultra low on-resistance with low gate charge

Fast switching and reverse body recovery

150℃ operating temperature

Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP3415A	SOT-23	AP3415A	3000

Absolute max Rating: @T_A=25℃ unless otherwise specified

Symbol	Parameter	Max.	Units
I_D @ TC = 25°C	Continuous Drain Current, V_{GS} @ 10V	-4 .2①	A
I_D @ TC = 70°C	Continuous Drain Current, V_{GS} @ 10V	-2.4 ①	
I_{DM}	Pulsed Drain Current ②	-30	
P_D @TC = 25°C	Power Dissipation ③	1.4	W
V_{DS}	Drain-Source Voltage	-20	V
V_{GS}	Gate-to-Source Voltage	± 8	V
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
$R_{\theta JA}$	Junction-to-ambient (t ≤ 10s) ④	90	°C /W

-20V P-Channel Enhancement Mode MOSFET

Electrical Characterizes @T_A=25℃ unless otherwise specified

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V(BR)DSS	Drain-to-Source breakdown voltage	V_{GS} = 0V, I_D = -250μA	-20	—	—	V
$R_{DS(on)}$	Static Drain-to-Source on-resistance	V_{GS}=-4.5V,I_D = -4A	—	37	43	mΩ
		V_{GS}=-2.5V,I_D = -4A	—	45	54	
		V_{GS}=-1.8V,I_D = -2A	—	56	73	
VGS(th)	Gate threshold voltage	V_{DS} = V_{GS}, I_D = -250μA	-0.3	—	-1.0	V
		T_J = 125°C	—	-0.44	—	
IDSS	Drain-to-Source leakage current	V_{DS} = -16V,V_{GS} = 0V	—	—	-1	μA
		T_J = 125°C	—	—	-50	
IGSS	Gate-to-Source forward leakage	V_{GS} =8V	—	—	10	μA
		V_{GS} = -8V	—	—	-10	
Q_g	Total gate charge	I_D = -4A, V_{DS}=-10V, V_{GS} = -4.5V	—	10	—	nC
Q_{gs}	Gate-to-Source charge		—	0.77	—	
Q_{gd}	Gate-to-Drain("Miller") charge		—	3.5	—	
$t_{d(on)}$	Turn-on delay time	V_{GS}=-4.5V, V_{DS} =-10V, RGEN=3Ω,	—	10	—	ns
t_r	Rise time		—	8.6	—	
$t_{d(off)}$	Turn-Off delay time		—	29	—	
t_f	Fall time		—	13	—	
C_{iss}	Input capacitance	V_{GS} = 0V, V_{DS} =-10V, f = 1MHz	—	939	—	pF
Coss	Output capacitance		—	130	—	
C_{rss}	Reverse transfer capacitance		—	111	—	

Source-Drain Ratings and Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_S	Continuous Source Current (Body Diode)	MOSFET symbol showing the integral reverse p-n junction diode.	—	—	-4.2A ①	A
I_{SM}	Pulsed Source Current (Body Diode)		—	—	-30	A
V_{SD}	Diode Forward Voltage	I_S=1A, V_{GS}=0V	—	-0.76	-1.0	V
trr	Reverse Recovery Time	TJ = 25°C, IF =-4A, di/dt = 100A/μs	—	8.7	—	ns
Qrr	Reverse Recovery Charge		—	2.3	—	nC

Notes:

①Calculated continuous current based on maximum allowable junction temperature.

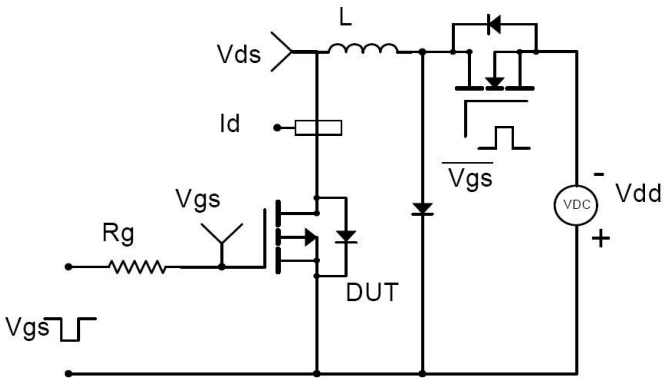
②Repetitive rating; pulse width limited by max. junction temperature.

③The power dissipation PD is based on max. junction temperature, using junction-to-case thermal resistance.

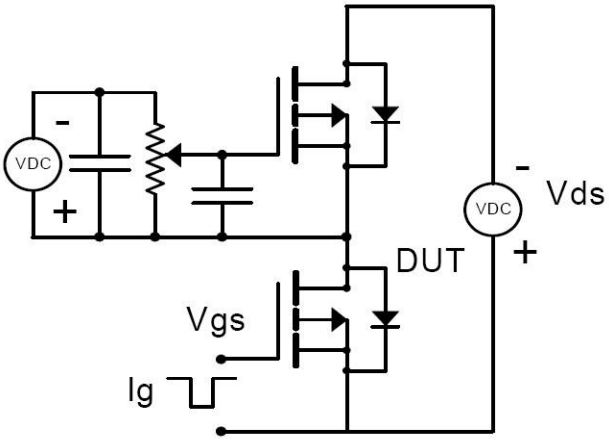
④The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with TA =25°C

Test circuits and Waveforms

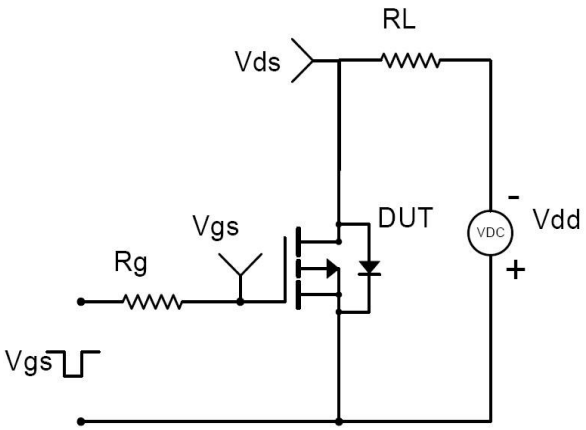
EAS test circuit:



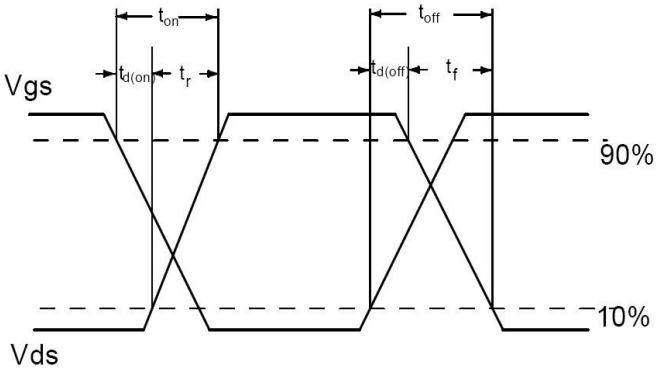
Gate charge test circuit:



Switching time test circuit:



Switch Waveforms:



Typical electrical and thermal characteristics

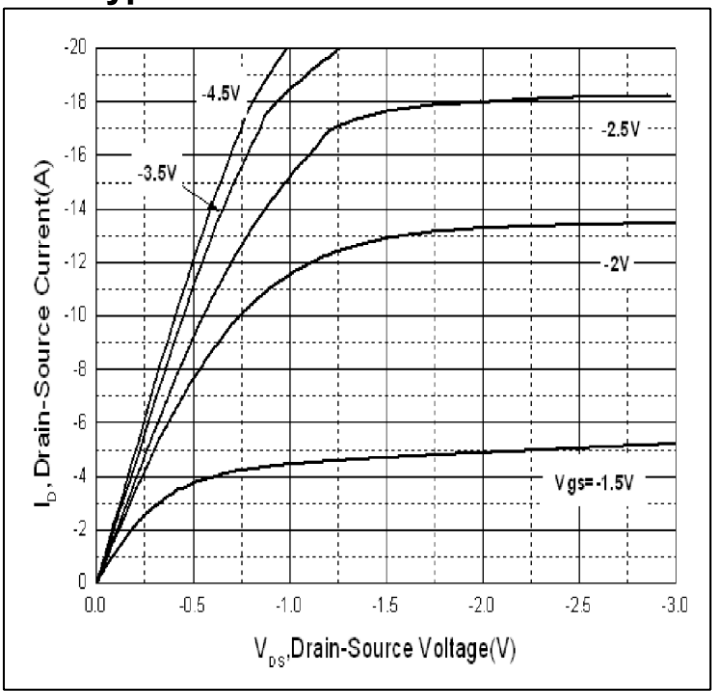


Figure 1: Typical Output Characteristics

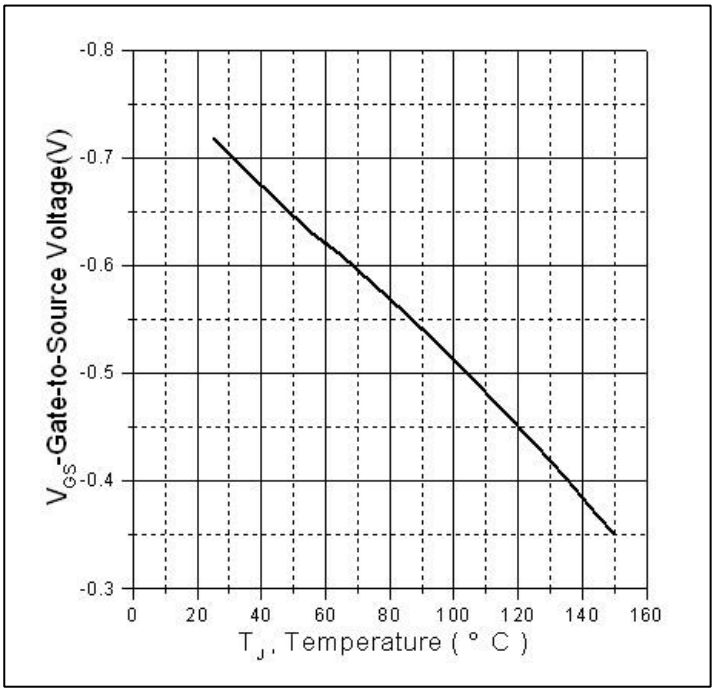


Figure 2. Gate to source cut-off voltage

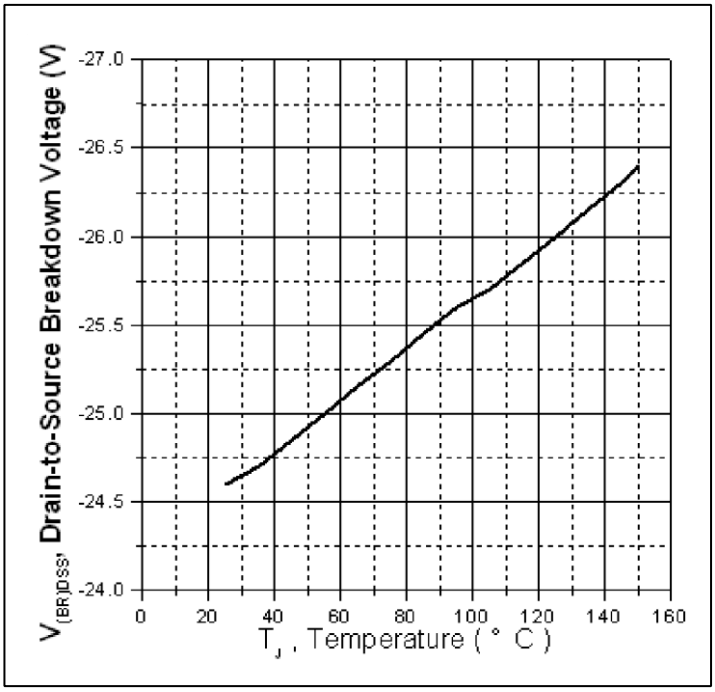


Figure 3. Drain-to-Source Breakdown Voltage Vs. Case Temperature

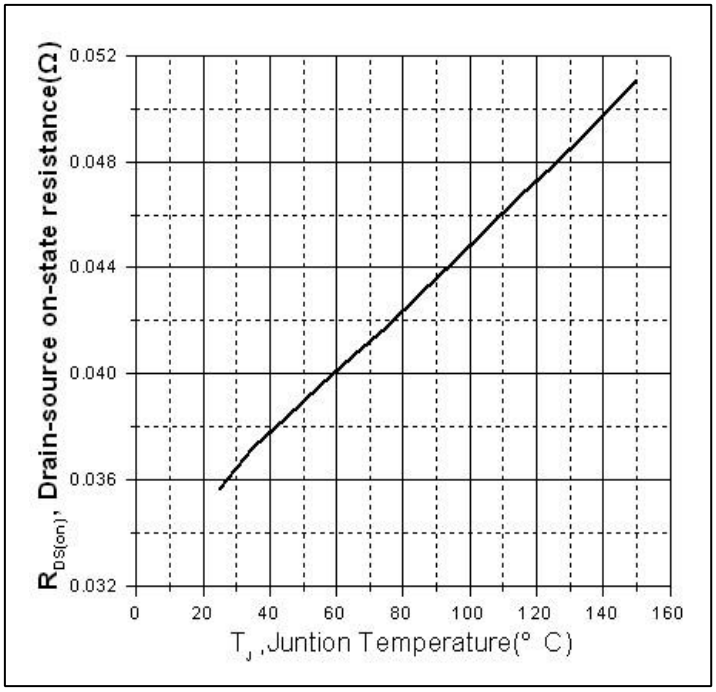


Figure 4: Normalized On-Resistance Vs. Case Temperature

Typical electrical and thermal characteristics

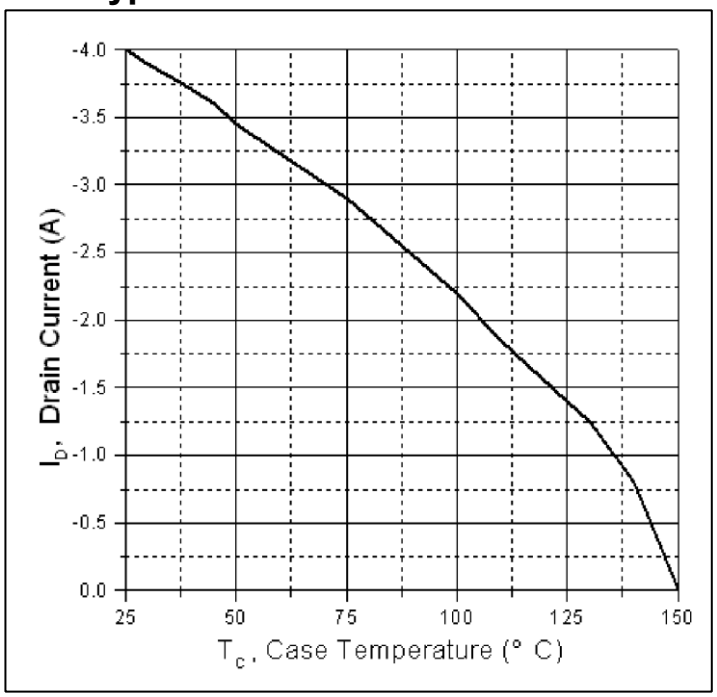


Figure 5. Maximum Drain Current Vs. Case Temperature

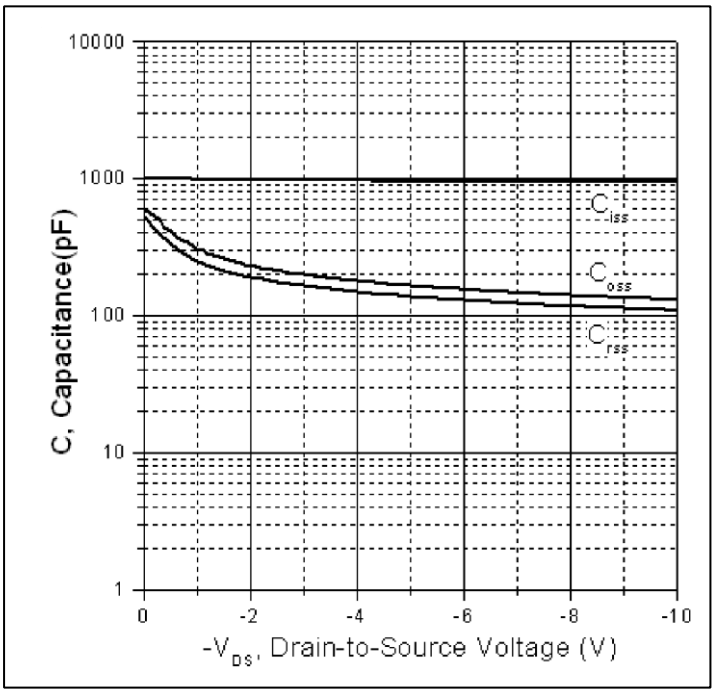


Figure 6. Typical Capacitance Vs. Drain-to-Source Voltage

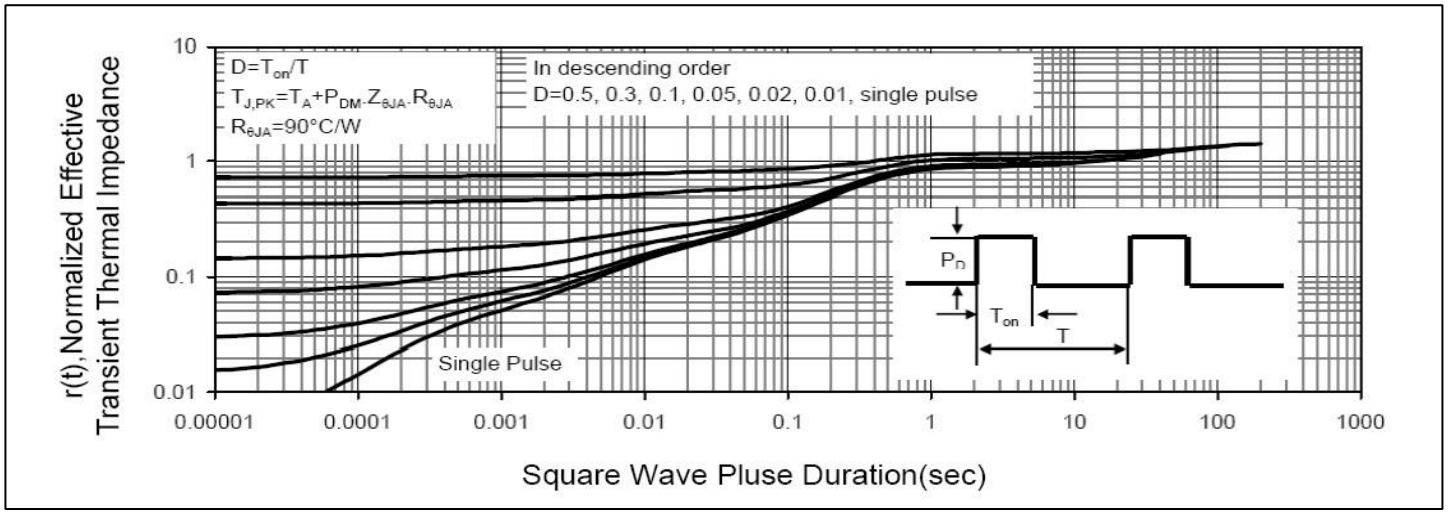
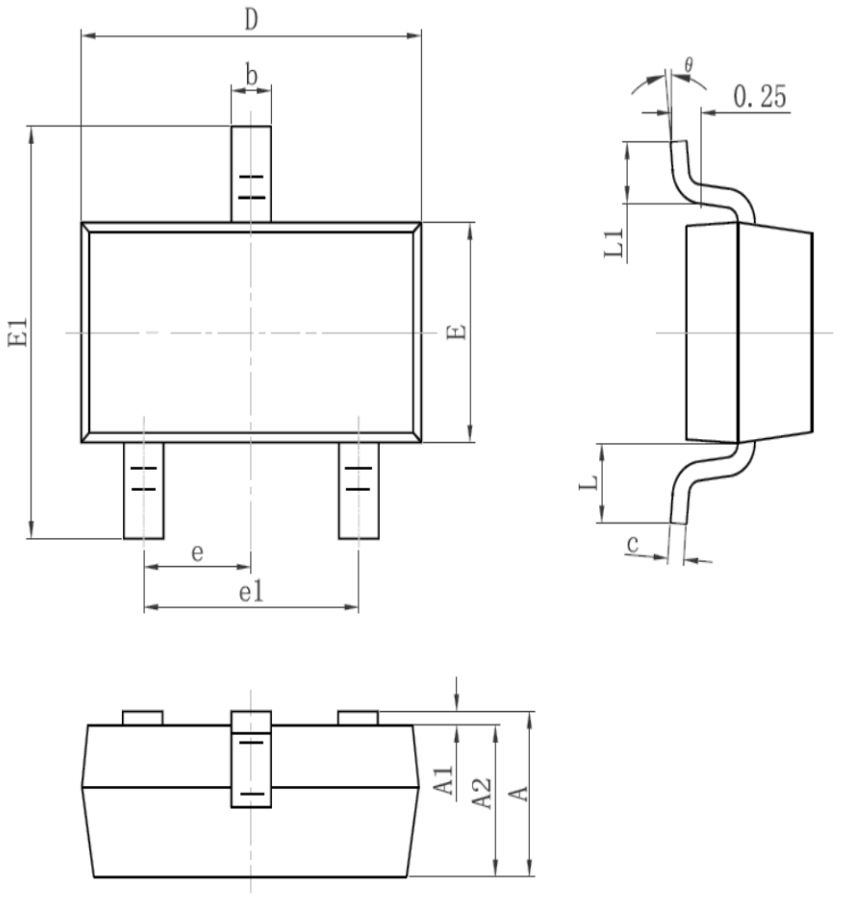


Figure7. Maximum Effective Transient Thermal Impedance Junction-to-Case

Mechanical Data

SOT-23 PACKAGE OUTLINE DIMENSION



Symbol	Dimension In Millimeters		Dimension In Inches	
	Min	Max	Min	Max
A	0.900	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.050	0.035	0.041
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.95TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.55REF		0.022REF	
L1	0.300	0.500	0.012	0.020
θ	0^0	8^0	0^0	8^0

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