

## -20V P-Channel Enhancement Mode MOSFET

### Description

The AP2301AI uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.

### General Features

$V_{DS} = -20V$   $I_D = -3.3A$

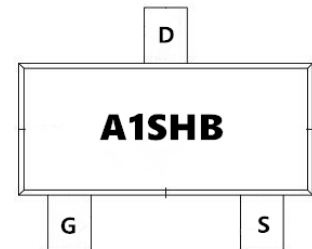
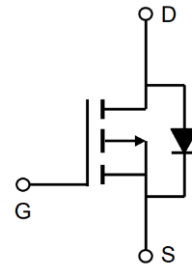
$R_{DS(ON)} < 80m\Omega @ V_{GS} = -4.5V$

### Application

Battery protection

Load switch

Uninterruptible power supply



### Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP2301AI	SOT-23	A1SHB	3000

### Absolute Maximum Ratings ( $T_C = 25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	-20	V
$V_{GS}$	Gate-Source Voltage	$\pm 12$	V
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ -4.5V^1$	-3.3	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ -4.5V^1$	-2.6	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	-13	A
$P_D @ T_A = 25^\circ C$	Total Power Dissipation <sup>3</sup>	1.4	W
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ C$
$R_{\theta JA}$	Thermal Resistance Junction-ambient <sup>1</sup>	125	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance Junction-ambient <sup>1</sup> ( $t \leq 10s$ )	90	$^\circ C/W$

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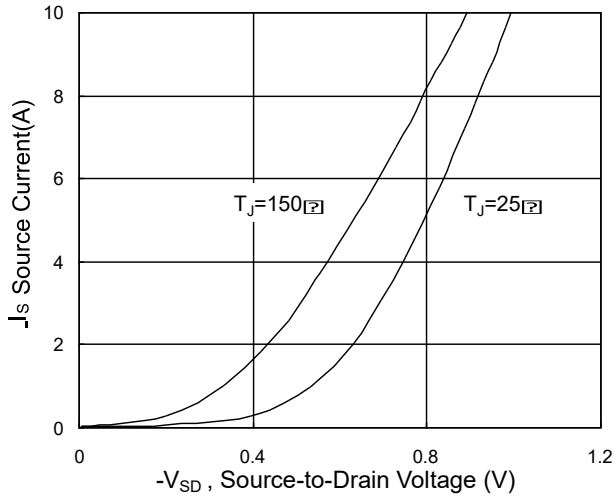
### Electrical Characteristics (T<sub>J</sub>=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =-250uA	-20	-22	---	V
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-3A	---	55	80	mΩ
		V <sub>GS</sub> =-2.5V, I <sub>D</sub> =-2A	---	75	100	
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =-250uA	-0.5	-0.7	-1.2	V
I <sub>DSS</sub>	Drain-Source Leakage Current	V <sub>DS</sub> =-20V, V <sub>GS</sub> =0V, T <sub>J</sub> =25°C	---	---	-1	uA
		V <sub>DS</sub> =-20V, V <sub>GS</sub> =0V, T <sub>J</sub> =55°C	---	---	-5	
I <sub>GSS</sub>	Gate-Source Leakage Current	V <sub>GS</sub> =±12V, V <sub>DS</sub> =0V	---	---	±100	nA
g <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> =-5V, I <sub>D</sub> =-3A	---	12.2	---	S
Q <sub>g</sub>	Total Gate Charge (-4.5V)	V <sub>DS</sub> =-15V, V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-3A	---	10.1	---	nC
Q <sub>gs</sub>	Gate-Source Charge		---	1.21	---	
Q <sub>gd</sub>	Gate-Drain Charge		---	2.46	---	
T <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> =-10V, V <sub>GS</sub> =-4.5V, R <sub>G</sub> =3.3Ω, I <sub>D</sub> =-3A	---	5.6	---	ns
T <sub>r</sub>	Rise Time		---	32.2	---	
T <sub>d(off)</sub>	Turn-Off Delay Time		---	45.6	---	
T <sub>f</sub>	Fall Time		---	29.2	---	
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =-15V, V <sub>GS</sub> =0V, f=1MHz	---	677	---	pF
C <sub>oss</sub>	Output Capacitance		---	82	---	
C <sub>rss</sub>	Reverse Transfer Capacitance		---	73	---	
I <sub>s</sub>	Continuous Source Current <sup>1,4</sup>	V <sub>G</sub> =V <sub>D</sub> =0V, Force Current	---	---	-3	A
V <sub>SD</sub>	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V, I <sub>s</sub> =-1A, T <sub>J</sub> =25°C	---	---	-1	V

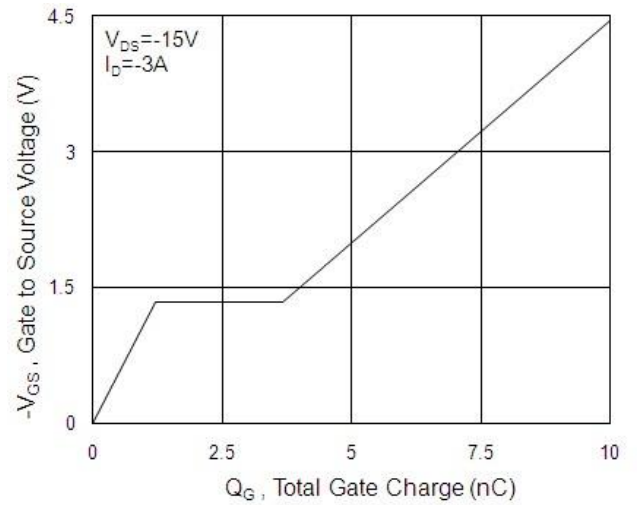
**Note :**

- 1、 The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2、 The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%
- 3、 The power dissipation is limited by 150°C junction temperature
- 4、 The data is theoretically the same as I<sub>D</sub> and I<sub>DM</sub> , in real applications , should be limited by total power dissipation.

### Typical Characteristics

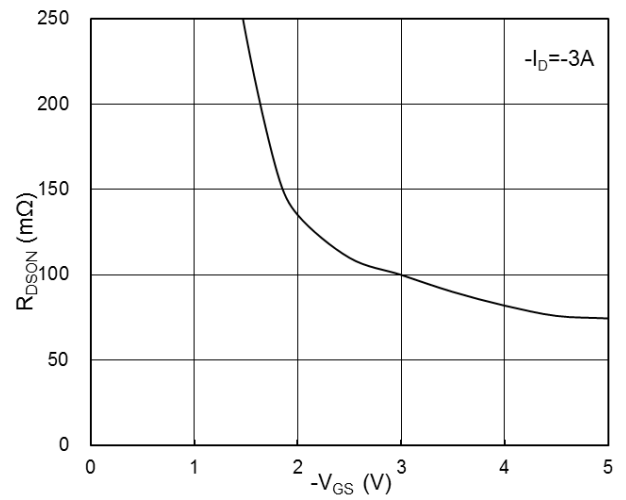
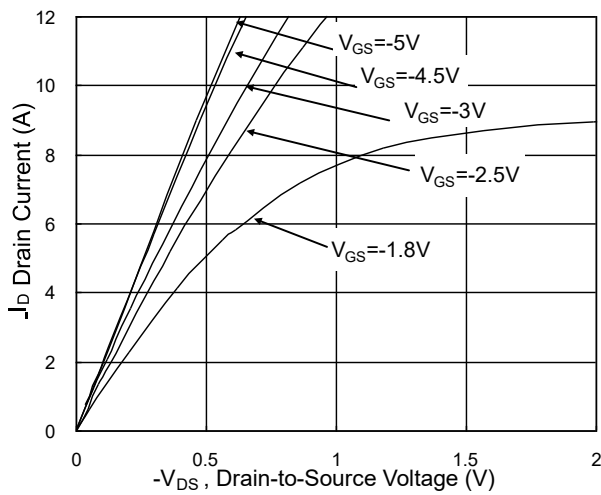


**Fig.1 Typical Output Characteristics**

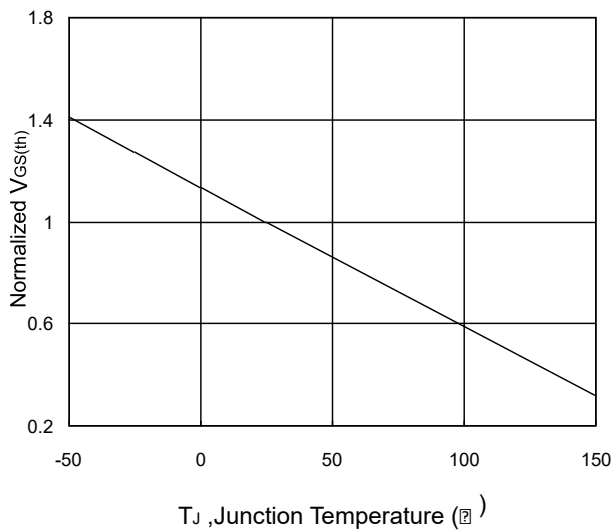


**Fig.3**

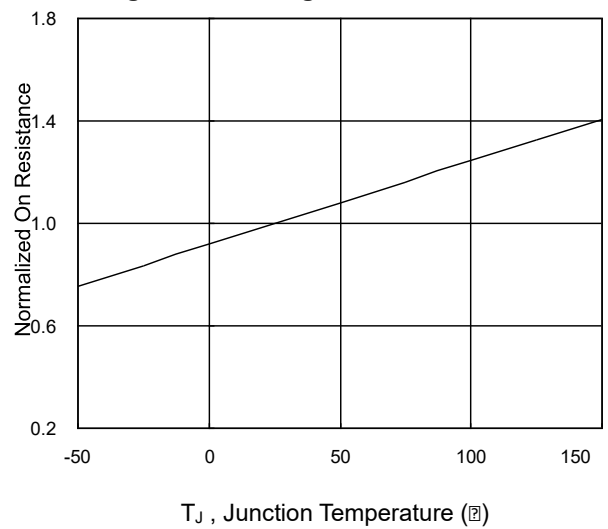
**Fig.2 On-Resistance vs. G-S Voltage**



### Source Drain Forward Characteristics

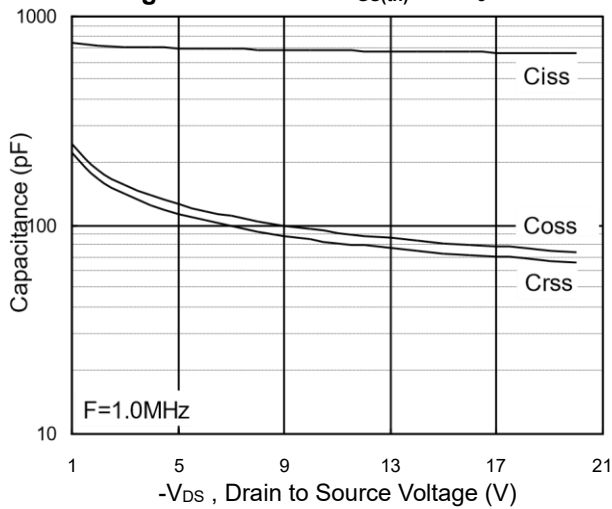


### Fig.4 Gate-Charge Characteristics



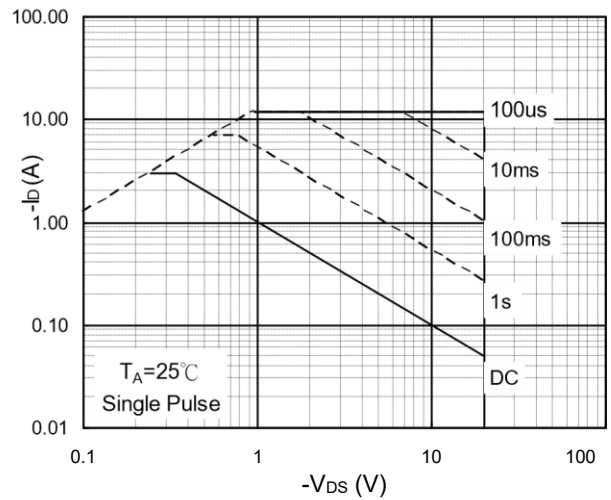
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**Fig.5 Normalized  $V_{GS(th)}$  vs.  $T_J$**

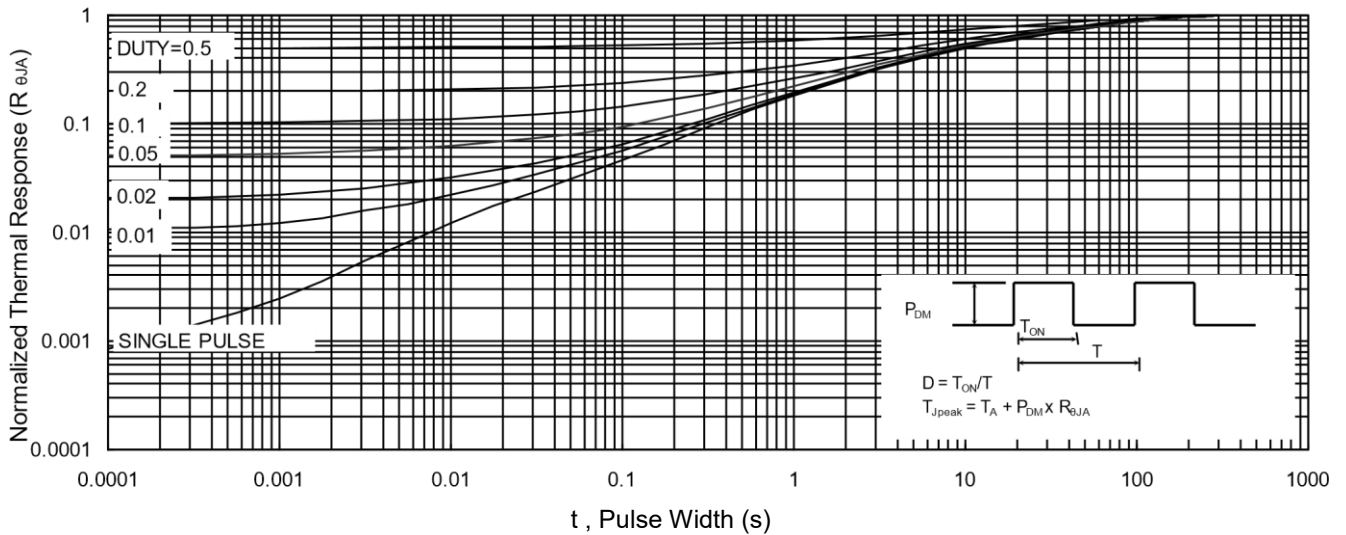


**Fig.7 Capacitance**

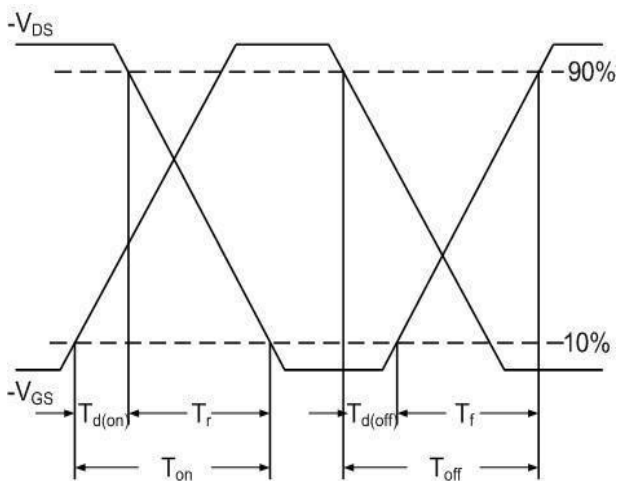
**Fig.6 Normalized  $R_{DS(on)}$  vs.  $T_J$**



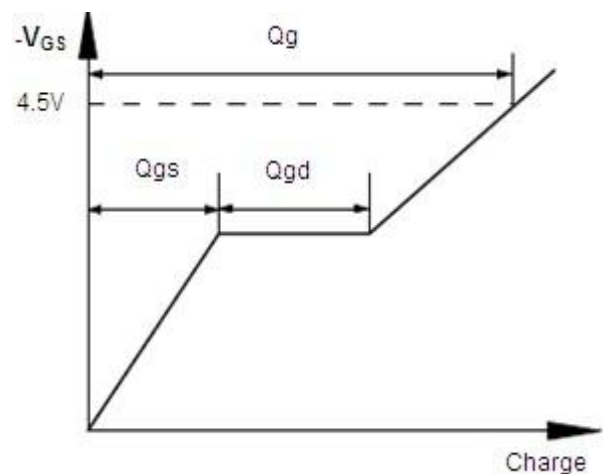
**Fig.8 Safe Operating Area**



**Fig.9 Normalized Maximum Transient Thermal Impedance**

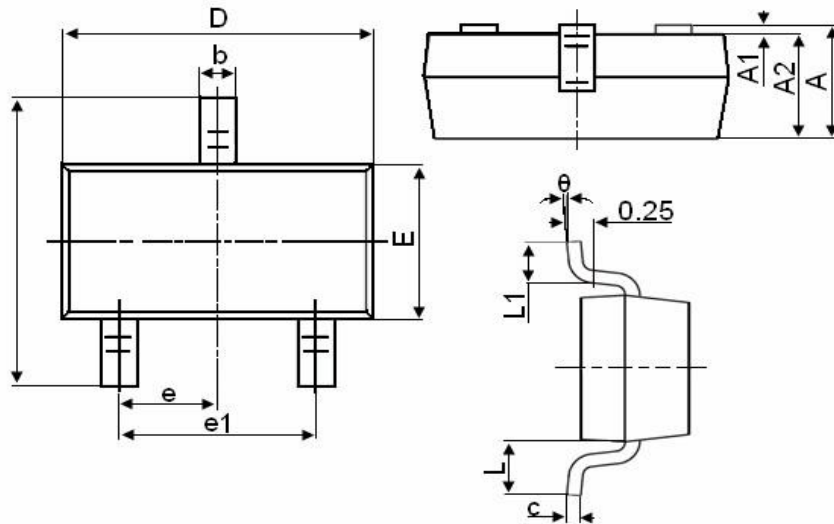


**Fig.10 Switching Time Waveform**



**Fig.11 Gate Charge Waveform**

### Package Mechanical Data-SOT-23



Symbol	Dimensions in Millimeters	
	MIN.	MAX.
A	0.900	1.150
A1	0.000	0.100
A2	0.900	1.050
b	0.300	0.500
c	0.080	0.150
D	2.800	3.000
E	1.200	1.400
E1	2.250	2.550
e	0.950TYP	
e1	1.800	2.000
L	0.550REF	
L1	0.300	0.500
θ	0°	8°

**-20V P-Channel Enhancement Mode MOSFET****Attention**

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<b>Edition</b>	<b>Date</b>	<b>Change</b>
RVE1.2	2017/6/19	Initial release
RVE1.3	2020/8/19	Reduce RDS(on)

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